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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe162fm72f80lrabfxuma1

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Summary of Features

1.2 Definition of Feature Variants

The XE162xM types are offered with several Flash memory sizes. **Table 2** describes the location of the available memory areas for each Flash memory size.

Total Flash Size	Flash Area A ¹⁾	Flash Area B	Flash Area C
576 Kbytes	C0'0000 _H	C1'0000 _H	СС'0000 _н
	C0'EFFF _H	C7'FFFF _H	СС'FFFF _н
384 Kbytes	C0'0000 _H	C1'0000 _H	СС'0000 _н
	C0'EFFF _H	C4'FFFF _H	СС'FFFF _н
192 Kbytes	C0'0000 _H	C1'0000 _H	СС'0000 _н
	C0'EFFF _H	C1'FFFF _H	СС'FFFF _н

Table 2 Flash Memory Allocation

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

Table 3	Flash Memory	Module Allocation	(in Kbv	tes)
		medale / medalen	(

Total Flash Size	Flash 0 ¹⁾	Flash 1	Flash 2	Flash 3
576 Kbytes	256	256		64
384 Kbytes	256	64		64
192 Kbytes	128			64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XE162xM types are offered with different interface options. Table 4 lists the available channels for each option.

Table 4	Interface	Channel	Association

Total Number	Available Channels	
7 ADC0 channels	CH0, CH2, CH4, CH8, CH10, CH13, CH15	
2 ADC1 channels	CH0, CH4	
2 CAN nodes	CAN0, CAN1 64 message objects	
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1	



General Device Information

2.2 Identification Registers

The identification registers describe the current version of the XE162xM and of its modules.

Table 6 XE162xM Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820 _H	00'F07E _H	
SCU_IDCHIP	3801 _H	00'F07C _H	
SCU_IDMEM	30D0 _H	00'F07A _H	
SCU_IDPROG	1313 _H	00'F078 _H	
JTAG_ID	0017'E083 _H		marking EES-AA, ES-AA or AA



Functional Description

3.5 Interrupt System

The architecture of the XE162xM supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE162xM has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11¹⁾ CPU clocks, the XE162xM can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XE162xM provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

¹⁾ Depending if the jump cache is used or not.



Functional Description

3.8 Capture/Compare Units CCU6x

The XE162xM types feature the CCU60 unit(s).

The CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal (CTRAP)
- · Control modes for multi-channel AC drives
- · Output levels can be selected and adapted to the power stage



XE162FM, XE162HM XE166 Family / Base Line

Functional Description



Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.



Functional Description

3.17 Parallel Ports

The XE162xM provides up to 40 I/O lines which are organized into 4 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in Table 9.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Port	Width	I/O	Connected Modules
P2	11	I/O	CAN, CC2, GPT12E, USIC, DAP/JTAG
P5	7	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	2	I/O	ADC, CAN, GPT12E
P7	1	I/O	CAN, GPT12E, SCU, DAP/JTAG, USIC
P10	16	I/O	CCU6, USIC, DAP/JTAG, CAN
P15	2	I	Analog Inputs, GPT12E

Table 9Summary of the XE162xM's Ports



4 Electrical Parameters

The operating range for the XE162xM is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

4.1.1 Absolut Maximum Rating Conditions

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.

During absolute maximum rating overload conditions ($V_{\rm IN} > V_{\rm DDP}$ or $V_{\rm IN} < V_{\rm SS}$) the voltage on $V_{\rm DDP}$ pins with respect to ground ($V_{\rm SS}$) must not exceed the values defined by the absolute maximum ratings.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Output current on a pin when high value is driven	I _{OH} SR	-30	-	-	mA	
Output current on a pin when low value is driven	I _{OL} SR	-	-	30	mA	
Overload current	I _{OV} SR	-10	-	10	mA	1)
Absolute sum of overload currents	$\Sigma I_{\rm OV} $ SR	-	-	100	mA	1)
Junction Temperature	$T_{\sf J}{\sf SR}$	-40	-	150	°C	
Storage Temperature	$T_{\rm ST}{ m SR}$	-65	-	150	°C	
Digital supply voltage for IO pads and voltage regulators	$V_{ m DDPA}, V_{ m DDPB}$	-0.5	-	6.0	V	
Voltage on any pin with respect to ground (Vss)	$V_{\rm IN}$ SR	-0.5	-	V _{DDP} + 0.5	V	$V_{\rm IN} \leq V_{\rm DDP(max)}$

Table 11 Absolute Maximum Rating Parameters

 Overload condition occurs if the input voltage V_{IN} is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.



Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Absolute sum of overload currents	$\Sigma I_{\rm OV} $ SR	-	-	50	mA	not subject to production test
Digital core supply voltage for domain M ⁸⁾	V _{DDIM} CC	-	1.5	_		
Digital core supply voltage for domain 1 ⁸⁾	V _{DDI1} CC	-	1.5	-		
Digital supply voltage for IO pads and voltage regulators	$V_{\rm DDP}{ m SR}$	4.5	-	5.5	V	
Digital ground voltage	$V_{\rm SS}{\rm SR}$	_	0	_	V	

Table 12 Operating Conditions (cont'd)

To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

2) Use one Capacitor for each pin.

- This is the reference load. For bigger capacitive loads, use the derating factors listed in the PAD properties section.
- 4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).
- 5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.
- 6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: V_{OV} > V_{IHmax} (I_{OV} > 0) or V_{OV} < V_{ILmin} ((I_{OV} < 0). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).
- 7) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pins leakage current (I_{OZ}) . The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV} . The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| K_{OV})$. The additional error current may distort the input voltage on analog inputs.
- 8) Value is controlled by on-chip regulator



- 2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.
 - In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to $3 + 0.6 \text{ x} f_{SYS}$.
- 3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XE162xM's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.

A small current is consumed because the drivers' input stages are switched.

The IO power domains can be supplied separately. Power domain A ($V_{\rm DDPA}$) supplies the A/D converters and Port 6. Power domain B ($V_{\rm DDPB}$) supplies the on-chip EVVRs and all other ports.

During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from $V_{\rm DDPA}$.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to $(3 + 0.6 \times f_{SYS})$ mA.



Table 16 Leakage Power Consumption

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Leakage supply current (DMP_1 powered) ¹⁾	$I_{\rm LK1}$ CC	-	0.03	0.05	mA	$T_{\rm J}$ = 25 °C ¹⁾
		-	0.5	1.3	mA	$T_{\rm J} = 85 \ ^{\circ}{\rm C}^{1)}$
		-	2.1	6.2	mA	$T_{\rm J}$ = 125 °C ¹⁾
		-	4.4	13.7	mA	$T_{\rm J}$ = 150 °C ¹⁾

 All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

Note: A fraction of the leakage current flows through domain DMP_A (pin V_{DDPA}). This current can be calculated as 7 000 × e^{- α}, with α = 5 000 / (273 + 1.3× T_{J}). For T_{J} = 150°C, this results in a current of 160 μ A.

The leakage power consumption can be calculated according to the following formulas:

 $I_{\rm LK0}$ = 500 000 × e^{- α}, with α = 3 000 / (273 + B× $T_{\rm J}$)

Parameter B must be replaced by

- 1.0 for typical values
- 1.6 for maximum values

 $I_{LK1} = 600\ 000 \times e^{-\alpha}$, with $\alpha = 5\ 000\ /\ (273 + B \times T_J)$

Parameter B must be replaced by

- 1.0 for typical values
- 1.3 for maximum values



XE162FM, XE162HM XE166 Family / Base Line

Electrical Parameters



Figure 15 Leakage Supply Current as a Function of Temperature



Table 17ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Broken wire detection delay against VAGND ²⁾	t _{BWG} CC	-	-	50	3)	
Broken wire detection delay against VAREF ²⁾	t _{BWR} CC	-	-	50	4)	
Conversion time for 8-bit result ²⁾	t _{c8} CC	(11 + S ⁻ + 2 x t _S	TC) x t _{AD} YS	ICI		
Conversion time for 10-bit result ²⁾	<i>t</i> _{c10} CC	(13 + S ⁻ + 2 x t _S	TC) x t _{AD} YS	ICI		
Total Unadjusted Error	TUE CC	-	1	2	LSB	5)
Wakeup time from analog powerdown, fast mode ²⁾	t _{WAF} CC	-	-	4	μS	
Wakeup time from analog powerdown, slow mode ²⁾	t _{WAS} CC	-	-	15	μS	
Analog reference ground	$V_{ m AGND}$ SR	V _{SS} - 0.05	-	1.5	V	
Analog input voltage range	$V_{\rm AIN}{ m SR}$	$V_{\rm AGND}$	-	V_{AREF}	V	6)
Analog reference voltage	V_{AREF} SR	V _{AGND} + 1.0	-	V _{DDPA} + 0.05	V	5)

 These parameter values cover the complete operating range. Under relaxed operating conditions (room temperature, nominal supply voltage) the typical values can be used for calculation.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

- 3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% (66_H).
- 4) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 μs. This function is influenced by leakage current, in particular at high temperature. Result above 80% (332_H).
- 5) TUE is tested at V_{AREF} = V_{DDPA} = 5.0 V, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.
- V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.



- 3) $f_{\rm WU}$ in MHz
- 4) This value includes a hysteresis of approximately 50 mV for rising voltage.
- 5) $V_{\rm LV}$ = selected SWD voltage level
- 6) The limit V_{LV} 0.10 V is valid for the OK1 level. The limit for the OK2 level is V_{LV} 0.15 V.

Conditions for t_{SPO} Timing Measurement

The time required for the transition from **Power-On** to **Base** mode is called t_{SPO} . It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. V_{DDPB} is above 3.0 V and remains above 3.0 V even though the XE162xM is starting up. No debugger is attached.

Start condition: Power-on reset is removed ($\overline{PORST} = 1$).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSO} Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called t_{SSO} . It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on ESR pin triggering the startup sequence.

Coding of bit fields LEVxV in SWD and PVC Configuration Registers

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

Table 20 County of bit neius LEVXV III Register SWDCONU							
Code	Default Voltage Level	Notes ¹⁾					
0000 _B	2.9 V						
0001 _B	3.0 V	LEV1V: reset request					
0010 _B	3.1 V						
0011 _B	3.2 V						
0100 _B	3.3 V						
0101 _B	3.4 V						
0110 _B	3.6 V						
0111 _B	4.0 V						
1000 _B	4.2 V						

Table 20 Coding of bit fields LEVxV in Register SWDCON0



Table 20	Coding of bit fields LEVxV in Register SWDCON0 (cont'd)							
Code	Default Voltage Level	Notes ¹⁾						
1001 _B	4.5 V	LEV2V: no request						
1010 _B	4.6 V							
1011 _B	4.7 V							
1100 _B	4.8 V							
1101 _B	4.9 V							
1110 _B	5.0 V							
1111 _B	5.5 V							

1) The indicated default levels are selected automatically after a power reset.

Table 21 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes ¹⁾
000 _B	0.95 V	
001 _B	1.05 V	
010 _B	1.15 V	
011 _B	1.25 V	
100 _B	1.35 V	LEV1V: reset request
101 _B	1.45 V	LEV2V: interrupt request ²⁾
110 _B	1.55 V	
111 _B	1.65 V	

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use the this warning level.



4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE162xM. The clock can be generated in two ways:

- By connecting a crystal or ceramic resonator to pins XTAL1/XTAL2
- By supplying an external clock signal
 - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain)

If connected to CLKIN1, the input signal must reach the defined input levels $V_{\rm IL}$ and $V_{\rm IH}$. If connected to XTAL1, a minimum amplitude $V_{\rm AX1}$ (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters $(t_1 \dots t_4)$ are only valid for an external clock input signal.

Note: Operating Conditions apply.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Oscillator frequency	$f_{\rm OSC}{\rm SR}$	4	-	40	MHz	Input = clock signal
		4	_	16	MHz	Input = crystal or ceramic resonator
XTAL1 input current absolute value	I _{IL} CC	-	-	20	μA	
Input clock high time	t ₁ SR	6	-	-	ns	
Input clock low time	t ₂ SR	6	-	-	ns	
Input clock rise time	t ₃ SR	-	-	8	ns	
Input clock fall time	t ₄ SR	-	-	8	ns	
Input voltage amplitude on XTAL1 ¹⁾	$V_{\rm AX1}{ m SR}$	$0.3 ext{ x}$ $V_{ ext{DDIM}}$	-	-	V	4 to 16 MHz
		$0.4 ext{ x}$ $V_{ ext{DDIM}}$	-	-	V	16 to 25 MHz
		$0.5 ext{ x}$ $V_{ ext{DDIM}}$	-	-	V	25 to 40 MHz
Input voltage range limits for signal on XTAL1	$V_{\rm IX1}$ SR	-1.7 + V _{DDIM}	-	1.7	V	2)

Table 24 External Clock Input Characteristics



Parameter	Symbol		Values		Unit	Note /
		Min.	Тур.	Max.		Test Condition
Receive data input setup time to SCLKOUT receive edge	t ₄ SR	40	-	-	ns	
Data input DX0 hold time from SCLKOUT receive edge	t ₅ SR	-5	_	_	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 29 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol		Values		Unit	Note / Test Condition
		Min.	Тур.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	<i>t</i> ₁₀ SR	7	-	-	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	<i>t</i> ₁₁ SR	7	-	-	ns	
Receive data input setup time to shift clock receive edge ¹⁾	<i>t</i> ₁₂ SR	7	_	-	ns	
Data input DX0 hold time from clock input DX1 receive edge ¹⁾	<i>t</i> ₁₃ SR	5	-	-	ns	
Data output DOUT valid time	<i>t</i> ₁₄ CC	7	-	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).



4.6.6 Debug Interface Timing

The debugger can communicate with the XE162xM either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; C_L = 20 pF.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
DAP0 clock period	<i>t</i> ₁₁ SR	25 ¹⁾	-	-	ns	
DAP0 high time	t ₁₂ SR	8	-	-	ns	
DAP0 low time	t ₁₃ SR	8	-	-	ns	
DAP0 clock rise time	<i>t</i> ₁₄ SR	-	_	4	ns	
DAP0 clock fall time	t ₁₅ SR	-	_	4	ns	
DAP1 setup to DAP0 rising edge	<i>t</i> ₁₆ SR	6	-	-	ns	pad_type= stan dard
DAP1 hold after DAP0 rising edge	<i>t</i> ₁₇ SR	6	-	-	ns	pad_type= stan dard
DAP1 valid per DAP0 clock period ²⁾	<i>t</i> ₁₉ CC	17	20	-	ns	pad_type= stan dard

 Table 31
 DAP Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \ge t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.



Package and Reliability

5 Package and Reliability

The XE166 Family devices use the package type PG-LQFP (Plastic Green - Low Profile Quad Flat Package). The following specifications must be regarded to ensure proper integration of the XE162xM in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Parameter	Symbol	Lin	nit Values	Unit	Notes
		Min.	Max.		
Power Dissipation	P _{DISS}	_	1.0	W	-
Thermal resistance	$R_{\Theta JA}$	-	58	K/W	No thermal via ¹⁾
Junction-Ambient			46	K/W	4-layer, no pad ²⁾

 Table 35
 Package Parameters (PG-LQFP-64-13)

1) Device mounted on a 2-layer JEDEC board (according to JESD 51-3) or a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias.

Package Compatibility Considerations

The XE162xM is a member of the XE166 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.



Package and Reliability

Package Outlines



Figure 28 PG-LQFP-64-13 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": http://www.infineon.com/packages



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5.2 Thermal Considerations

When operating the XE162xM in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 125 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta,IA}$

The internal power consumption is defined as

 $P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as $P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}} \cdot V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- · Reduce the number of output pins
- Reduce the load on active output drivers