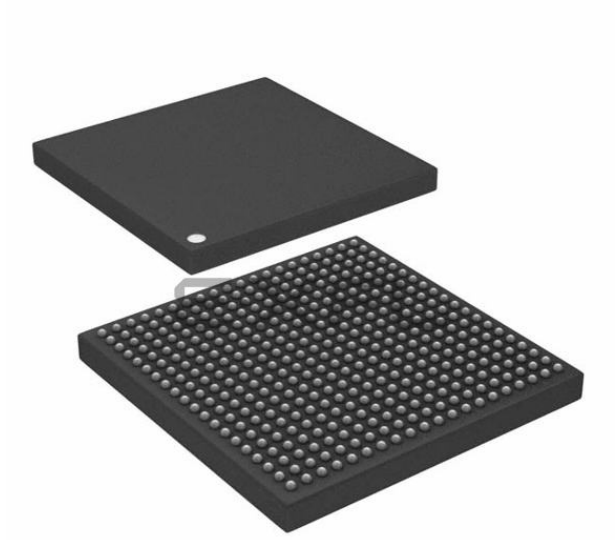

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	External
On-Chip RAM	1.768MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21573bbcz-4

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6/2018—Rev. A to Rev. B

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ARM CORTEX-A5 PROCESSOR

The ARM Cortex-A5 processor (see Figure 2) is a high performance processor with the following features:

- Instruction cache unit (32 Kb) and data Level 1 (L1) cache unit (32 Kb)
- In order pipeline with dynamic branch prediction
- ARM, Thumb, and ThumbEE instruction set support
- ARM TrustZone® security extensions
- Harvard L1 memory system with a memory management unit (MMU)
- ARM v7 debug architecture
- Trace support through an embedded trace macrocell (ETM) interface
- Extension—vector floating-point unit (IEEE754) with trapless execution
- Extension—media processing engine (MPE) with NEON™ technology
- Extension—Jazelle® hardware acceleration

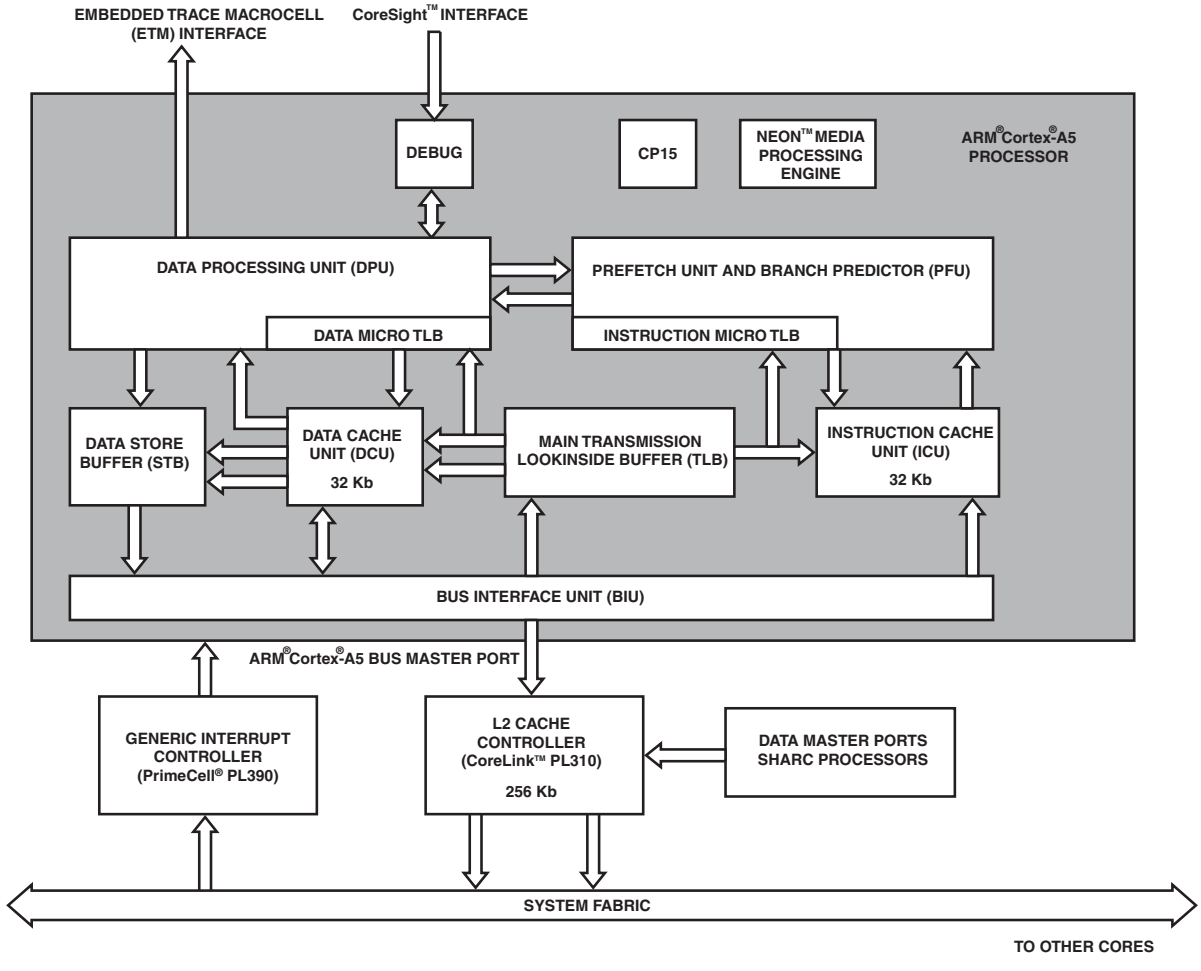


Figure 2. ARM Cortex-A5 Processor Block Diagram

The system configuration is flexible, but a typical configuration is 512 Kb DM, 128 Kb PM, and 128 Kb of instruction cache, with the remaining L1 memory configured as SRAM. Each addressable memory space outside the L1 memory can be accessed either directly or via cache.

The memory map in Table 4 gives the L1 memory address space and shows multiple L1 memory blocks offering a configurable mix of SRAM and cache.

L1 Master and Slave Ports

Each SHARC+ core has two master ports and two slave ports to and from the system fabric. One master port fetches instructions. The second master port drives data to the system world. Slave port 1 together with slave port 2 (MDMA) run conflict free access to the individual memory blocks. For the slave port address, refer to the L1 memory address map in Table 4.

L1 On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks, assuming no block conflicts. The total bandwidth is realized using both the DMD and PMD buses (2 × 64-bits CCLK speed and 2 × 32-bit SYSCLK speed).

Instruction and Data Cache

The ADSP-SC57x/ADSP-2157x processors also include a traditional instruction cache (I-cache) and two data caches (D-cache) (PM/DM caches) with parity support for all caches. These caches support one instruction access and two data accesses over the DM and PM buses, per CCLK cycle. The cache controllers automatically manage the configured L1 memory. The system can configure part of the L1 memory for automatic management by the cache controllers. The sizes of these caches are independently configurable from 0 kB to a maximum of 128 kB each. The memory not managed by the cache controllers is directly addressable by the processors. The controllers ensure the data coherence between the two data caches. The caches provide user-controllable features such as full and partial locking, range bound invalidation, and flushing.

System Event Controller (SEC) Input

The output of the system event controller (SEC) controller is forwarded to the core event controller (CEC) to respond directly to all unmasked system-based interrupts. The SEC also supports nesting including various SEC interrupt channel arbitration options. The processor automatically stacks the arithmetic status (ASTATx and ASTATy) registers and mode (MODE1) register in parallel with the interrupt servicing for all SEC channels.

Core Memory-Mapped Registers (CMMR)

The core memory-mapped registers (CMMR) control the L1 instruction and data cache, BTB, L2 cache, parity error, system control, debug, and monitor functions.

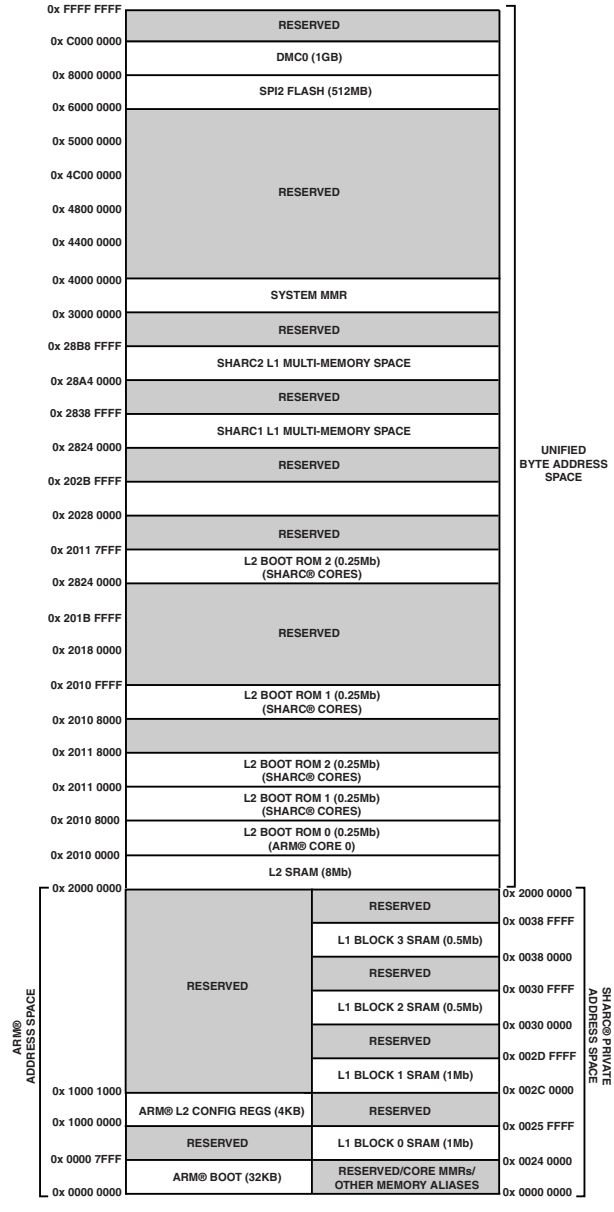


Figure 5. ADSP-SC57x/ADSP-2157x Memory Map

SHARC+ CORE ARCHITECTURE

The ADSP-SC57x/ADSP-2157x processors are code compatible at the assembly level with the ADSP-2148x, ADSP-2147x, ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-2116x, and with the first-generation ADSP-2106x SHARC processors.

The ADSP-SC57x/ADSP-2157x processors share architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-214xx, and ADSP-2116x SIMD SHARC processors, shown in Figure 4 and detailed in the following sections.

acting as either a master device or a slave device. In a multimaster environment, the SPI peripheral uses open-drain outputs to avoid data bus contention. The flow control features enable slow slave devices to interface with fast master devices by providing an SPI ready pin (SPI_RDY) which flexibly controls the transfers.

The baud rate and clock phase and polarities of the SPI port are programmable. The port has integrated DMA channels for both transmit and receive data streams.

Link Port (LP)

Two 8-bit wide link ports (LPs) for the BGA package (one link port for the LQFP package) can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional and have eight data lines, an acknowledge line, and a clock line.

ADC Control Module (ACM) Interface

The ADC control module (ACM) provides an interface that synchronizes the controls between the processors and an ADC. The analog-to-digital conversions are initiated by the processors, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

The ACM synchronizes the ADC conversion process, generating the ADC controls, the ADC conversion start signal, and other signals. The actual data acquisition from the ADC is done by an internal DAI routing of the ACM with the SPORT0 block.

The processors interface directly to many ADCs without any glue logic required.

Ethernet Media Access Controller (EMAC)

The processor features an ethernet media access controller (EMAC): 10/100/1000 AVB Ethernet with precision time protocol (IEEE 1588).

The processors can directly connect to a network through embedded fast EMAC that supports 10Base-T (10 Mb/sec), 100Base-T (100 Mb/sec) and 1000Base-T (1 Gb/sec) operations.

Some standard features of the EMAC are as follows:

- Support and MII/RMII/RGMII protocols for external PHYs.
- RGMII support for the BGA package only
- Full-duplex and half-duplex modes
- Media access management (in half-duplex operation)
- Flow control
- Station management, including the generation of MDC/MDIO frames for read/write access to PHY registers

Some advanced features of the EMAC include the following:

- Automatic checksum computation of IP header and IP payload fields of receive frames
- Independent 32-bit descriptor driven receive and transmit DMA channels
- Frame status delivery to memory through DMA, including frame completion semaphores for efficient buffer queue management in software
- Transmit DMA support for separate descriptors for MAC header and payload fields to eliminate buffer copy operations
- Convenient frame alignment modes
- 47 MAC management statistics counters with selectable clear on read behavior and programmable interrupts on half maximum value
- Advanced power management
- Magic packet detection and wakeup frame filtering
- Support for 802.3Q tagged VLAN frames
- Programmable MDC clock rate and preamble suppression

Audio Video Bridging (AVB) Support

The 10/100/1000 EMAC supports the following audio video bridging (AVB) features:

- Separate channels or queues for AV data transfer in 100 Mbps and 1000 Mbps modes)
- IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for the additional transmit channels
- Configuring up to two additional channels (Channel 1 and Channel 2) on the transmit and receive paths for AV traffic. Channel 0 is available by default and carries the legacy best effort Ethernet traffic on the transmit side.
- Separate DMA, transmit and receive FIFO for AVB latency class
- Programmable control to route received VLAN tagged non AV packets to channels or queues

Precision Time Protocol (PTP) IEEE 1588 Support

The IEEE 1588 standard is a precision clock synchronization protocol for networked measurement and control systems. The processors include hardware support for IEEE 1588 with an integrated precision time protocol synchronization engine (PTP_TSYNC).

This engine provides hardware assisted time stamping to improve the accuracy of clock synchronization between PTP nodes. The main features of the engine include the following:

- Support for both IEEE 1588-2002 and IEEE 1588-2008 protocol standards
- Hardware assisted time stamping capable of up to 12.5 ns resolution
- Lock adjustment
- Automatic detection of IPv4 and IPv6 packets, as well as PTP messages
- Multiple input clock sources (SCLK0, RGMII, RMII, MII clock, and external clock)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

Controller Area Network (CAN)

There are two controller area network (CAN) modules. A CAN controller implements the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to the capability to communicate reliably over a network. This is because the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit)
- Dedicated acceptance masks for each mailbox
- Additional data filtering on the first two bytes
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats
- Support for remote frames
- Active or passive network support
- Interrupts, including transmit and receive complete, error, and global

An additional crystal is not required to supply the CAN clock because it is derived from a system clock through a programmable divider.

Timers

The processors include several timers that are described in the following sections.

General-Purpose (GP) Timers (TIMER)

There is one general-purpose (GP) timer unit, providing eight GP programmable timers. Each timer has an external pin that can be configured either as PWM or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TM_TMR[n] pins, an external TM_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software autobaud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault). Each timer can also be started and/or stopped by any TRU master without core intervention.

Watchdog Timer (WDT)

Three on-chip software watchdog timers (WDT) can be used by the ARM Cortex-A5 and/or SHARC+ cores. A software watchdog can improve system availability by forcing the processors to a known state, via a general-purpose interrupt, or a fault, if the timer expires before being reset by software.

The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to zero from the programmed value, protecting the system from remaining in an unknown state where software that normally resets the timer stops running due to an external noise condition or software error.

General-Purpose Counters (CNT)

A 32-bit counter (CNT) is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can input the push button signal of thumbwheel devices. All three CNT0 pins have a programmable debouncing circuit.

Internal signals forwarded to a GP timer enable the timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

Housekeeping Analog-to-Digital Converter (HADC)

The housekeeping analog-to-digital converter (HADC) provides a general-purpose, multichannel successive approximation ADC. It supports the following set of features:

- 12-bit ADC core with built in sample and hold.
- Eight single-ended input channels for the BGA package; four single-ended input channels for the LQFP package.
- Throughput rates up to 1 MSPS.
- Single external reference with analog inputs between 0 V and 3.3 V.
- Selectable ADC clock frequency including the ability to program a prescaler.
- Adaptable conversion type; allows single or continuous conversion with option of autoscan.
- Autosequencing capability with up to eight autoconversions in a single session. Each conversion can be programmed to select one to eight input channels.
- Six data registers (individually addressable) to store conversion values

USB 2.0 On the Go (OTG) Dual-Role Device Controller (BGA Only)

The USB supports high speed/full speed/low speed (HS/FS/LS) USB2.0 on the go (OTG).

The USB 2.0 OTG dual-role device controller provides a low cost connectivity solution in industrial applications, as well as consumer mobile devices such as cell phones, digital still cameras, and MP3 players. The USB 2.0 controller allows these devices to transfer data using a point to point USB connection without the need for a PC host. The module can operate in a traditional USB peripheral only mode as well as the host mode presented in the OTG supplement to the USB 2.0 specification.

Board Support Packages (BSPs) for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add ins called board support packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product.

Middleware Packages

Analog Devices offers middleware add ins such as real-time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos2
- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/ucusbh
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add ins that perform popular audio and video processing algorithms. These are available for use with CrossCore Embedded Studio. For more information visit www.analog.com.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG test access port (TAP). In circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the internal features of the processor via the TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers.

The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the JTAG port of the DSP to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see "Analog Devices JTAG Emulation Technical Reference" (EE-68).

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-SC57x/ADSP-2157x architecture and functionality. For detailed information on the core architecture and instruction set, refer to the SHARC+ Core Programming Reference.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (www.analog.com\circuits) provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 20. ADSP-SC57x/ADSP-2157x 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPI2_MISO	SPI2 Master In, Slave Out	B	PB_10
SPI2_MOSI	SPI2 Master Out, Slave In	B	PB_11
SPI2_RDY	SPI2 Ready	C	PC_00
$\overline{\text{SPI2\_SEL1}}$	SPI2 Slave Select Output 1	B	PB_15
$\overline{\text{SPI2\_SEL2}}$	SPI2 Slave Select Output 2	A	PA_07
$\overline{\text{SPI2\_SEL3}}$	SPI2 Slave Select Output 3	C	PC_00
$\overline{\text{SPI2\_SEL4}}$	SPI2 Slave Select Output 4	D	PD_08
$\overline{\text{SPI2\_SEL5}}$	SPI2 Slave Select Output 5	A	PA_15
$\overline{\text{SPI2\_SEL6}}$	SPI2 Slave Select Output n	A	PA_10
$\overline{\text{SPI2\_SEL7}}$	SPI2 Slave Select Output n	B	PB_07
$\overline{\text{SPI2\_SS}}$	SPI2 Slave Select Input	B	PB_15
SYS_BMODE0	Boot Mode Control n	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control n	Not Muxed	SYS_BMODE1
SYS_CLKIN0	Clock/Crystal Input	Not Muxed	SYS_CLKIN0
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
$\overline{\text{SYS\_FAULT}}$	Active-High Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_XTAL0	Crystal Output	Not Muxed	SYS_XTAL0
TM0_ACI0	TIMER0 Alternate Capture Input 0	A	PA_06
TM0_ACI1	TIMER0 Alternate Capture Input 1	A	PA_08
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_12
TM0_ACI3	TIMER0 Alternate Capture Input 3	C	PC_14
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_13
TM0_ACI5	TIMER0 Alternate Capture Input 5	Not Applicable	DAI_PB04_O
TM0_ACI6	TIMER0 Alternate Capture Input 6	Not Applicable	DAI_PB19_O
TM0_ACI7	TIMER0 Alternate Capture Input 7	Not Applicable	CNT0_TO
TM0_ACLK1	TIMER0 Alternate Clock 1	A	PA_00
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_01
TM0_ACLK3	TIMER0 Alternate Clock 3	D	PD_09
TM0_ACLK4	TIMER0 Alternate Clock 4	C	PC_11
TM0_ACLK5	TIMER0 Alternate Clock 5	Not Applicable	DAI_PB03_O
TM0_ACLK6	TIMER0 Alternate Clock 6	Not Applicable	DAI_PB20_O
TM0_ACLK7	TIMER0 Alternate Clock 7	Not Applicable	SYS_CLKIN0
TM0_CLK	TIMER0 Clock	C	PC_03
TM0_TMR0	TIMER0 Timer 0	D	PD_02
TM0_TMR1	TIMER0 Timer 1	D	PD_03
TM0_TMR2	TIMER0 Timer 2	D	PD_04
TM0_TMR3	TIMER0 Timer 3	B	PB_01
TM0_TMR4	TIMER0 Timer 4	B	PB_03
TM0_TMR5	TIMER0 Timer 5	C	PC_15
TM0_TMR7	TIMER0 Timer 7	D	PD_07
TRACE0_CLK	TRACE0 Trace Clock	A	PA_00
TRACE0_D00	TRACE0 Trace Data	A	PA_01
TRACE0_D01	TRACE0 Trace Data	A	PA_02
TRACE0_D02	TRACE0 Trace Data	A	PA_03
TRACE0_D03	TRACE0 Trace Data	A	PA_04
TRACE0_D04	TRACE0 Trace Data	D	PD_10

ADSP-SC57x/ADSP-2157x DESIGNER QUICK REFERENCE

Table 25 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The type column identifies the I/O type or supply type of the pin. The abbreviations used in this column are analog (a), supply (s), ground (g) and Input, Output, and InOut.
- The driver type column identifies the driver type used by the corresponding pin. The driver types are defined in the Output Drive Currents section of this data sheet.
- The internal termination column specifies the termination present after the processor is powered up (both during reset and after reset).
- The reset drive column specifies the active drive on the signal when the processor is in the reset state.
- The power domain column specifies the power supply domain in which the signal resides.
- The description and notes column identifies any special requirements or characteristics for a signal. These recommendations apply whether or not the hardware block associated with the signal is featured on the product. If no special requirements are listed, the signal can be left unconnected if it is not used. For multiplexed GPIO pins, this column identifies the functions available on the pin.

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
DAI0_PIN01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 1 Notes: See note[2]
DAI0_PIN02	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 2 Notes: See note[2]
DAI0_PIN03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 3 Notes: See note[2]
DAI0_PIN04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 4 Notes: See note[2]
DAI0_PIN05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 5 Notes: See note[2]
DAI0_PIN06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 6 Notes: See note[2]
DAI0_PIN07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 7 Notes: See note[2]
DAI0_PIN08	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 8 Notes: See note[2]
DAI0_PIN09	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 9 Notes: See note[2]
DAI0_PIN10	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 10 Notes: See note[2]
DAI0_PIN11	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 11 Notes: See note[2]
DAI0_PIN12	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 12 Notes: See note[2]
DAI0_PIN13	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 13 Notes: See note[2]
DAI0_PIN14	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 14 Notes: See note[2]
DAI0_PIN15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 15 Notes: See note[2]

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
PD_00	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 0 Notes: See note[2]
PD_01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 1 Notes: See note[2]
PD_02	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 2 Notes: See note[2]
PD_03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 3 Notes: See note[2]
PD_04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 4 Notes: See note[2]
PD_05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 5 Notes: See note[2]
PD_06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 6 Notes: See note[2]
PD_07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 7 Notes: See note[2]
PD_08	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 8 Notes: See note[2]
PD_09	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 9 Notes: See note[2]
PD_10	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 10 Notes: See note[2]
PD_11	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 11 Notes: See note[2]
PD_12	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 12 Notes: See note[2]
PD_13	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 13 Notes: See note[2]
PD_14	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 14 Notes: See note[2]
PD_15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 15 Notes: See note[2]
PE_00	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 0 Notes: See note[2]
PE_01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 1 Notes: See note[2]
PE_02	InOut	H	none	none	VDD_EXT	Desc: PORTE Position 2 Notes: Connect to VDD_EXT or GND if not used
PE_03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 3 Notes: See note[2]
PE_04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 4 Notes: See note[2]
PE_05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 5 Notes: See note[2]
PE_06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 6 Notes: See note[2]
PE_07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 7 Notes: See note[2]

Parameter		Conditions	Min	Typ	Max	Unit
I_{DD_IDLE}	V_{DD_INT} Current in Idle	f_{CCLK} = 500 MHz ASF_{SHARC1} = 0.32 ASF_{SHARC2} = 0.32 ASF_{A5} = 0.25 f_{SYSCLK} = 250 MHz $f_{SCLK0/1}$ = 125 MHz (Other clocks are disabled) No Peripheral or DMA activity T_J = 25°C V_{DD_INT} = 1.15 V		477		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 450 MHz ASF_{SHARC1} = 1.0 ASF_{SHARC2} = 1.0 ASF_{A5} = 0.67 f_{SYSCLK} = 225 MHz $f_{SCLK0/1}$ = 112.5 MHz (Other clocks are disabled) DMA data rate = 600 MB/s T_J = 25°C V_{DD_INT} = 1.1 V		890		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 500 MHz ASF_{SHARC1} = 1.0 ASF_{SHARC2} = 1.0 ASF_{A5} = 0.67 f_{SYSCLK} = 250 MHz $f_{SCLK0/1}$ = 125 MHz (Other clocks are disabled) DMA data rate = 600 MB/s T_J = 25°C V_{DD_INT} = 1.15 V		1031		mA
I_{DD_INT}[11]	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK0/1} \geq 0$ MHz			See $I_{DD\_INT\_TOT}$ equation in the Total Internal Power Dissipation section.	mA

[1] Applies to all output and bidirectional pins except TWI, DMC, USB, and MLB.
[2] See the Output Drive Currents section for typical drive current capabilities.
[3] Applies to all DMC output and bidirectional signals in DDR2 mode.
[4] Applies to all DMC output and bidirectional signals in DDR3 mode.
[5] Applies to all DMC output and bidirectional signals in LPDDR mode.
[6] Applies to input pins: SYS_BMODE0-2, SYS_CLKIN0, SYS_CLKIN1, $\overline{\text{SYS\_HWRST}}$, JTG_TDI, JTG_TMS, and USB0_CLKIN.
[7] Applies to input pins with internal pull-ups: JTG_TDI, JTG_TMS, and JTG_TCK.
[8] Applies to signals: JTAG_TRST, USB0_VBUS.
[9] Applies to signals: PA0-15, PB0-15, PC0-15, PD0-15, PE0-15, PF0-11, DAI0_PINx, DMC0_DQx, DMC0_LDQS, DMC0_UDQS, $\overline{\text{DMC0\_LDQS}}$, $\overline{\text{DMC0\_UDQS}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, JTG_TDO, USB0_ID, USB0_DM, USB0_DP, and USB0_VBC.
[10] Applies to all signal pins.
[11] See "Estimating Power for ADSP-SC57x/2157x SHARC+ Processors" (EE-397) for further information.

Table 32. Dynamic Current for Each SHARC+®Core (mA, with ASF = 1.00)[1]

f_{CCLK} (MHz)	Voltage (V_{DD_INT})			
	1.05	1.10	1.15	1.20
500	N/A	347	362	378
450	298	312	326	340
400	265	277	290	302
350	232	243	254	265
300	198	208	217	227
250	165	173	181	189
200	132	139	145	151
150	99	104	109	113
100	66	69	72	76

[1] N/A means not applicable.

Table 33. Dynamic Current for the ARM® Cortex®-A5 Core (mA, with ASF = 1.00)[1]

f_{CCLK} (MHz)	Voltage (V_{DD_INT})			
	1.05	1.10	1.15	1.20
500	N/A	88	92	96
450	76	79	83	86
400	67	70	74	77
350	59	62	64	67
300	50	53	55	58
250	42	44	46	48
200	34	35	37	39
150	25	26	28	29
100	17	18	18	19

[1] N/A means not applicable.

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency, and a unique scaling factor.

$I_{DD\_INT\_SYSCLK\_DYN}$ (mA) = 0.52 × f_{SYSCLK} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_SCLK0\_DYN}$ (mA) = 0.28 × f_{SCLK0} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_SCLK1\_DYN}$ (mA) = 0.013 × f_{SCLK1} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_DCLK\_DYN}$ (mA) = 0.08 × f_{DCLK} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_OCLK\_DYN}$ (mA) = 0.015 × f_{OCLK} (MHz) × V_{DD_INT} (V)

Current from High Speed Peripheral Operation

The following modules contribute significantly to power dissipation, and a single term is added when they are used.

$I_{DD\_INT\_USB\_DYN}$ = 9.6 mA (if USB is enabled in HS mode)

$I_{DD\_INT\_MLB\_DYN}$ = 10 mA (if MLB 6-pin interface is enabled)

$I_{DD\_INT\_EMAC\_DYN}$ = 10 mA (if EMAC is enabled)

Data Transmission Current

The data transmission current represents the power dissipated when moving data throughout the system via DMA. This current is proportional to the data rate. Refer to the power calculator available with "Estimating Power for ADSP-SC57x/2157x SHARC+ Processors" (EE-397) to estimate $I_{DD\_INT\_DMA\_DR\_DYN}$ based on the bandwidth of the data transfer.

DDR3 SDRAM Read Cycle Timing

Table 50 and Figure 17 show mobile DDR3 SDRAM read cycle timing, related to the DMC.

Table 50. DDR3 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.5 V

Parameter		450 MHz[1]		Unit
		Min	Max	
Timing Requirements				
t_{DQSQ}	DMC0_DQS to DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.15	ns
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	0.38		t_{CK}
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.3		t_{CK}

[1] To ensure proper operation of the DDR3, all the DDR3 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

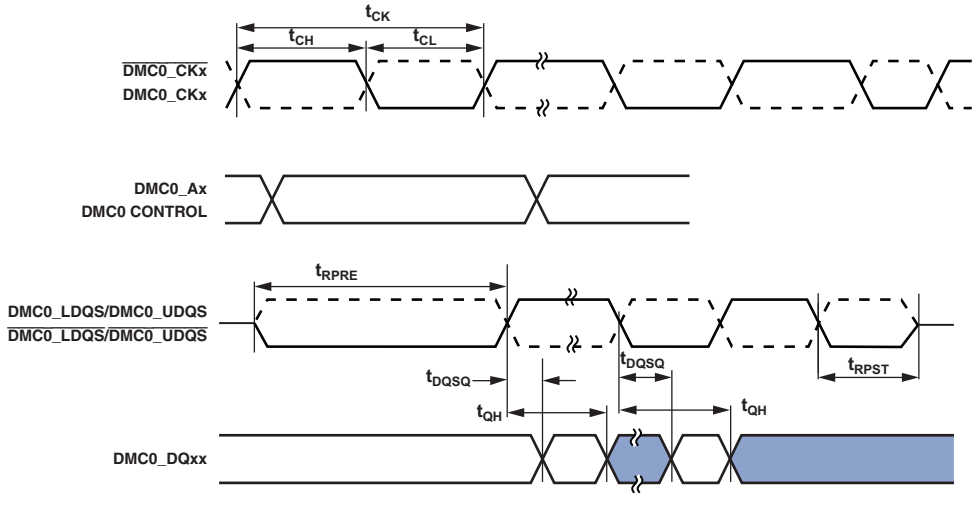


Figure 17. DDR3 SDRAM Controller Input AC Timing

DDR3 SDRAM Write Cycle Timing

Table 51 and Figure 18 show mobile DDR3 SDRAM output ac timing, related to the DMC.

Table 51. DDR3 SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.5 V

Parameter		450 MHz[1] Min	450 MHz[1] Max	Unit
Switching Characteristics				
t_{DQSS}	DMC0_DQS Latching Rising Transitions to Associated Clock Edges[2]	–0.25	+0.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay (Slew > 1 V/ns)	0.125		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.150		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.45	0.55	t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.45	0.55	t_{CK}
t_{WPRE}	Write Preamble	0.9		t_{CK}
t_{WPST}	Write Postamble	0.3		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.840		ns
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	0.550		ns

[1] To ensure proper operation of the DDR3, all the DDR3 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

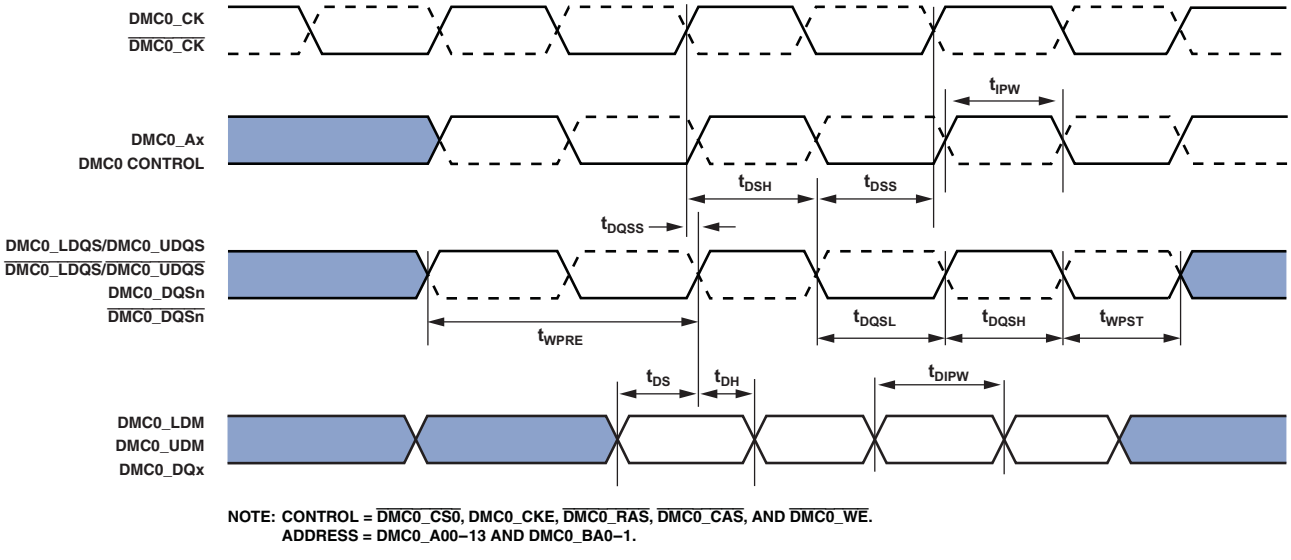


Figure 18. DDR3 SDRAM Controller Output AC Timing

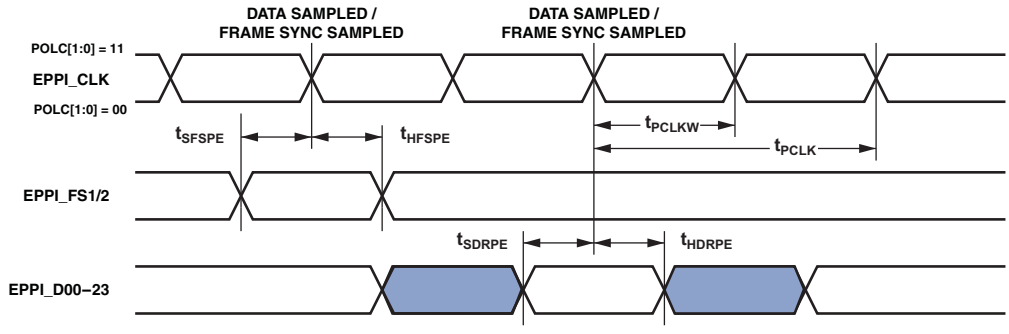


Figure 26. EPPI External Clock GP Receive Mode with External Frame Sync Timing

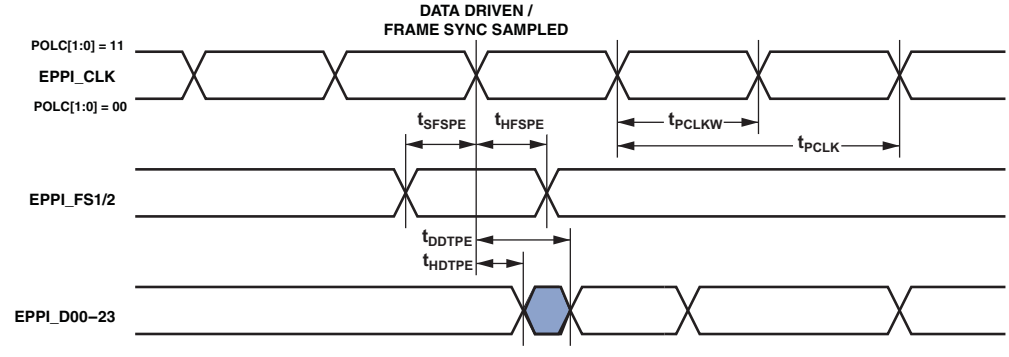


Figure 27. EPPI External Clock GP Transmit Mode with External Frame Sync Timing

Link Ports (LPs)

In LP receive mode, the LP clock is supplied externally and is called $f_{LCLKREXT}$, therefore the period can be represented by

$$t_{LCLKREXT} = \frac{1}{f_{LCLKREXT}}$$

In LP transmit mode, the programmed LP clock ($f_{LCLKTPROG}$) frequency in megahertz is set by the following equation where VALUE is a field in the LP_DIV register that can be set from 1 to 255:

$$f_{LCLKTPROG} = \frac{f_{SCLK0}}{(VALUE \times 2)}$$

In the case where VALUE = 0, $f_{LCLKTPROG} = f_{SCLK0}$. For all settings of VALUE, the following equation is true:

$$t_{LCLKTPROG} = \frac{1}{f_{LCLKTPROG}}$$

Calculation of the link receiver data setup and hold relative to the link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LPx_Dx and LPx_CLK. Setup skew is the maximum delay that can be introduced in LPx_Dx relative to LPx_CLK (setup skew = $t_{LCLKTWH}$ minimum − t_{DLDCH} − t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LPx_CLK relative to LPx_Dx (hold skew = $t_{LCLKTWL}$ minimum − t_{HLDCH} − t_{HLDCL}).

Table 54. LPs—Receive[1]

Parameter		Min	Max	Unit
Timing Requirements				
$f_{LCLKREXT}$	LPx_CLK Frequency		112.5	MHz
t_{SLDCL}	Data Setup Before LPx_CLK Low	0.9		ns
t_{HLDCL}	Data Hold After LPx_CLK Low	1.4		ns
t_{LCLKEW}	LPx_CLK Period[2]	$t_{LCLKREXT}$ − 0.8		ns
$t_{LCLKRWL}$	LPx_CLK Width Low[2]	0.5 × $t_{LCLKREXT}$		ns
$t_{LCLKRWH}$	LPx_CLK Width High[2]	0.5 × $t_{LCLKREXT}$		ns
Switching Characteristic				
t_{DLALC}	LPx_ACK Low Delay After LPx_CLK Low[3]	1.5 × t_{SCLK0} + 4	2.5 × t_{SCLK0} + 12	ns

[1] Specifications apply to LP0 and LP1.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external LPx_CLK. For the external LPx_CLK ideal maximum frequency, see the $f_{LCLKTEXT}$ specification in Table 27.
[3] LPx_ACK goes low with t_{DLALC} relative to rise of LPx_CLK after first byte, but does not go low if the link buffer of the receiver is not about to fill.

Asynchronous Sample Rate Converter (ASRC)—Serial Input Port

The ASRC input signals are routed from the DAI0_PINx pins using the SRU. Therefore, the timing specifications provided in Table 61 are valid at the DAI0_PINx pins.

Table 61. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$t_{SCLK0} - 1$		ns
t_{SRCCLK}	Clock Period	$2 \times t_{SCLK0}$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

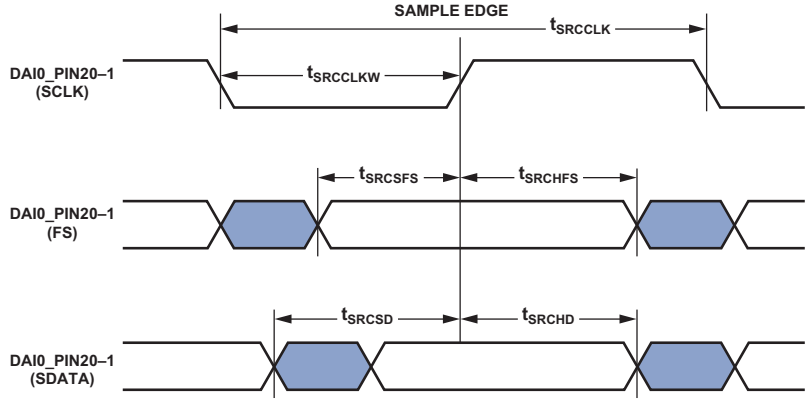


Figure 34. ASRC Serial Input Port Timing

SPI Port—SPIx_RDY Slave Timing

SPIx_RDY provides flow control. CPOL, CPHA, and FCCH are configuration bits in the SPIx_CTL register.

Table 67. SPI Port—SPIx_RDY Slave Timing[1]

Parameter	Conditions	Min	Max	Unit
Switching Characteristic				
$t_{DSPISCKRDYS}$ SPIx_RDY Deassertion from Last Valid Input SPIx_CLK Edge	FCCH = 0	$3 \times t_{SCLK1}$	$4 \times t_{SCLK1} + 10$	ns
	FCCH = 1	$4 \times t_{SCLK1}$	$5 \times t_{SCLK1} + 10$	ns

[1] All specifications apply to all three SPIs.

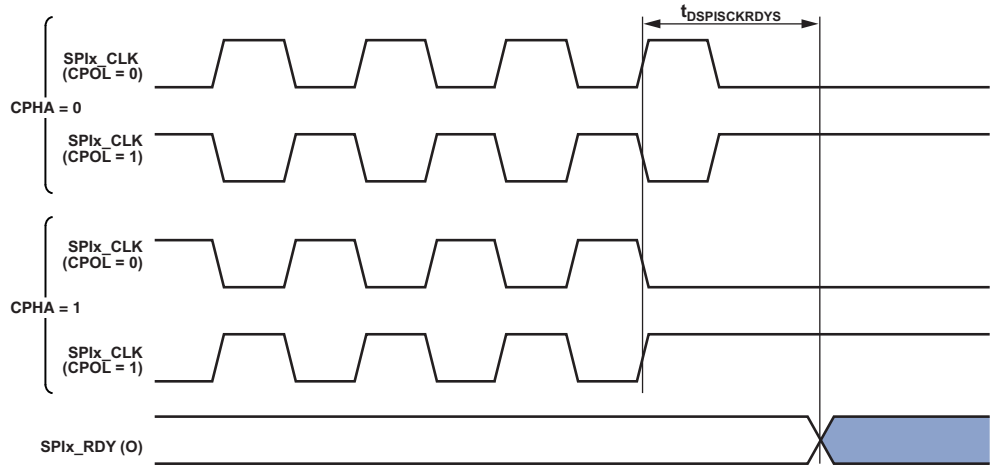
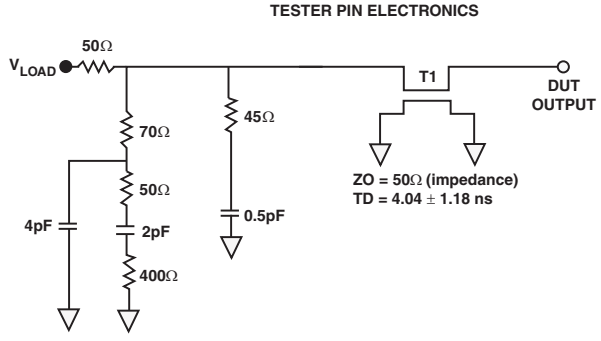


Figure 38. SPIx_RDY Deassertion from Valid Input SPIx_CLK Edge in Slave Mode



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, THE SYSTEM CAN INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 83. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

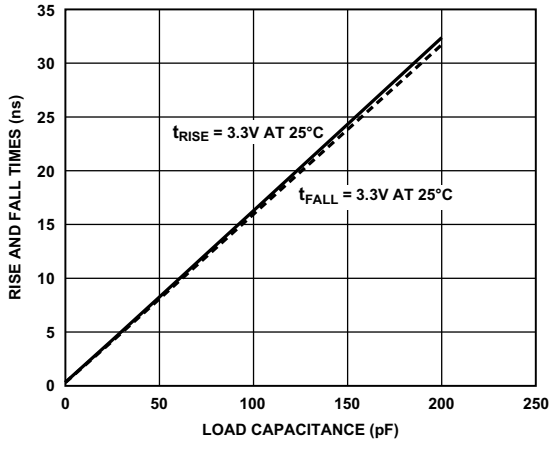


Figure 84. Driver Type A Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

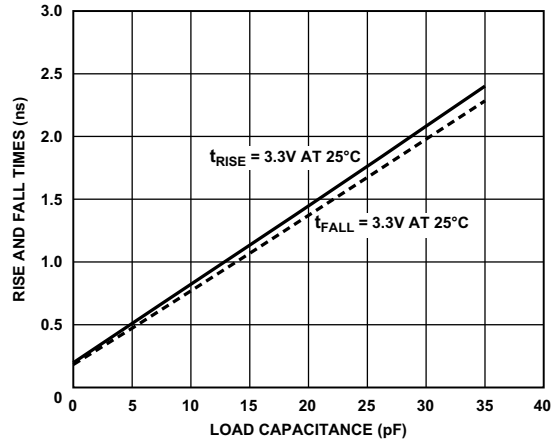


Figure 85. Driver Type H Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_EXT} = 3.3 V)

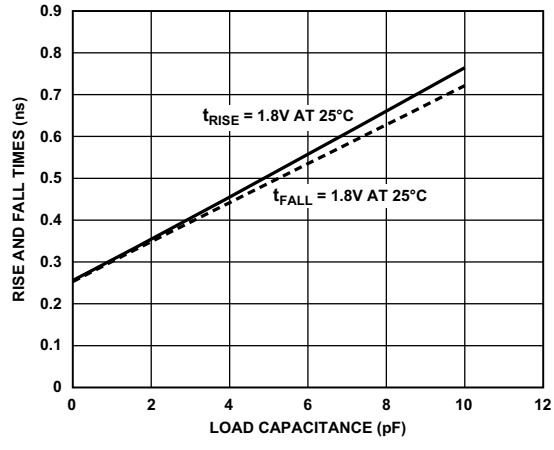


Figure 86. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for LPDDR

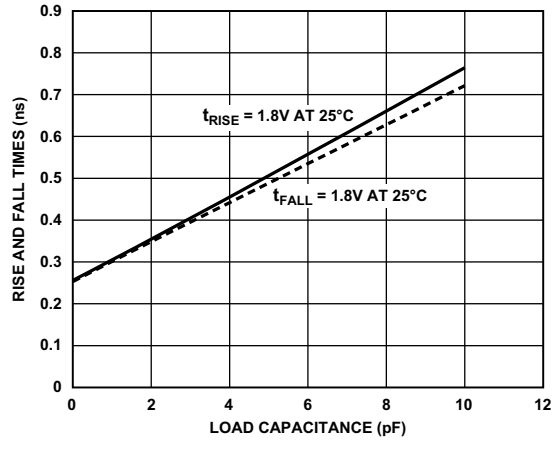


Figure 87. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.8 V) for DDR2

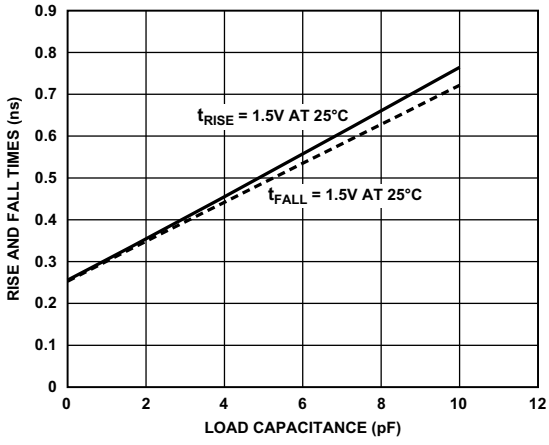


Figure 88. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.5 V) for DDR3

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application PCB, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J = junction temperature (°C).
T_{CASE} = case temperature (°C) measured at the top center of the package.
Ψ_{JT} = from Table 96 and Table 97.
P_D = power dissipation (see the Total Internal Power Dissipation section for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A = ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

In Table 96 and Table 97, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction to case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 6 layer PCB with 101.6 mm × 152.4 mm dimensions.

Table 96. Thermal Characteristics for 400 CSP_BGA

Parameter	Conditions	Typical	Unit
θ_{JA}	0 linear m/s air flow	14.24	°C/W
θ_{JA}	1 linear m/s air flow	12.61	°C/W
θ_{JA}	2 linear m/s air flow	12.09	°C/W
θ_{JC}		5.71	°C/W
Ψ_{JT}	0 linear m/s air flow	0.08	°C/W
Ψ_{JT}	1 linear m/s air flow	0.14	°C/W
Ψ_{JT}	2 linear m/s air flow	0.17	°C/W

Table 97. Thermal Characteristics for 176 LQFP_EP

Parameter	Conditions	Typical	Unit
θ_{JA}	0 linear m/s air flow	11.95	°C/W
θ_{JA}	1 linear m/s air flow	10.43	°C/W
θ_{JA}	2 linear m/s air flow	9.98	°C/W
θ_{JC}		11.10	°C/W
Ψ_{JT}	0 linear m/s air flow	0.15	°C/W
Ψ_{JT}	1 linear m/s air flow	0.24	°C/W
Ψ_{JT}	2 linear m/s air flow	0.29	°C/W

CONFIGURATION OF THE 176-LEAD LQFP LEAD CONFIGURATION

Figure 90 shows the top view of the 176-lead LQFP lead configuration and Figure 91 shows the bottom view of the 176-lead LQFP lead configuration.

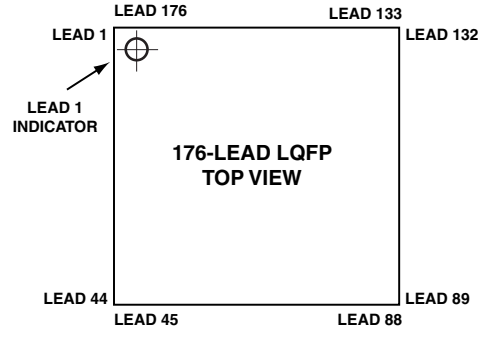


Figure 90. 176-Lead LQFP Lead Configuration (Top View)

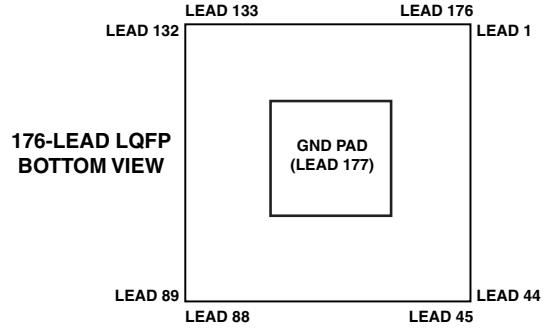


Figure 91. 176-Lead LQFP Lead Configuration (Bottom View)