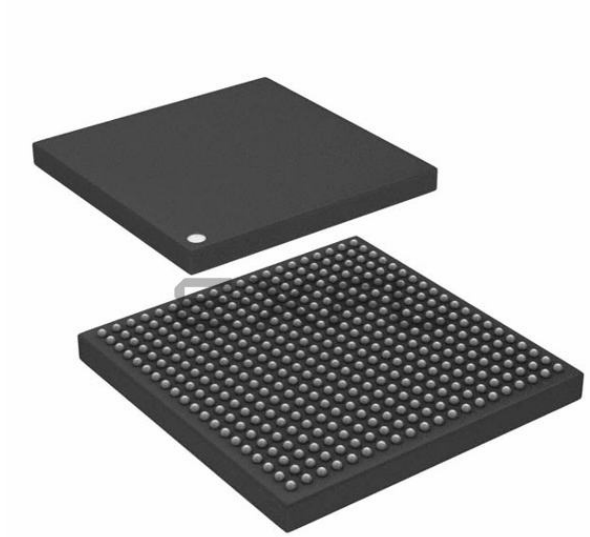

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz
Non-Volatile Memory	External
On-Chip RAM	1.768MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21573kbcz-4

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6/2018—Rev. A to Rev. B

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Generic Interrupt Controller (GIC), PL390 (ADSP-SC57x Only)

The generic interrupt controller (GIC) is a centralized resource for supporting and managing interrupts. The GIC splits into the distributor block (GICPORT0) and the central processing unit (CPU) interface block (GICPORT1).

Generic Interrupt Controller Port0 (GICPORT0)

The GICPORT0 distributor block performs interrupt prioritization and distribution to the GICPORT1 CPU interface blocks that connect to the processors in the system. It centralizes all interrupt sources, determines the priority of each interrupt, and forwards the interrupt with the highest priority to the interface, for priority masking and preemption handling.

Generic Interrupt Controller Port1 (GICPORT1)

The GICPORT1 CPU interface block performs priority masking and preemption handling for a connected processor in the system. GICPORT1 supports 8 software generated interrupts (SGIs) and 212 shared peripheral interrupts (SPIs).

L2 Cache Controller, PL310 (ADSP-SC57x Only)

The Level 2 (L2) cache controller, PL310 (see Figure 2), works efficiently with the ARM Cortex-A5 processors that implement system fabric. The cache controller directly interfaces on the data and instruction interface. The internal pipelining of the cache controller is optimized to enable the processors to operate at the same clock frequency. The cache controller supports the following:

- Two read/write 64-bit slave ports, one connected to the ARM Cortex-A5 instruction and data interfaces, and one connecting the ARM Cortex-A5 and SHARC+ cores for data coherency.
- Two read/write 64-bit master ports for interfacing with the system fabric.

SHARC PROCESSOR

Figure 3 shows the SHARC processor integrates a SHARC+ SIMD core, L1 memory crossbar, I/D cache controller, L1 memory blocks, and the master/slave ports. Figure 4 shows the SHARC+ SIMD core block diagram.

The SHARC processor supports a modified Harvard architecture in combination with a hierarchical memory structure. L1 memories typically operate at the full processor speed with little or no latency.

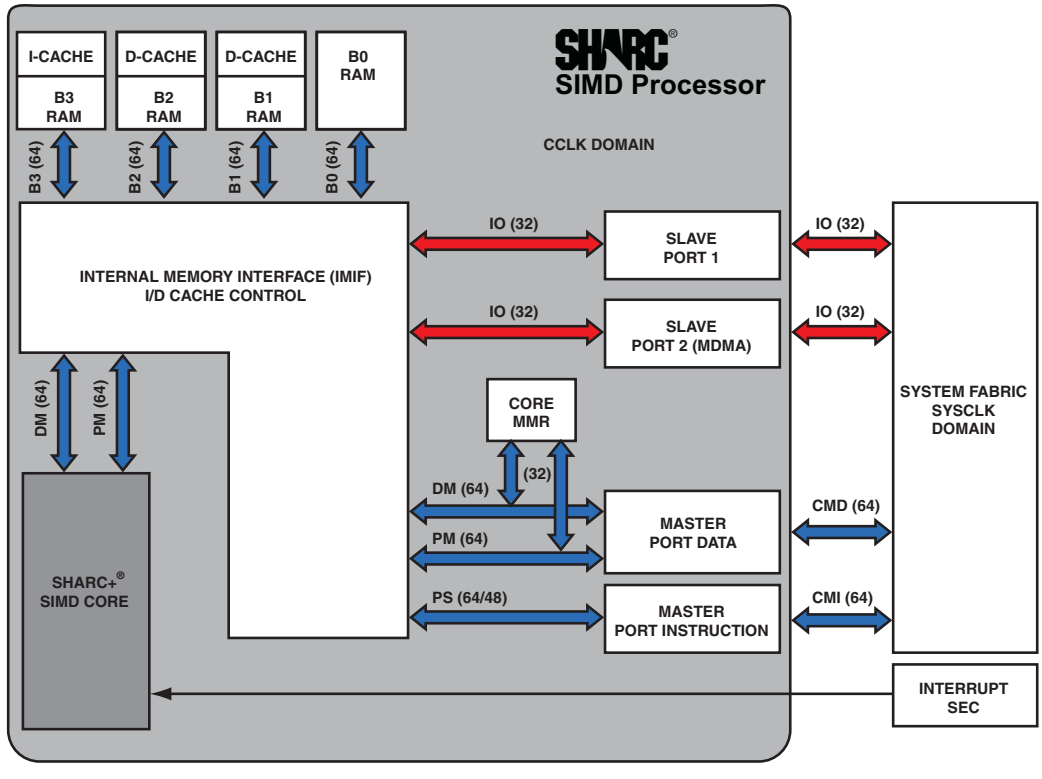


Figure 3. SHARC Processor Block Diagram

Table 10. Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DD_INT}
DDR3/DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
HADC/TMU	V_{DD_HADC}
All other I/O (includes SYS, JTAG, and ports pins)	V_{DD_EXT}

The power dissipated by a processor is largely a function of the clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

Target Board JTAG Emulator Connector

The Analog Devices DSP tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. The Analog Devices DSP tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor JTAG interface ensures the emulator does not affect target system loading or timing.

For information on JTAG emulator operation, see the appropriate emulator hardware user's guide at SHARC Processors Software and Tools.

SYSTEM DEBUG

The processors include various features that allow easy system debug. These are described in the following sections.

System Watchpoint Unit (SWU)

The system watchpoint unit (SWU) is a single module that connects to a single system bus and provides transaction monitoring. One SWU is attached to the bus going to each system slave. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently but share common event (for example, interrupt and trigger) outputs.

Debug Access Port (DAP)

Debug access port (DAP) provides IEEE 1149.1 JTAG interface support through the JTAG debug. The DAP provides an optional instrumentation trace for both the core and system. It provides a trace stream that conforms to *MIPI System Trace Protocol version 2 (STPv2)*.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including an integrated development environment (CrossCore® Embedded Studio), evaluation products, emulators, and a variety of software add ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers the CrossCore Embedded Studio integrated development environment (IDE).

CrossCore Embedded Studio is based on the Eclipse framework. Supporting most Analog Devices processor families, it is the IDE of choice for processors, including multicore devices.

CrossCore Embedded Studio seamlessly integrates available software add ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information, visit www.analog.com/cces.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides a wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Various EZ-Extenders® are also available, which are daughter cards that deliver additional specialized functionality, including audio and video processing. For more information visit www.analog.com.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in circuit. This permits users to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in circuit programming of the on-board Flash® device to store user specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add Ins for CrossCore Embedded Studio

Analog Devices offers software add ins which seamlessly integrate with CrossCore Embedded Studio to extend the capabilities and reduce development time. Add ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add ins are viewable through the CrossCore Embedded Studio IDE once the add in is installed.

400-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor pin definitions are shown in Table 12 for the 400-ball CSP_BGA package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a GPIO port pin.
- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a GPIO pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the Digital Audio Interface (DAI) chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for complete information on the use of the DAI and SRUs.

Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
ACM0_A0	ACM0 ADC Control Signals	F	PF_11
ACM0_A1	ACM0 ADC Control Signals	C	PC_14
ACM0_A2	ACM0 ADC Control Signals	C	PC_15
ACM0_A3	ACM0 ADC Control Signals	A	PA_14
ACM0_A4	ACM0 ADC Control Signals	B	PB_01
ACM0_T0	ACM0 External Trigger n	A	PA_15
C1_FLG0	SHARC Core 1 Flag Pin	E	PE_13
C1_FLG1	SHARC Core 1 Flag Pin	E	PE_01
C1_FLG2	SHARC Core 1 Flag Pin	F	PF_04
C1_FLG3	SHARC Core 1 Flag Pin	D	PD_06
C2_FLG0	SHARC Core 2 Flag Pin	B	PB_00
C2_FLG1	SHARC Core 2 Flag Pin	C	PC_14
C2_FLG2	SHARC Core 2 Flag Pin	F	PF_11
C2_FLG3	SHARC Core 2 Flag Pin	E	PE_15
CAN0_RX	CAN0 Receive	C	PC_12
CAN0_TX	CAN0 Transmit	C	PC_13
CAN1_RX	CAN1 Receive	C	PC_14
CAN1_TX	CAN1 Transmit	C	PC_15
CNT0_DG	CNT0 Count Down and Gate	D	PD_08
CNT0_UD	CNT0 Count Up and Direction	E	PE_13
CNT0_ZM	CNT0 Count Zero Marker	D	PD_07
DAI0_PIN01	DAI0 Pin 1	Not Muxed	DAI0_PIN01
DAI0_PIN02	DAI0 Pin 2	Not Muxed	DAI0_PIN02
DAI0_PIN03	DAI0 Pin 3	Not Muxed	DAI0_PIN03
DAI0_PIN04	DAI0 Pin 4	Not Muxed	DAI0_PIN04
DAI0_PIN05	DAI0 Pin 5	Not Muxed	DAI0_PIN05
DAI0_PIN06	DAI0 Pin 6	Not Muxed	DAI0_PIN06
DAI0_PIN07	DAI0 Pin 7	Not Muxed	DAI0_PIN07
DAI0_PIN08	DAI0 Pin 8	Not Muxed	DAI0_PIN08
DAI0_PIN09	DAI0 Pin 9	Not Muxed	DAI0_PIN09
DAI0_PIN10	DAI0 Pin 10	Not Muxed	DAI0_PIN10
DAI0_PIN11	DAI0 Pin 11	Not Muxed	DAI0_PIN11
DAI0_PIN12	DAI0 Pin 12	Not Muxed	DAI0_PIN12
DAI0_PIN13	DAI0 Pin 13	Not Muxed	DAI0_PIN13
DAI0_PIN14	DAI0 Pin 14	Not Muxed	DAI0_PIN14
DAI0_PIN15	DAI0 Pin 15	Not Muxed	DAI0_PIN15

Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TRACE0_D03	TRACE0 Trace Data 3	F	PF_03
TRACE0_D04	TRACE0 Trace Data 4	D	PD_10
TRACE0_D05	TRACE0 Trace Data 5	D	PD_11
TRACE0_D06	TRACE0 Trace Data 6	D	PD_12
TRACE0_D07	TRACE0 Trace Data 7	D	PD_13
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
TWI1_SCL	TWI1 Serial Clock	Not Muxed	TWI1_SCL
TWI1_SDA	TWI1 Serial Data	Not Muxed	TWI1_SDA
TWI2_SCL	TWI2 Serial Clock	Not Muxed	TWI2_SCL
TWI2_SDA	TWI2 Serial Data	Not Muxed	TWI2_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	D	PD_06
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	D	PD_05
$\overline{\text{UART0\_RX}}$	UART0 Receive	F	PF_09
$\overline{\text{UART0\_TX}}$	UART0 Transmit	F	PF_08
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	E	PE_14
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	E	PE_00
$\overline{\text{UART1\_RX}}$	UART1 Receive	F	PF_11
$\overline{\text{UART1\_TX}}$	UART1 Transmit	F	PF_10
$\overline{\text{UART2\_CTS}}$	UART2 Clear to Send	A	PA_11
$\overline{\text{UART2\_RTS}}$	UART2 Request to Send	A	PA_10
$\overline{\text{UART2\_RX}}$	UART2 Receive	C	PC_13
$\overline{\text{UART2\_TX}}$	UART2 Transmit	C	PC_12
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB_CLKIN
USB0_DM	USB0 Data –	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB_XTAL
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT
VDD_INT	Internal Voltage Domain	Not Muxed	VDD_INT
VDD_DMC	DMC VDD	Not Muxed	VDD_DMC
VDD_HADC	HADC/TMU VDD	Not Muxed	VDD_HADC
VDD_USB	USB VDD	Not Muxed	VDD_USB

[1] Signal is routed to the DAI0_PINnn pin through the DAI0_PBnn pin buffers using the SRU.

GPIO MULTIPLEXING FOR 176-LEAD LQFP PACKAGE

Table 21 through Table 24 identify the pin functions that are multiplexed on the GPIO pins of the 176-lead LQFP package.

Table 21. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	TRACE0_CLK				TM0_ACLK1
PA_01	TRACE0_D00				
PA_02	TRACE0_D01				
PA_03	TRACE0_D02				
PA_04	TRACE0_D03				
PA_05	UART0_TX				
PA_06	UART0_RX				TM0_ACI0
PA_07	UART1_TX	SPI2_SEL2			
PA_08	UART1_RX	ACM0_A0	SPI1_SEL3		TM0_ACI1
PA_09	ETH0_PTPPPS0	LP1_D6	SPI0_SEL4		
PA_10	ETH0_MDIO	UART2_RTS	SPI2_SEL6		
PA_11	ETH0_MDC	UART2_CTS			
PA_12	ETH0_RXD1				
PA_13	ETH0_RXD0				
PA_14	ETH0_RXD2	ACM0_A3	SPI1_SEL4		
PA_15	ETH0_RXD3	ACM0_T0	SPI2_SEL5		

Table 22. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	ETH0_RXCLK_REFCLK	C2_FLG0			
PB_01	ETH0_CRS	ACM0_A4	LP1_ACK	TM0_TMR3	
PB_02	ETH0_RXCTL_RXDV		SPI1_SEL5		
PB_03	ETH0_RXERR	MLB0_CLKOUT	LP1_CLK	TM0_TMR4	
PB_04	ETH0_TXCLK	MLB0_DAT			
PB_05	ETH0_TXD3	MLB0_SIG			
PB_06	ETH0_TXD2	MLB0_CLK			
PB_07	ETH0_TXD0		SPI2_SEL7		
PB_08	ETH0_TXD1				
PB_09	ETH0_TXCTL_TXEN				
PB_10	SPI2_MISO				
PB_11	SPI2_MOSI				
PB_12	SPI2_D2				
PB_13	SPI2_D3				
PB_14	SPI2_CLK				
PB_15	SPI2_SEL1				SPI2_SS

ADSP-SC57x/ADSP-2157x DESIGNER QUICK REFERENCE

Table 25 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The type column identifies the I/O type or supply type of the pin. The abbreviations used in this column are analog (a), supply (s), ground (g) and Input, Output, and InOut.
- The driver type column identifies the driver type used by the corresponding pin. The driver types are defined in the Output Drive Currents section of this data sheet.
- The internal termination column specifies the termination present after the processor is powered up (both during reset and after reset).
- The reset drive column specifies the active drive on the signal when the processor is in the reset state.
- The power domain column specifies the power supply domain in which the signal resides.
- The description and notes column identifies any special requirements or characteristics for a signal. These recommendations apply whether or not the hardware block associated with the signal is featured on the product. If no special requirements are listed, the signal can be left unconnected if it is not used. For multiplexed GPIO pins, this column identifies the functions available on the pin.

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
DAI0_PIN01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 1 Notes: See note[2]
DAI0_PIN02	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 2 Notes: See note[2]
DAI0_PIN03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 3 Notes: See note[2]
DAI0_PIN04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 4 Notes: See note[2]
DAI0_PIN05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 5 Notes: See note[2]
DAI0_PIN06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 6 Notes: See note[2]
DAI0_PIN07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 7 Notes: See note[2]
DAI0_PIN08	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 8 Notes: See note[2]
DAI0_PIN09	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 9 Notes: See note[2]
DAI0_PIN10	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 10 Notes: See note[2]
DAI0_PIN11	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 11 Notes: See note[2]
DAI0_PIN12	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 12 Notes: See note[2]
DAI0_PIN13	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 13 Notes: See note[2]
DAI0_PIN14	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 14 Notes: See note[2]
DAI0_PIN15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 15 Notes: See note[2]

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
$\overline{\text{DMC0\_CAS}}$	Output	B	none	L	VDD_DMC	Desc: DMC0 Column Address Strobe Notes: No notes
DMC0_CK	Output	C	none	L	VDD_DMC	Desc: DMC0 Clock Notes: No notes
DMC0_CKE	Output	B	none	L	VDD_DMC	Desc: DMC0 Clock enable Notes: No notes
$\overline{\text{DMC0\_CK}}$	Output	C	none	L	VDD_DMC	Desc: DMC0 Clock (complement) Notes: No notes
$\overline{\text{DMC0\_CS0}}$	Output	B	none	L	VDD_DMC	Desc: DMC0 Chip Select 0 Notes: No notes
DMC0_DQ00	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 0 Notes: No notes
DMC0_DQ01	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 1 Notes: No notes
DMC0_DQ02	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 2 Notes: No notes
DMC0_DQ03	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 3 Notes: No notes
DMC0_DQ04	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 4 Notes: No notes
DMC0_DQ05	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 5 Notes: No notes
DMC0_DQ06	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 6 Notes: No notes
DMC0_DQ07	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 7 Notes: No notes
DMC0_DQ08	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 8 Notes: No notes
DMC0_DQ09	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 9 Notes: No notes
DMC0_DQ10	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 10 Notes: No notes
DMC0_DQ11	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 11 Notes: No notes
DMC0_DQ12	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 12 Notes: No notes
DMC0_DQ13	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 13 Notes: No notes
DMC0_DQ14	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 14 Notes: No notes
DMC0_DQ15	InOut	B	none	none	VDD_DMC	Desc: DMC0 Data 15 Notes: No notes
DMC0_LDM	Output	B	none	L	VDD_DMC	Desc: DMC0 Data Mask for Lower Byte Notes: No notes
DMC0_LDQS	InOut	C	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte Notes: External weak pull-down required in LPDDR mode

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
SYS_CLKIN1	a	NA	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: Connect to GND if not used
SYS_CLKOUT	a	H	none	High-Z when $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ are both active[5]	VDD_EXT	Desc: Processor Clock Output Notes: No notes
SYS_FAULT	InOut	A	none	none	VDD_EXT	Desc: Active-High Fault Output Notes: Pull down if not used
$\overline{\text{SYS\_FAULT}}$	InOut	A	none	none	VDD_EXT	Desc: Active-Low Fault Output Notes: Pull up if not used
$\overline{\text{SYS\_HWRST}}$	Input	NA	none	none	VDD_EXT	Desc: Processor Hardware Reset Control Notes: No connection not allowed
$\overline{\text{SYS\_RESOUT}}$	Output	A	none	High-Z when $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ are both active[5]	VDD_EXT	Desc: Reset Output Notes: No notes
SYS_XTAL0	a	NA	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
SYS_XTAL1	a	NA	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
TWI0_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI0_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
TWI1_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI1 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI1_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI1 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
TWI2_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI2 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI2_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI2 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
USB0_DM	InOut	F	none	none	VDD_USB	Desc: USB0 Data– Notes: Add external pull-down if not used[6]
USB0_DP	InOut	F	none	none	VDD_USB	Desc: USB0 Data + Notes: Add external pull-down if not used[6]
USB0_ID	InOut		none	none	VDD_USB	Desc: USB0 OTG ID Notes: Connect to GND when USB is not used[6]

HADC

HADC Electrical Characteristics

Table 34. HADC Electrical Characteristics

Parameter	Conditions	Typ	Unit
$I_{DD\_HADC\_IDLE}$	Current consumption on V_{DD_HADC} HADC is powered on, but not converting	2.0	mA
$I_{DD\_HADC\_ACTIVE}$	Current consumption on V_{DD_HADC} during a conversion	2.5	mA
$I_{DD\_HADC\_POWERDOWN}$	Current consumption on V_{DD_HADC} Analog circuitry of the HADC is powered down	60	µA

HADC DC Accuracy

Table 35. HADC DC Accuracy for CSP_BGA[1]

Parameter	Typ	Unit[2]
Resolution	9	Bits
No Missing Codes (NMC) – Unrestricted	9	Bits
No Missing Codes (NMC) – Pin Restrictions[3]	10	Bits
Integral Nonlinearity (INL)	±2	LSB
Differential Nonlinearity (DNL)	±2	LSB
Offset Error	±5	LSB
Offset Error Matching	±6	LSB
Gain Error	±4	LSB
Gain Error Matching	±4	LSB

[1] See the Operating Conditions section for the HADC0_VINx specification.
[2] LSB = HADC0_VREFP ÷ 512.
[3] Pin restrictions required: pins DAI18, DAI19, and DAI20 must be programmed to inputs and a static (non-switching) signal applied to the pins.

Table 36. HADC DC Accuracy for LQFP_EP[1]

Parameter	Typ	Unit[2]
Resolution	7	Bits
No Missing Codes (NMC) – Unrestricted	7	Bits
No Missing Codes (NMC) – Pin Restrictions[3]	9	Bits
Integral Nonlinearity (INL)	±2	LSB
Differential Nonlinearity (DNL)	±2	LSB
Offset Error	±5	LSB
Offset Error Matching	±6	LSB
Gain Error	±4	LSB
Gain Error Matching	±4	LSB

[1] See the Operating Conditions section for the HADC0_VINx specification.
[2] LSB = HADC0_VREFP ÷ 128.
[3] Pin restrictions required: pins DAI18, DAI19, and DAI20 must be programmed to inputs and a static (non-switching) signal applied to the pins.

HADC Timing Specifications

Table 37. HADC Timing Specifications

Parameter	Typ	Max	Unit
Conversion Time[1]	20 × T_{SAMPLE}		µs
Throughput Range		1	MSPS
T_{WAKEUP}		100	µs

[1] Refer to the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for additional information about T_{SAMPLE}.

TMU

TMU Characteristics

Table 38. TMU Characteristics

Parameter	Typ	Unit
Resolution	1	°C
Accuracy	±8	°C

Table 39. TMU Gain and Offset

Junction Temperature Range	TMU_GAIN	TMU_OFFSET
–40°C to +40°C	Contact Analog Devices, Inc.	
40°C to 85°C	Contact Analog Devices, Inc.	
85°C to 133°C	Contact Analog Devices, Inc.	

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 40 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 40. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.33 V to +1.26 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to +3.60 V
DDR2/LPDDR Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.90 V
DDR3 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.60 V
DDR2 Reference Voltage (V_{DDR_VREF})	–0.33 V to +1.90 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to +3.60 V
HADC Supply Voltage (V_{DD_HADC})	–0.33 V to +3.60 V
HADC Reference Voltage (V_{HADC_REF})	–0.33 V to +3.60 V
DDR2/LPDDR Input Voltage[1]	–0.33 V to +1.90 V
DDR3 Input Voltage[1]	–0.33 V to +1.60 V
Digital Input Voltage[1, 2]	–0.33 V to +3.60 V
TWI Input Voltage[1, 3]	–0.33 V to +5.50 V
USB0_Dx Input Voltage[1, 4]	–0.33 V to +5.25 V
USB0_VBUS Input Voltage[1, 4]	–0.33 V to +6 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} +0.5 V
Analog Input Voltage[5]	–0.2 V to V_{DD_HADC} +0.2 V
I_{OH}/I_{OL} Current per Signal[2]	6 mA (maximum)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	133°C

[1] Applies only when the related power supply (V_{DD_DMC}, V_{DD_EXT}, or V_{DD_USB}) is within specification. When the power supply is below specification, the range is the voltage being applied to that power domain ± 0.2 V.

[2] Applies to 100% transient duty cycle.

[3] Applies to TWI_SCL and TWI_SDA.

[4] If the USB is not used, connect these pins according to Table 25.

[5] Applies only when V_{DD_HADC} is within specifications and ≤ 3.4 V. When V_{DD_HADC} is within specifications and > 3.4 V, the maximum rating is 3.6 V. When V_{DD_HADC} is below specifications, the range is V_{DD_HADC} ± 0.2 V.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Power-Up Reset Timing

Table 41 and Figure 8 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU).

In Figure 8, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, and V_{DD_HADC}.

Table 41. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{SYS\_HWRST}$ Deasserted after $V_{DD\_SUPPLIES}$ (V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}) and SYS_CLKINx are Stable and within Specification	$11 \times t_{CKIN}$		ns

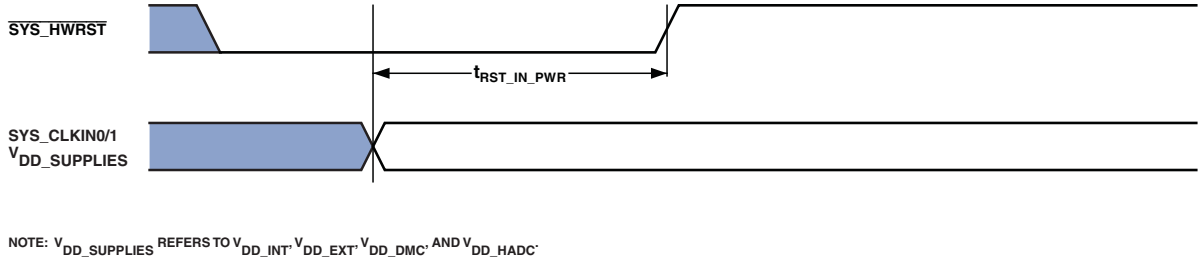


Figure 8. Power-Up Reset Timing

DDR2 SDRAM Clock and Control Cycle Timing

Table 43 and Figure 10 show DDR2 SDRAM clock and control cycle timing, related to the DMC.

Table 43. DDR2 SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		400 MHz[1] Min	400 MHz[1] Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.5		ns
$t_{CH(abs)}$[2]	Minimum Clock Pulse Width	0.48	0.52	t_{CK}
$t_{CL(abs)}$[2]	Maximum Clock Pulse Width	0.48	0.52	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	175		ps
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	250		ps

[1] To ensure proper operation of DDR2, all the DDR2 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[2] As per JESD79-2E definition.

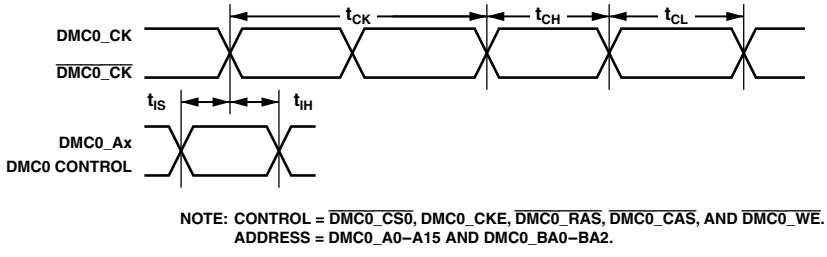


Figure 10. DDR2 SDRAM Clock and Control Cycle Timing

Mobile DDR SDRAM Write Cycle Timing

Table 48 and Figure 15 show mobile DDR SDRAM write cycle timing, related to the DMC.

Table 48. Mobile DDR SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1]		Unit
		Min	Max	
Switching Characteristics				
t_{DQSS}[2]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	0.75	1.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay (Slew > 1 V/ns)	0.48		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.48		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.4		t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.4		t_{CK}
t_{WPRE}	Write Preamble	0.25		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	2.3		ns
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	1.8		ns

[1] To ensure proper operation of LPDDR, all the LPDDR requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

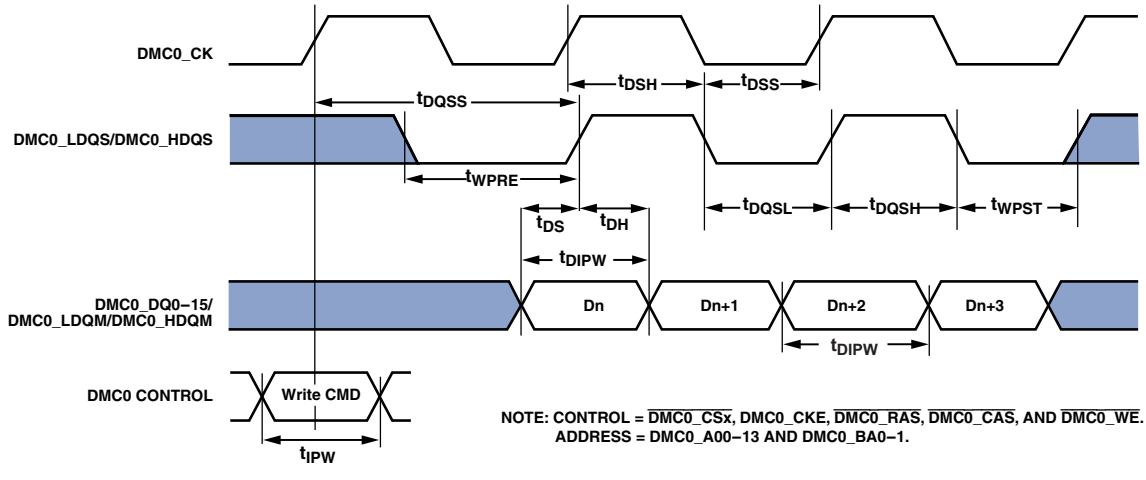
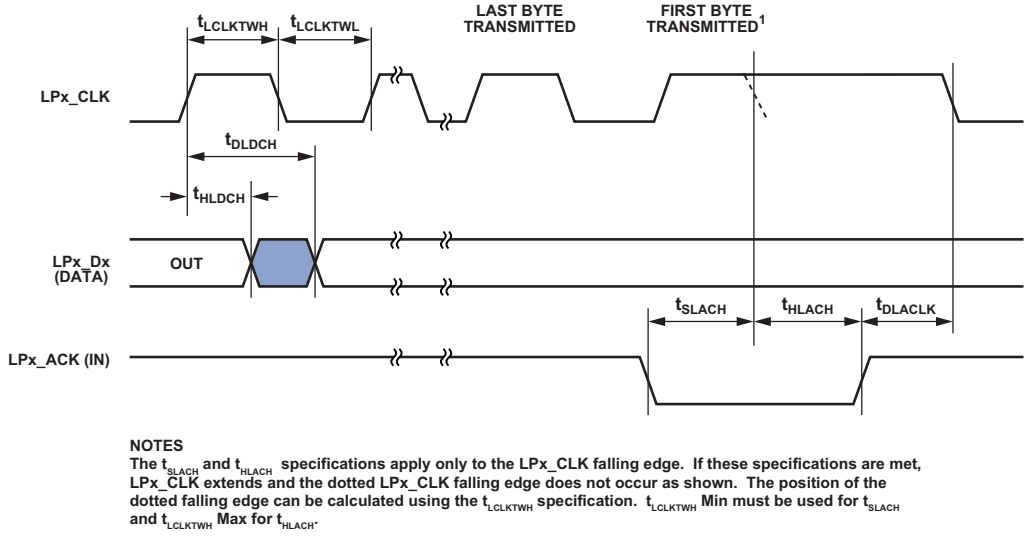


Figure 15. Mobile DDR SDRAM Controller Output AC Timing

Table 55. LPs—Transmit[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LPx_ACK Setup Before LPx_CLK Low	$2 \times t_{SCLK0} + 13.5$		ns
t_{HLACH}	LPx_ACK Hold After LPx_CLK Low	–5.5		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LPx_CLK High		2.23	ns
t_{HLDCH}	Data Hold After LPx_CLK High	–2.3		ns
$t_{LCLKTWL}$[2]	LPx_CLK Width Low	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	ns
$t_{LCLKTWH}$[2]	LPx_CLK Width High	$0.4 \times t_{LCLKTPROG}$	$0.6 \times t_{LCLKTPROG}$	ns
t_{LCLKTW}[2]	LPx_CLK Period	$N \times t_{LCLKTPROG} - 0.6$		ns
t_{DLACLK}	LPx_CLK Low Delay After LPx_ACK High	$t_{SCLK0} + 4$	$2 \times t_{SCLK0} + 1 \times t_{LPCLK} + 10$	ns

[1] Specifications apply to LP0 and LP1.
[2] See Table 27 for details on the minimum period that can be programmed for $t_{LCLKTPROG}$.



NOTES
The t_{SLACH} and t_{HLACH} specifications apply only to the LPx_CLK falling edge. If these specifications are met, LPx_CLK extends and the dotted LPx_CLK falling edge does not occur as shown. The position of the dotted falling edge can be calculated using the $t_{LCLKTWH}$ specification. $t_{LCLKTWH}$ Min must be used for t_{SLACH} and $t_{LCLKTWH}$ Max for t_{HLACH}.

Figure 29. LPs—Transmit

Table 83. 10/100/1000 EMAC Timing—RMII and RGMII Station Management

Parameter[1]		Min	Max	Unit
Timing Requirements				
t_{MDIOS}	ETH0_MDIO Input Valid to ETH0_MDC Rising Edge (Setup)	12.6		ns
t_{MDCIH}	ETH0_MDC Rising Edge to ETH0_MDIO Input Invalid (Hold)	0		ns
Switching Characteristics				
t_{MDCOV}	ETH0_MDC Falling Edge to ETH0_MDIO Output Valid		t_{SCLK0} + 2	ns
t_{MDCOH}	ETH0_MDC Falling Edge to ETH0_MDIO Output Invalid (Hold)	t_{SCLK0} –2.9		ns

[1] ETH0_MDC/ETH0_MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. ETH0_MDC is an output clock with a minimum period that is programmable as a multiple of the system clock SCLK0. ETH0_MDIO is a bidirectional data line.

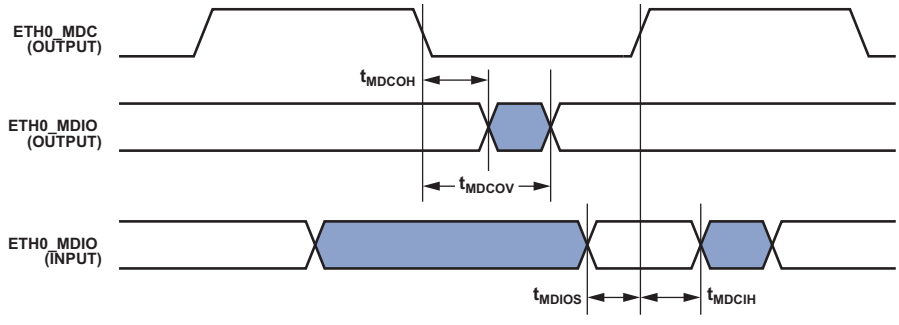


Figure 53. 10/100 /1000 Ethernet MAC Controller Timing—RMII and RGMII Station Management

10/100/1000 EMAC Timing

Table 84 and Figure 54 describe the RGMII EMAC timing.

Table 84. 10/100/1000 EMAC Timing—RGMII Receive and Transmit Signals

Parameter		Min	Max	Unit
Timing Requirements				
t_{SETUPR}	Data to Clock Input Setup at Receiver	1		ns
t_{HOLDR}	Data to Clock Input Hold at Receiver	1		ns
$t_{GREFCLKF}$	RGMII Receive Clock Period	8		ns
$t_{GREFCLKW}$	RGMII Receive Clock Pulse Width	4		ns
Switching Characteristics				
t_{SKEWT}	Data to Clock Output Skew at Transmitter	–0.5	+0.5	ns
t_{CYC}	Clock Cycle Duration	7.2	8.8	ns
t_{DUTY_G}	Duty Cycle for RGMII Minimum	$t_{GREFCLKF} \times 45\%$	$t_{GREFCLKF} \times 55\%$	ns

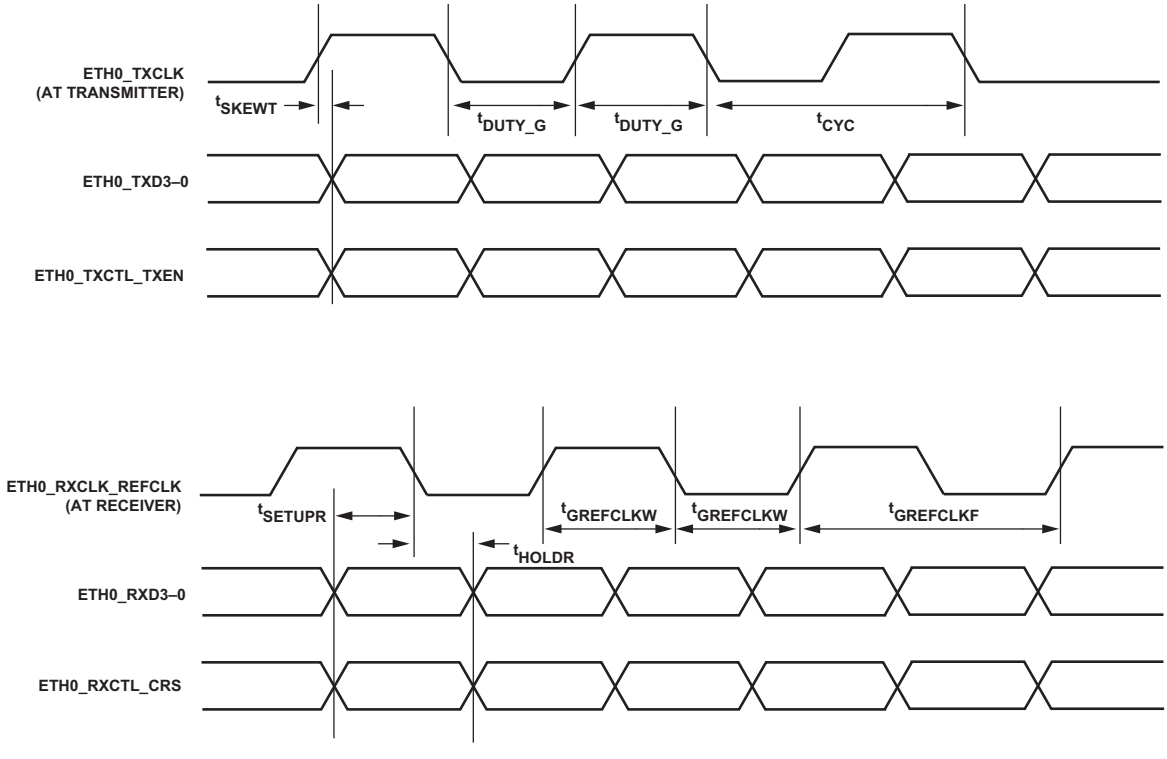


Figure 54. EMAC Timing—RGMII

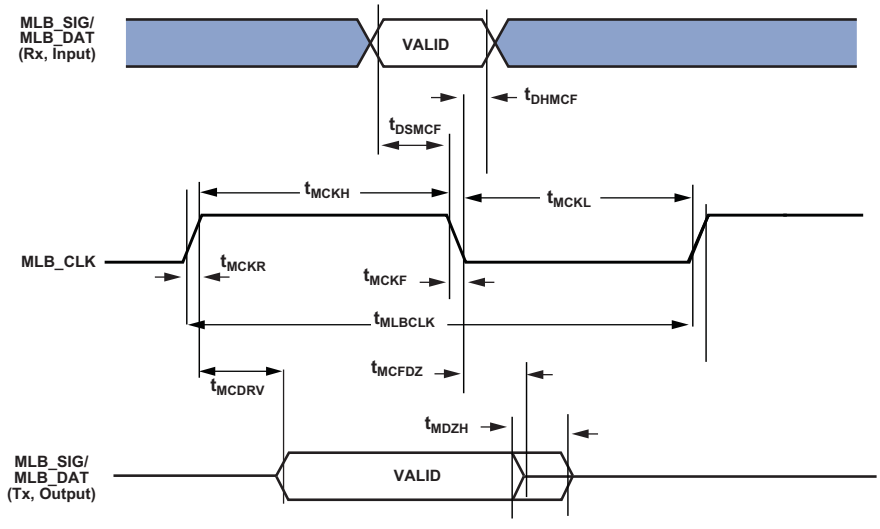


Figure 60. MLB Timing (3-Pin Interface)

The ac timing specifications of the 6-pin MLB interface is detailed in Table 92. Refer to the *Media Local Bus Specification version 4.2* for more details.

Table 92. 6-Pin MLB Interface Specifications

Parameter		Conditions	Min	Typ	Max	Unit
t_{MT}	Differential Transition Time at the Input Pin (See Figure 61)	20% to 80% $V_{IN}+/V_{IN}-$ 80% to 20% $V_{IN}+/V_{IN}-$			1	ns
f_{MCKE}	MLBCP/N External Clock Operating Frequency (See Figure 62)[1]	2048 × FS at 44.0 kHz	90.112			MHz
		2048 × FS at 50.0 kHz			102.4	MHz
f_{MCKR}	Recovered Clock Operating Frequency (Internal, Not Observable at Pins, Only for Timing References) (See Figure 62)	2048 × FS at 44.0 kHz	90.112			MHz
		2048 × FS at 50.0 kHz			102.4	MHz
t_{DELAY}	Transmitter MLBSP/N (MLBDP/N) Output Valid From Transition of MLBCP/N (Low to High) (See Figure 63)	f_{MCKR} = 2048 × FS	0.6		5	ns
t_{PHZ}	Disable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 64)	f_{MCKR} = 2048 × FS	0.6		7	ns
t_{PLZ}	Enable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 64)	f_{MCKR} = 2048 × FS	0.6		11.2	ns
t_{SU}	MLBSP/N (MLBDP/N) Valid to Transition of MLBCP/N (Low to High) (See Figure 63)	f_{MCKR} = 2048 × FS	1			ns
t_{HD}	MLBSP/N (MLBDP/N) Hold From Transition of MLBCP/N (Low to High) (See Figure 63)[2]		0.6			ns

[1] f_{MCKE} (maximum) and f_{MCKR} (maximum) include maximum cycle to cycle system jitter (t_{JITTER}) of 600 ps for a bit error rate of 10E-9.
[2] Receivers must latch MLBSP/N (MLBDP/N) data within t_{HD} (minimum) of the rising edge of MLBCP/N.

Lead No.	Pin Name
161	PB_08
162	PB_07
163	VDD_INT
164	VDD_EXT
165	PB_06
166	PB_05
167	VDD_EXT
168	PB_04
169	PB_03
170	VDD_INT
171	VDD_EXT
172	PB_02
173	PB_01
174	PB_00
175	VDD_INT
176	GND
177[1]	GND

[1] Pin177 is the GND supply (see Figure 91) for the processor; this pad must connect to GND.

AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 99 are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 99. Automotive Products

Model [1, 2, 3]	Processor Instruction Rate (Max)	ARM Instruction Rate (Max)[4]	Temperature Range[5]	ARM Cores[4]	SHARC+ Cores	External Memory Ports	Package Description	Package Option
AD21571WCSWZ4xx	450 MHz	N/A	–40°C to +105°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
AD21571WCSWZ5xx	500 MHz	N/A	–40°C to +105°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
AD21573WCBCZ4xx	450 MHz	N/A	–40°C to +105°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
AD21573WCBCZ5xx	500 MHz	N/A	–40°C to +105°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC570WCSWZ42xx	450 MHz	225 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSC570WCSWZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ3xx	300 MHz	300 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ5xx	500 MHz	500 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC572WCBCZ42xx	450 MHz	225 MHz	–40°C to +105°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC572WCBCZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ3xx	300 MHz	300 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ5xx	500 MHz	500 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2

[1] Z = RoHS Compliant Part.
[2] xx denotes the current die revision.
[3] For evaluation of all models, order the ADZS-SC573-EZLITE evaluation board.
[4] N/A means not applicable.
[5] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.