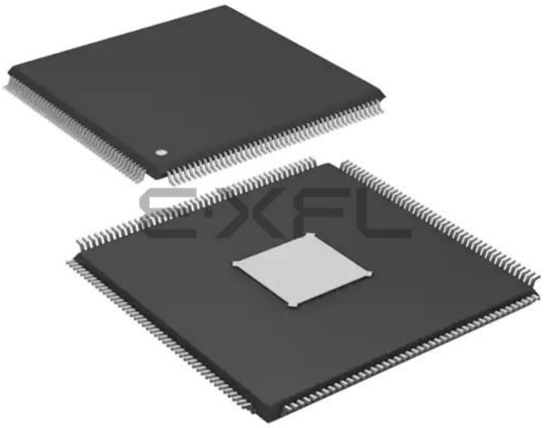

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz, 450MHz
Non-Volatile Memory	External
On-Chip RAM	1.640MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc570bswz-4

Single-Instruction, Multiple Data (SIMD) Computational Engine

The SHARC+ core contains two computational processing elements that operate as a single-instruction, multiple data (SIMD) engine.

The processing elements are referred to as PEx and PEy data registers and each contain an arithmetic logic unit (ALU), multiplier, shifter, and register file. PEx is always active and PEy is enabled by setting the PEYEN mode bit in the mode control register (MODE1).

SIMD mode allows the processors to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture efficiently executes math intensive DSP algorithms. In addition to all the features of previous generation SHARC cores, the SHARC+ core also provides a new and simpler way to execute an instruction only on the PEy data register.

SIMD mode also affects the way data transfers between memory and the processing elements because to sustain computational operation in the processing elements requires twice the data bandwidth. Therefore, entering SIMD mode doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values transfer with each memory or register file access.

Independent Parallel Computation Units

Within each processing element is a set of pipelined computational units. The computational units consist of a multiplier, arithmetic/logic unit (ALU), and shifter. These units are arranged in parallel, maximizing computational throughput. These computational units support IEEE 32-bit single-precision floating-point, 40-bit extended-precision floating-point, IEEE 64-bit double-precision floating-point, and 32-bit fixed-point data formats.

A multifunction instruction set supports parallel execution of the ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements per core.

All processing operations take one cycle to complete. For all floating-point operations, the processor takes two cycles to complete in case of data dependency. Double-precision floating-point data take two to six cycles to complete. The processor stalls for the appropriate number of cycles for an interlocked pipeline plus data dependency check.

Core Timer

Each SHARC+ processor core also has a timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register register files (16 primary, 16 secondary), combined with the enhanced Harvard architecture of the processor, allow unconstrained data flow between computation units and internal memory. The registers in the PEx data register file are referred to as R0–R15 and in the PEy data register file as S0–S15.

Context Switch

Many of the registers of the processor have secondary registers that can activate during interrupt servicing for a fast context switch. The data, DAG, and multiplier result registers have secondary registers. The primary registers are active at reset, while control bits in MODE1 activate the secondary registers.

Universal Registers

General-purpose tasks use the universal registers. The four USTAT registers allow easy bit manipulations (set, clear, toggle, test, XOR) for all control and status peripheral registers.

The data bus exchange register (PX) permits data to pass between the 64-bit PM data bus and the 64-bit DM data bus or between the 40-bit register file and the PM or DM data bus. These registers contain hardware to handle the data width difference.

Data Address Generators (DAG) With Zero-Overhead Hardware Circular Buffer Support

For indirect addressing and implementing circular data buffers in hardware, the ADSP-SC57x/ADSP-2157x processor uses the two data address generators (DAGs). Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and fast Fourier transforms (FFT). The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets and 16 secondary sets). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set Architecture (ISA)

The flexible instruction set architecture (ISA), a 48-bit instruction word, accommodates various parallel operations for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction. Additionally, the double-precision floating-point instruction set is an addition to the SHARC+ core.

Table 8. DMC Memory Map[1]

	Byte Address Space ARM Cortex-A5—Data Access and Instruction Fetch SHARC+—Data Access	Normal Word Address Space SHARC+ Data Access	VISA Address Space SHARC+ Instruction Fetch	ISA Address Space SHARC+ Instruction Fetch
DMC0 (1 GB)	0x80000000–0x805FFFFF	0x10000000–0x17FFFFFF	Not applicable	0x00400000–0x004FFFFF
	0x80600000–0x809FFFFF		Not applicable	Not applicable
	0x80A00000–0x80FFFFFF		0x00800000–0x00AFFFFF	Not applicable
	0x81000000–0x9FFFFFFF		Not applicable	Not applicable
	0xA0000000–0xBFFFFFFF	Not applicable	Not applicable	Not applicable

[1] The ARM Cortex-A5 can access the entire byte address space. The SHARC+ VISA/ISA address space for instruction fetch and the normal word address space for data access do not cover the entire byte address space.

System Crossbars (SCBs)

The system crossbars (SCBs) are the fundamental building blocks of a switch fabric style for on-chip system bus interconnection. The SCBs connect system bus masters to system bus slaves, providing concurrent data transfer between multiple bus masters and multiple bus slaves. A hierarchical model—built from multiple SCBs—provides a power and area efficient system interconnection.

The SCBs provide the following features:

- Highly efficient, pipelined bus transfer protocol for sustained throughput
- Full-duplex bus operation for flexibility and reduced latency
- Concurrent bus transfer support to allow multiple bus masters to access bus slaves simultaneously
- Protection model (privileged/secure) support for selective bus interconnect protection

Direct Memory Access (DMA)

The processors use direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processors can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory to memory DMA stream uses two channels: the source channel and the destination channel.

All DMA channels can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers: descriptor-based or register-based. Register-based DMA allows the processors to program DMA control registers directly to initiate a DMA transfer. On completion, the DMA control registers automatically update with original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together. Program a DMA channel to set up and start another DMA transfer automatically after the current sequence completes.

The DMA engine supports the following DMA operations:

- A single linear buffer that stops on completion
- A linear buffer with negative, positive, or zero stride length
- A circular autorefreshing buffer that interrupts when each buffer becomes full
- A similar circular buffer that interrupts on fractional buffers, such as at the halfway point
- The 1D DMA uses a set of identical ping pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address
- The 1D DMA uses a linked list of four-word descriptor sets containing a link pointer, an address, a length, and a configuration
- The 2D DMA uses an array of one-word descriptor sets, specifying only the base DMA address
- The 2D DMA uses a linked list of multiword descriptor sets, specifying all configurable parameters

Memory Direct Memory Access (MDMA)

The processor supports various memory direct memory access (MDMA) operations, including,

- Enhanced bandwidth MDMA channels with CRC protection (32-bit bus width, run on SYSCLK)
- Enhanced bandwidth MDMA channel (32-bit bus width, runs on SYSCLK)
- Maximum bandwidth MDMA channel (64-bit bus width, runs on SYCLK)

Extended Memory DMA

Extended memory DMA supports various operating modes, such as delay line (which allows processor reads and writes to external delay line buffers and to the external memory), with limited core interaction and scatter/gather DMA (writes to and from noncontiguous memory blocks).

Cyclic Redundant Code (CRC) Protection

The cyclic redundant codes (CRC) protection modules allow system software to calculate the signature of code, data, or both in memory, the content of memory-mapped registers, or periodic communication message objects. Dedicated hardware circuitry compares the signature with precalculated values and triggers appropriate fault events.

For example, every 100 ms the system software initiates the signature calculation of the entire memory contents and compares these contents with expected, precalculated values. If a mismatch occurs, a fault condition is generated through the processor core or the trigger routing unit.

The CRC is a hardware module based on a CRC32 engine that computes the CRC value of the 32-bit data-words presented to it. The source channel of the memory to memory DMA (in memory scan mode) provides data. The data can be optionally forwarded to the destination channel (memory transfer mode). The main features of the CRC peripheral are as follows:

- Memory scan mode
- Memory transfer mode
- Data verify mode
- Data fill mode
- User-programmable CRC32 polynomial
- Bit and byte mirroring option (endianness)
- Fault and error interrupt mechanisms
- 1D and 2D fill block to initialize an array with constants
- 32-bit CRC signature of a block of a memory or an MMR block

Event Handling

The processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing a higher priority event takes precedence over servicing a lower priority event.

The processors provide support for four different types of events:

- An emulation event causes the processors to enter emulation mode, allowing command and control of the processors through the JTAG interface.
- A reset event resets the processors.
- An exceptions event occurs synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions triggered on the one side by the SHARC+ core, such as data alignment (SIMD or long word) or compute violations (fixed or floating point), and illegal instructions cause core exceptions. Conditions triggered on the other side by the SEC, such as error correcting codes (ECC), parity, watchdog, or system clock, cause system exceptions.
- An interrupts event occurs asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

System Event Controller (SEC)

Both SHARC+ cores feature a system event controller. The SEC features include the following:

- Comprehensive system event source management, including interrupt enable, fault enable, priority, core mapping, and source grouping
- A distributed programming model where each system event source control and all status fields are independent of each other
- Determinism where all system events have the same propagation delay and provide unique identification of a specific system event source
- A slave control port that provides access to all SEC registers for configuration, status, and interrupt and fault services
- Global locking that supports a register level protection model to prevent writes to locked registers
- Fault management including fault action configuration, time out, external indication, and system reset

Trigger Routing Unit (TRU)

The trigger routing unit (TRU) provides system level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include,

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

SECURITY FEATURES

The following sections describe the security features of the ADSP-SC57x/ADSP-2157x processors.

ARM TrustZone

The ADSP-SC57x processors provide TrustZone technology that is integrated into the ARM Cortex-A5 processors. The TrustZone technology enables a secure state that is extended throughout the system fabric.

Cryptographic Hardware Accelerators

The ADSP-SC57x/ADSP-2157x processors support standards-based hardware accelerated encryption, decryption, authentication, and true random number generation.

Support for the hardware accelerated cryptographic ciphers includes the following:

- AES in ECB, CBC, ICM, and CTR modes with 128-bit, 192-bit, and 256-bit keys
- DES in ECB and CBC mode with 56-bit key
- 3DES in ECB and CBC mode with 3x 56-bit key
- ARC4 in stateful, stateless mode, up to 128-bit key

The two capacitors and the series resistor, shown in Figure 6, fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 6 are typical values only. The capacitor values are dependent upon the load capacitance recommendations of the crystal manufacturer and the physical layout of the printed circuit board (PCB). The resistor value depends on the drive level specified by the crystal manufacturer. The user must verify the customized values based on careful investigations on multiple devices over the required temperature range.

A third overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit, shown in Figure 6. A design procedure for third overtone operation is discussed in detail in "Using Third Overtone Crystals with the ADSP-218x DSP" (EE-168). The same recommendations can be used for the USB crystal oscillator.

Clock Distribution Unit (CDU)

The two CGUs each provide outputs which feed a clock distribution unit (CDU). The clock outputs CLKO0–CLKO9 are connected to various targets. For more information, refer to the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference.

Power-Up

SYS_XTALx oscillations (SYS_CLKINx) start when power is applied to the VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ starts on-chip PLL locking (PLL lock counter). The deassertion must apply only if all voltage supplies and SYS_CLKINx oscillations are valid (refer to the Power-Up Reset Timing section).

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_ CLKIN0 input. Refer to the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference to change the default mapping of clocks.

Booting

The processors have several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE[n] input pins. There are two categories of boot modes. In master boot mode, the processors actively load data from serial memories. In slave boot modes, the processors receive data from external host devices.

The boot modes are shown in Table 9. These modes are implemented by the SYS_BMODE[n] bits of the reset configuration register and are sampled during power-on resets and software initiated resets.

In the ADSP-SC57x processors, the ARM Cortex-A5 (Core 0) controls the boot process, including loading all internal and external memory. Likewise, in the ADSP-2157x processors, the SHARC+ (Core 1) controls the boot function. The option for secure boot is available on all models.

Table 9. Boot Modes

SYS_BMODE[n] Setting[1, 2]	Boot Mode
000	No boot
001	SPI2 master
010	SPI2 slave
011	UART0 slave
100	Reserved
101	Reserved
110	Link0 slave

[1] SYS_BMODE2 pin is applicable only for the BGA package.
[2] Link0 slave boot is supported only on the BGA package.

Thermal Monitoring Unit (TMU)

The thermal monitoring unit (TMU) provides on-chip temperature measurement for applications that require substantial power consumption. The TMU is integrated into the processor die and digital infrastructure using an MMR-based system access to measure the die temperature variations in real-time.

TMU features include the following:

- On-chip temperature sensing
- Programmable over temperature and under temperature limits
- Programmable conversion rate
- Programmable clock source selection to run the sensor off an independent local clock
- Averaging feature available

Power Supplies

The processors have separate power supply connections for

- Internal (VDD_INT)
- External (VDD_EXT)
- USB (VDD_USB)
- HADC/TMU (VDD_HADC)
- DMC (VDD_DMC)

All power supplies must meet the specifications provided in Operating Conditions section. All external supply pins must be connected to the same power supply.

Power Management

As shown in Table 10, the processors support four different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate specifications (see the Specifications section for processor operating conditions). If the feature or the peripheral is not used, refer to Table 25.

Table 10. Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DD_INT}
DDR3/DDR2/LPDDR	V_{DD_DMC}
USB	V_{DD_USB}
HADC/TMU	V_{DD_HADC}
All other I/O (includes SYS, JTAG, and ports pins)	V_{DD_EXT}

The power dissipated by a processor is largely a function of the clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

Target Board JTAG Emulator Connector

The Analog Devices DSP tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. The Analog Devices DSP tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor JTAG interface ensures the emulator does not affect target system loading or timing.

For information on JTAG emulator operation, see the appropriate emulator hardware user's guide at SHARC Processors Software and Tools.

SYSTEM DEBUG

The processors include various features that allow easy system debug. These are described in the following sections.

System Watchpoint Unit (SWU)

The system watchpoint unit (SWU) is a single module that connects to a single system bus and provides transaction monitoring. One SWU is attached to the bus going to each system slave. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently but share common event (for example, interrupt and trigger) outputs.

Debug Access Port (DAP)

Debug access port (DAP) provides IEEE 1149.1 JTAG interface support through the JTAG debug. The DAP provides an optional instrumentation trace for both the core and system. It provides a trace stream that conforms to *MIPI System Trace Protocol version 2 (STPv2)*.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including an integrated development environment (CrossCore® Embedded Studio), evaluation products, emulators, and a variety of software add ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers the CrossCore Embedded Studio integrated development environment (IDE).

CrossCore Embedded Studio is based on the Eclipse framework. Supporting most Analog Devices processor families, it is the IDE of choice for processors, including multicore devices.

CrossCore Embedded Studio seamlessly integrates available software add ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information, visit www.analog.com/cces.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides a wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Various EZ-Extenders® are also available, which are daughter cards that deliver additional specialized functionality, including audio and video processing. For more information visit www.analog.com.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in circuit. This permits users to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in circuit programming of the on-board Flash® device to store user specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add Ins for CrossCore Embedded Studio

Analog Devices offers software add ins which seamlessly integrate with CrossCore Embedded Studio to extend the capabilities and reduce development time. Add ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add ins are viewable through the CrossCore Embedded Studio IDE once the add in is installed.

Table 11. ADSP-SC57x/ADSP-2157x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
$\overline{\text{DMC\_UDQS}}$	InOut	**Data Strobe for Upper Byte (Complement).** Complement of DMC_UDQS. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Connects to half of the VDD_DMC voltage. Applies to the DMC0_VREF pin.
$\overline{\text{DMC\_WE}}$	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory.
ETH_COL	Input	**MII Collision Detect.** Collision detect input signal valid only in MII.
ETH_CRS	Input	**MII Carrier Sense.** Asserted by the PHY when either the transmit or receive medium is not idle. Deasserted when both are idle. This signal is not used in RMII/RGMII modes.
ETH_MDC	Output	**Management Channel Clock.** Clocks the MDC input of the PHY for RMII/RGMII.
ETH_MDIO	InOut	**Management Channel Serial Data.** Bidirectional data bus for PHY control for RMII/RGMII.
ETH_PTPAUXIN[n]	Input	**PTP Auxiliary Trigger Input.** Assert this signal to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO.
ETH_PTPCLKIN[n]	Input	**PTP Clock Input.** Optional external PTP clock input.
ETH_PTPPPS[n]	Output	**PTP Pulse Per Second Output.** When the advanced time stamp feature enables, this signal is asserted based on the PPS mode selected. Otherwise, this signal is asserted every time the seconds counter is incremented.
ETH_RXCLK_REFCLK	InOut	**RXCLK (10/100/1000) or REFCLK (10/100).**
ETH_RXCTL_RXDV	InOut	**RXCTL (10/100/1000) or RXDV (10/100).** In RGMII mode, RX_CTL multiplexes receive data valid and receiver error. In RMII mode, RXDV is carrier sense and receive data valid (CRS_DV), multiplexed on alternating clock cycles. In MII mode, RXDV is receive data valid (RX_DV), asserted by the PHY when the data on ETH_RXD[n] is valid.
ETH_RXD[n]	Input	**Receive Data n.** Receive data bus.
ETH_RXERR	Input	**Receive Error.**
ETH_TXCLK	Input	**Reference Clock.** Externally supplied Ethernet clock
ETH_TXCTL_TXEN	InOut	**TXCTL (10/100/1000) or TXEN (10/100).**
ETH_TXD[n]	Output	**Transmit Data n.** Transmit data bus.
HADC_EOC_DOUT	Output	**End of Conversion/Serial Data Out.** Transitions high for one cycle of the HADC internal clock at the end of every conversion. Alternatively, HADC serial data out can be seen by setting the appropriate bit in HADC_CTL.
HADC_VIN[n]	Input	**Analog Input at Channel n.** Analog voltage inputs for digital conversion.
HADC_VREFN	Input	**Ground Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications.
HADC_VREFP	Input	**External Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications.
JTG_TCK	Input	**JTAG Clock.** JTAG test access port clock.
JTG_TDI	Input	**JTAG Serial Data In.** JTAG test access port data input.
JTG_TDO	Output	**JTAG Serial Data Out.** JTAG test access port data output.
JTG_TMS	Input	**JTAG Mode Select.** JTAG test access port mode select.
$\overline{\text{JTG\_TRST}}$	Input	**JTAG Reset.** JTAG test access port reset.
LP_ACK	InOut	**Acknowledge.** Provides handshaking. When the link port is configured as a receiver, ACK is an output. When the link port is configured as a transmitter, ACK is an input.
LP_CLK	InOut	**Clock.** When the link port is configured as a receiver, CLK is an input. When the link port is configured as a transmitter, CLK is an output.
LP_D[n]	InOut	**Data n.** Data bus. Input when receiving, output when transmitting.
MLB_CLK	InOut	**Single Ended Clock.**
MLB_CLKN	InOut	**Differential Clock (–).**
MLB_CLKOUT	InOut	**Single Ended Clock Out.**
MLB_CLKP	InOut	**Differential Clock (+).**
MLB_DAT	InOut	**Single Ended Data.**

400-BALL CSP_BGA SIGNAL DESCRIPTIONS

The processor pin definitions are shown in Table 12 for the 400-ball CSP_BGA package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a GPIO port pin.
- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a GPIO pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the Digital Audio Interface (DAI) chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for complete information on the use of the DAI and SRUs.

Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions

Signal Name	Description	Port	Pin Name
ACM0_A0	ACM0 ADC Control Signals	F	PF_11
ACM0_A1	ACM0 ADC Control Signals	C	PC_14
ACM0_A2	ACM0 ADC Control Signals	C	PC_15
ACM0_A3	ACM0 ADC Control Signals	A	PA_14
ACM0_A4	ACM0 ADC Control Signals	B	PB_01
ACM0_T0	ACM0 External Trigger n	A	PA_15
C1_FLG0	SHARC Core 1 Flag Pin	E	PE_13
C1_FLG1	SHARC Core 1 Flag Pin	E	PE_01
C1_FLG2	SHARC Core 1 Flag Pin	F	PF_04
C1_FLG3	SHARC Core 1 Flag Pin	D	PD_06
C2_FLG0	SHARC Core 2 Flag Pin	B	PB_00
C2_FLG1	SHARC Core 2 Flag Pin	C	PC_14
C2_FLG2	SHARC Core 2 Flag Pin	F	PF_11
C2_FLG3	SHARC Core 2 Flag Pin	E	PE_15
CAN0_RX	CAN0 Receive	C	PC_12
CAN0_TX	CAN0 Transmit	C	PC_13
CAN1_RX	CAN1 Receive	C	PC_14
CAN1_TX	CAN1 Transmit	C	PC_15
CNT0_DG	CNT0 Count Down and Gate	D	PD_08
CNT0_UD	CNT0 Count Up and Direction	E	PE_13
CNT0_ZM	CNT0 Count Zero Marker	D	PD_07
DAI0_PIN01	DAI0 Pin 1	Not Muxed	DAI0_PIN01
DAI0_PIN02	DAI0 Pin 2	Not Muxed	DAI0_PIN02
DAI0_PIN03	DAI0 Pin 3	Not Muxed	DAI0_PIN03
DAI0_PIN04	DAI0 Pin 4	Not Muxed	DAI0_PIN04
DAI0_PIN05	DAI0 Pin 5	Not Muxed	DAI0_PIN05
DAI0_PIN06	DAI0 Pin 6	Not Muxed	DAI0_PIN06
DAI0_PIN07	DAI0 Pin 7	Not Muxed	DAI0_PIN07
DAI0_PIN08	DAI0 Pin 8	Not Muxed	DAI0_PIN08
DAI0_PIN09	DAI0 Pin 9	Not Muxed	DAI0_PIN09
DAI0_PIN10	DAI0 Pin 10	Not Muxed	DAI0_PIN10
DAI0_PIN11	DAI0 Pin 11	Not Muxed	DAI0_PIN11
DAI0_PIN12	DAI0 Pin 12	Not Muxed	DAI0_PIN12
DAI0_PIN13	DAI0 Pin 13	Not Muxed	DAI0_PIN13
DAI0_PIN14	DAI0 Pin 14	Not Muxed	DAI0_PIN14
DAI0_PIN15	DAI0 Pin 15	Not Muxed	DAI0_PIN15

Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DMC0_ODT	DMC0 On die termination	Not Muxed	DMC0_ODT
DMC0_RAS	DMC0 Row Address Strobe	Not Muxed	DMC0_RAS
DMC0_RESET	DMC0 Reset (DDR3 only)	Not Muxed	DMC0_RESET
DMC0_RZQ	DMC0 External calibration resistor connection	Not Muxed	DMC0_RZQ
DMC0_UDM	DMC0 Data Mask for Upper Byte	Not Muxed	DMC0_UDM
DMC0_UDQS	DMC0 Data Strobe for Upper Byte	Not Muxed	DMC0_UDQS
DMC0_UDQS	DMC0 Data Strobe for Upper Byte (complement)	Not Muxed	DMC0_UDQS
DMC0_VREF	DMC0 Voltage Reference	Not Muxed	DMC0_VREF
DMC0_WE	DMC0 Write Enable	Not Muxed	DMC0_WE
ETH0_COL	EMAC0 MII Collision detect	C	PC_06
ETH0_CRS	EMAC0 Carrier Sense/RMII Receive Data Valid	B	PB_01
ETH0_MDC	EMAC0 Management Channel Clock	A	PA_11
ETH0_MDIO	EMAC0 Management Channel Serial Data	A	PA_10
ETH0_PTPAUXIN0	EMAC0 PTP Auxiliary Trigger Input 0	D	PD_14
ETH0_PTPAUXIN1	EMAC0 PTP Auxiliary Trigger Input 1	D	PD_15
ETH0_PTPAUXIN2	EMAC0 PTP Auxiliary Trigger Input 2	F	PF_06
ETH0_PTPAUXIN3	EMAC0 PTP Auxiliary Trigger Input 3	F	PF_07
ETH0_PTPCLKIN0	EMAC0 PTP Clock Input 0	F	PF_05
ETH0_PTPPPS0	EMAC0 PTP Pulse Per Second Output 0	A	PA_09
ETH0_PTPPPS1	EMAC0 PTP Pulse Per Second Output 1	D	PD_08
ETH0_PTPPPS2	EMAC0 PTP Pulse Per Second Output 2	E	PE_00
ETH0_PTPPPS3	EMAC0 PTP Pulse Per Second Output 3	E	PE_01
ETH0_RXCLK_REFCLK	EMAC0 RXCLK (10/100/1000) or REFCLK (10/100)	B	PB_00
ETH0_RXCTL_RXDV	EMAC0 RXCTL (10/100/1000) or CRS (10/100)	B	PB_01
ETH0_RXD0	EMAC0 Receive Data 0	A	PA_13
ETH0_RXD1	EMAC0 Receive Data 1	A	PA_12
ETH0_RXD2	EMAC0 Receive Data 2	A	PA_14
ETH0_RXD3	EMAC0 Receive Data 3	A	PA_15
ETH0_RXERR	EMAC0 Receive Error	B	PB_03
ETH0_TXCLK	EMAC0 Transmit Clock	B	PB_04
ETH0_TXCTL_TXEN	EMAC0 TXCTL (10/100/1000) or TXEN (10/100)	B	PB_09
ETH0_TXD0	EMAC0 Transmit Data 0	B	PB_07
ETH0_TXD1	EMAC0 Transmit Data 1	B	PB_08
ETH0_TXD2	EMAC0 Transmit Data 2	B	PB_06
ETH0_TXD3	EMAC0 Transmit Data 3	B	PB_05
HADC0_EOC_DOUT	HADC0 End of Conversion/Serial Data Out	D	PD_09
HADC0_VIN0	HADC0 Analog Input at channel 0	Not Muxed	HADC0_VIN0
HADC0_VIN1	HADC0 Analog Input at channel 1	Not Muxed	HADC0_VIN1
HADC0_VIN2	HADC0 Analog Input at channel 2	Not Muxed	HADC0_VIN2
HADC0_VIN3	HADC0 Analog Input at channel 3	Not Muxed	HADC0_VIN3
HADC0_VIN4	HADC0 Analog Input at channel 4	Not Muxed	HADC0_VIN4
HADC0_VIN5	HADC0 Analog Input at channel 5	Not Muxed	HADC0_VIN5
HADC0_VIN6	HADC0 Analog Input at channel 6	Not Muxed	HADC0_VIN6
HADC0_VIN7	HADC0 Analog Input at channel 7	Not Muxed	HADC0_VIN7
HADC0_VREFN	HADC0 Ground Reference for ADC	Not Muxed	HADC0_VREFN
HADC0_VREFP	HADC0 External Reference for ADC	Not Muxed	HADC0_VREFP
JTG_TCK	JTAG Clock	Not Muxed	JTG_TCK
JTG_TDI	JTAG Serial Data In	Not Muxed	JTG_TDI

Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D02	EPPI0 Data 2	D	PD_12
PPI0_D03	EPPI0 Data 3	D	PD_13
PPI0_D04	EPPI0 Data 4	D	PD_14
PPI0_D05	EPPI0 Data 5	D	PD_15
PPI0_D06	EPPI0 Data 6	C	PC_05
PPI0_D07	EPPI0 Data 7	D	PD_09
PPI0_D08	EPPI0 Data 8	C	PC_01
PPI0_D09	EPPI0 Data 9	C	PC_02
PPI0_D10	EPPI0 Data 10	C	PC_03
PPI0_D11	EPPI0 Data 11	C	PC_04
PPI0_D12	EPPI0 Data 12	E	PE_00
PPI0_D13	EPPI0 Data 13	C	PC_07
PPI0_D14	EPPI0 Data 14	C	PC_08
PPI0_D15	EPPI0 Data 15	E	PE_01
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	C	PC_14
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	C	PC_15
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	C	PC_06
SPI0_CLK	SPI0 Clock	C	PC_01
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_02
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_03
SPI0_RDY	SPI0 Ready	C	PC_05
SPI0_SEL1	SPI0 Slave Select Output 1	C	PC_04
SPI0_SEL2	SPI0 Slave Select Output 2	C	PC_05
SPI0_SEL3	SPI0 Slave Select Output 3	C	PC_06
SPI0_SEL4	SPI0 Slave Select Output 4	A	PA_09
SPI0_SEL5	SPI0 Slave Select Output 5	F	PF_05
SPI0_SEL6	SPI0 Slave Select Output 6	F	PF_04
SPI0_SEL7	SPI0 Slave Select Output 7	D	PD_05
SPI0_SS	SPI0 Slave Select Input	C	PC_04
SPI1_CLK	SPI1 Clock	C	PC_07
SPI1_MISO	SPI1 Master In, Slave Out	C	PC_08
SPI1_MOSI	SPI1 Master Out, Slave In	C	PC_09
SPI1_RDY	SPI1 Ready	C	PC_11
SPI1_SEL1	SPI1 Slave Select Output 1	C	PC_10
SPI1_SEL2	SPI1 Slave Select Output 2	C	PC_11
SPI1_SEL3	SPI1 Slave Select Output 3	F	PF_11
SPI1_SEL4	SPI1 Slave Select Output 4	A	PA_14
SPI1_SEL5	SPI1 Slave Select Output 5	B	PB_02
SPI1_SEL6	SPI1 Slave Select Output 6	D	PD_07
SPI1_SEL7	SPI1 Slave Select Output 7	D	PD_06
SPI1_SS	SPI1 Slave Select Input	C	PC_10
SPI2_CLK	SPI2 Clock	B	PB_14
SPI2_D2	SPI2 Data 2	B	PB_12
SPI2_D3	SPI2 Data 3	B	PB_13
SPI2_MISO	SPI2 Master In, Slave Out	B	PB_10
SPI2_MOSI	SPI2 Master Out, Slave In	B	PB_11
SPI2_RDY	SPI2 Ready	C	PC_00
SPI2_SEL1	SPI2 Slave Select Output 1	B	PB_15

Table 20. ADSP-SC57x/ADSP-2157x 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
SPI2_MISO	SPI2 Master In, Slave Out	B	PB_10
SPI2_MOSI	SPI2 Master Out, Slave In	B	PB_11
SPI2_RDY	SPI2 Ready	C	PC_00
SPI2_SEL1	SPI2 Slave Select Output 1	B	PB_15
SPI2_SEL2	SPI2 Slave Select Output 2	A	PA_07
SPI2_SEL3	SPI2 Slave Select Output 3	C	PC_00
SPI2_SEL4	SPI2 Slave Select Output 4	D	PD_08
SPI2_SEL5	SPI2 Slave Select Output 5	A	PA_15
SPI2_SEL6	SPI2 Slave Select Output n	A	PA_10
SPI2_SEL7	SPI2 Slave Select Output n	B	PB_07
SPI2_SS	SPI2 Slave Select Input	B	PB_15
SYS_BMODE0	Boot Mode Control n	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control n	Not Muxed	SYS_BMODE1
SYS_CLKIN0	Clock/Crystal Input	Not Muxed	SYS_CLKIN0
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
SYS_FAULT	Active-High Fault Output	Not Muxed	SYS_FAULT
SYS_HWRST	Processor Hardware Reset Control	Not Muxed	SYS_HWRST
SYS_RESOUT	Reset Output	Not Muxed	SYS_RESOUT
SYS_XTAL0	Crystal Output	Not Muxed	SYS_XTAL0
TM0_ACI0	TIMER0 Alternate Capture Input 0	A	PA_06
TM0_ACI1	TIMER0 Alternate Capture Input 1	A	PA_08
TM0_ACI2	TIMER0 Alternate Capture Input 2	C	PC_12
TM0_ACI3	TIMER0 Alternate Capture Input 3	C	PC_14
TM0_ACI4	TIMER0 Alternate Capture Input 4	C	PC_13
TM0_ACI5	TIMER0 Alternate Capture Input 5	Not Applicable	DAI_PB04_O
TM0_ACI6	TIMER0 Alternate Capture Input 6	Not Applicable	DAI_PB19_O
TM0_ACI7	TIMER0 Alternate Capture Input 7	Not Applicable	CNT0_TO
TM0_ACLK1	TIMER0 Alternate Clock 1	A	PA_00
TM0_ACLK2	TIMER0 Alternate Clock 2	C	PC_01
TM0_ACLK3	TIMER0 Alternate Clock 3	D	PD_09
TM0_ACLK4	TIMER0 Alternate Clock 4	C	PC_11
TM0_ACLK5	TIMER0 Alternate Clock 5	Not Applicable	DAI_PB03_O
TM0_ACLK6	TIMER0 Alternate Clock 6	Not Applicable	DAI_PB20_O
TM0_ACLK7	TIMER0 Alternate Clock 7	Not Applicable	SYS_CLKIN0
TM0_CLK	TIMER0 Clock	C	PC_03
TM0_TMR0	TIMER0 Timer 0	D	PD_02
TM0_TMR1	TIMER0 Timer 1	D	PD_03
TM0_TMR2	TIMER0 Timer 2	D	PD_04
TM0_TMR3	TIMER0 Timer 3	B	PB_01
TM0_TMR4	TIMER0 Timer 4	B	PB_03
TM0_TMR5	TIMER0 Timer 5	C	PC_15
TM0_TMR7	TIMER0 Timer 7	D	PD_07
TRACE0_CLK	TRACE0 Trace Clock	A	PA_00
TRACE0_D00	TRACE0 Trace Data	A	PA_01
TRACE0_D01	TRACE0 Trace Data	A	PA_02
TRACE0_D02	TRACE0 Trace Data	A	PA_03
TRACE0_D03	TRACE0 Trace Data	A	PA_04
TRACE0_D04	TRACE0 Trace Data	D	PD_10

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
PB_10	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 10 Notes: Connect to VDD_EXT or GND if not used
PB_11	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 11 Notes: Connect to VDD_EXT or GND if not used
PB_12	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 12 Notes: Connect to VDD_EXT or GND if not used
PB_13	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 13 Notes: Connect to VDD_EXT or GND if not used
PB_14	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 14 Notes: Connect to VDD_EXT or GND if not used
PB_15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTB Position 15 Notes: See note[2]
PC_00	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 0 Notes: See note[2]
PC_01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 1 Notes: See note[2]
PC_02	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 2 Notes: See note[2]
PC_03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 3 Notes: See note[2]
PC_04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 4 Notes: See note[2]
PC_05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 5 Notes: See note[2]
PC_06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 6 Notes: See note[2]
PC_07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 7 Notes: See note[2]
PC_08	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 8 Notes: See note[2]
PC_09	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 9 Notes: See note[2]
PC_10	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 10 Notes: See note[2]
PC_11	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 11 Notes: See note[2]
PC_12	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 12 Notes: See note[2]
PC_13	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 13 Notes: See note[2]
PC_14	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 14 Notes: See note[2]
PC_15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 15 Notes: See note[2]

SPECIFICATIONS

For information about product specifications, contact your Analog Devices representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	CCLK ≤ 450 MHz	1.05	1.10	1.15	V
		CCLK ≤ 500 MHz	1.10	1.15	1.20	V
V_{DD_EXT}	External (I/O) Supply Voltage		3.13	3.3	3.47	V
V_{DD_HADC}	Analog Power Supply Voltage		3.13	3.3	3.47	V
V_{DD_DMC}[1]	DDR2/LPDDR Controller Supply Voltage		1.7	1.8	1.9	V
	DDR3 Controller Supply Voltage		1.425	1.5	1.575	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage Applies to the DMC0_VREF pin		$0.49 \times V_{DD\_DMC}$	$0.50 \times V_{DD\_DMC}$	$0.51 \times V_{DD\_DMC}$	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{HADC0_VINx}	HADC Input Voltage		0		$V_{HADC\_REF} + 0.2$	V
V_{IH}[4]	High Level Input Voltage	$V_{DD\_EXT} = 3.47$ V	2.0			V
V_{IHTWI}[5, 6]	High Level Input Voltage	$V_{DD\_EXT} = 3.47$ V	$0.7 \times V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IL}[4]	Low Level Input Voltage	$V_{DD\_EXT} = 3.13$ V			0.8	V
V_{ILTWI}[5, 6]	Low Level Input Voltage	$V_{DD\_EXT} = 3.13$ V			$0.3 \times V_{VBUSTWI}$	V
V_{IL_DDR2}[7]	Low Level Input Voltage	$V_{DD\_DMC} = 1.7$ V			$V_{REF} - 0.25$	V
V_{IL_DDR3}[7]	Low Level Input Voltage	$V_{DD\_DMC} = 1.425$ V			$V_{REF} - 0.175$	V
V_{IH_DDR2}[7]	High Level Input Voltage	$V_{DD\_DMC} = 1.9$ V	$V_{REF} + 0.25$			V
V_{IH_DDR3}[7]	High Level Input Voltage	$V_{DD\_DMC} = 1.575$ V	$V_{REF} + 0.175$			V
V_{IL_LPDDR}[8]	Low Level Input Voltage	$V_{DD\_DMC} = 1.7$ V			$0.2 \times V_{DD\_DMC}$	V
V_{IH_LPDDR}[8]	High Level Input Voltage	$V_{DD\_DMC} = 1.9$ V	$0.8 \times V_{DD\_DMC}$			V
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 450 MHz	0		95	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = –40°C to +100°C CCLK ≤ 450 MHz	–40		+125	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 450 MHz	0		90	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = –40°C to +105°C CCLK ≤ 450 MHz	–40		+125	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 500 MHz	0		100	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = –40°C to +95°C CCLK ≤ 500 MHz	–40		+125	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 500 MHz	0		95	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = –40°C to +100°C CCLK ≤ 500 MHz	–40		+125	°C

HADC

HADC Electrical Characteristics

Table 34. HADC Electrical Characteristics

Parameter	Conditions	Typ	Unit
$I_{DD\_HADC\_IDLE}$	Current consumption on V_{DD_HADC} HADC is powered on, but not converting	2.0	mA
$I_{DD\_HADC\_ACTIVE}$	Current consumption on V_{DD_HADC} during a conversion	2.5	mA
$I_{DD\_HADC\_POWERDOWN}$	Current consumption on V_{DD_HADC} Analog circuitry of the HADC is powered down	60	µA

HADC DC Accuracy

Table 35. HADC DC Accuracy for CSP_BGA[1]

Parameter	Typ	Unit[2]
Resolution	9	Bits
No Missing Codes (NMC) – Unrestricted	9	Bits
No Missing Codes (NMC) – Pin Restrictions[3]	10	Bits
Integral Nonlinearity (INL)	±2	LSB
Differential Nonlinearity (DNL)	±2	LSB
Offset Error	±5	LSB
Offset Error Matching	±6	LSB
Gain Error	±4	LSB
Gain Error Matching	±4	LSB

[1] See the Operating Conditions section for the HADC0_VINx specification.
[2] LSB = HADC0_VREFP ÷ 512.
[3] Pin restrictions required: pins DAI18, DAI19, and DAI20 must be programmed to inputs and a static (non-switching) signal applied to the pins.

Table 36. HADC DC Accuracy for LQFP_EP[1]

Parameter	Typ	Unit[2]
Resolution	7	Bits
No Missing Codes (NMC) – Unrestricted	7	Bits
No Missing Codes (NMC) – Pin Restrictions[3]	9	Bits
Integral Nonlinearity (INL)	±2	LSB
Differential Nonlinearity (DNL)	±2	LSB
Offset Error	±5	LSB
Offset Error Matching	±6	LSB
Gain Error	±4	LSB
Gain Error Matching	±4	LSB

[1] See the Operating Conditions section for the HADC0_VINx specification.
[2] LSB = HADC0_VREFP ÷ 128.
[3] Pin restrictions required: pins DAI18, DAI19, and DAI20 must be programmed to inputs and a static (non-switching) signal applied to the pins.

HADC Timing Specifications

Table 37. HADC Timing Specifications

Parameter	Typ	Max	Unit
Conversion Time[1]	$20 \times T_{SAMPLE}$		µs
Throughput Range		1	MSPS
T_{WAKEUP}		100	µs

[1] Refer to the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for additional information about T_{SAMPLE}.

TMU

TMU Characteristics

Table 38. TMU Characteristics

Parameter	Typ	Unit
Resolution	1	°C
Accuracy	±8	°C

Table 39. TMU Gain and Offset

Junction Temperature Range	TMU_GAIN	TMU_OFFSET
–40°C to +40°C	Contact Analog Devices, Inc.	
40°C to 85°C	Contact Analog Devices, Inc.	
85°C to 133°C	Contact Analog Devices, Inc.	

DDR3 SDRAM Clock and Control Cycle Timing

Table 49 and Figure 16 show mobile DDR3 SDRAM clock and control cycle timing, related to the DMC.

Table 49. DDR3 SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.5 V

Parameter		450 MHz[1] Min	Max	Unit
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.22		ns
$t_{CH(abs)}$[2]	Minimum Clock Pulse Width	0.47	0.53	t_{CK}
$t_{CL(abs)}$[2]	Maximum Clock Pulse Width	0.47	0.53	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	0.2		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	0.275		ns

[1] To ensure proper operation of the DDR3, all the DDR3 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

[2] As per JESD79-3F definition.

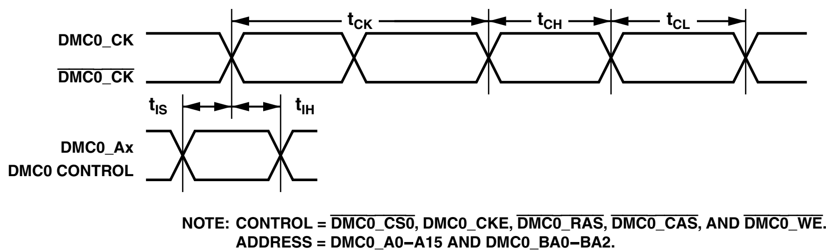

Figure 16. DDR3 SDRAM Clock and Control Cycle Timing

Table 64. SPI2 Port—Master Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	2.7		ns
t_{HSPIDM}	SPIx_CLK Sampling Edge to Data Input Invalid	0.75		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{\text{SPIx\_SEL}}$ low to First SPI_CLK Edge for CPHA = 1[2]	$t_{SPICLKPROG} - 5$		ns
	$\overline{\text{SPIx\_SEL}}$ low to First SPI_CLK Edge for CPHA = 0[2]	$1.5 \times t_{SPICLKPROG} - 5$		ns
t_{SPICHM}	SPIx_CLK High Period[3]	$0.5 \times t_{SPICLKPROG} - 1.5$		ns
t_{SPICLM}	SPIx_CLK Low Period[3]	$0.5 \times t_{SPICLKPROG} - 1.5$		ns
t_{SPICLK}	SPIx_CLK Period[3]	$t_{SPICLKPROG} - 1.5$		ns
t_{HDSM}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SEL}}$ High for CPHA = 1[2]	$1.5 \times t_{SPICLKPROG} - 5$		ns
	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SEL}}$ High for CPHA = 0[2]	$t_{SPICLKPROG} - 5$		ns
t_{SPITDM}	Sequential Transfer Delay[2, 4]	$t_{SPICLKPROG} - 1.5$		ns
$t_{DDSPIDM}$	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		3.17	ns
$t_{HDSPIDM}$	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	−2.4		ns

[1] All specifications apply to SPI2 only.
[2] Specification assumes the LEADX and LAGX bits in the SPI_DLY register are 1.
[3] See Table 27 for details on the minimum period that may be programmed for $t_{SPICLKPROG}$.
[4] Applies to sequential mode with STOP ≥ 1.

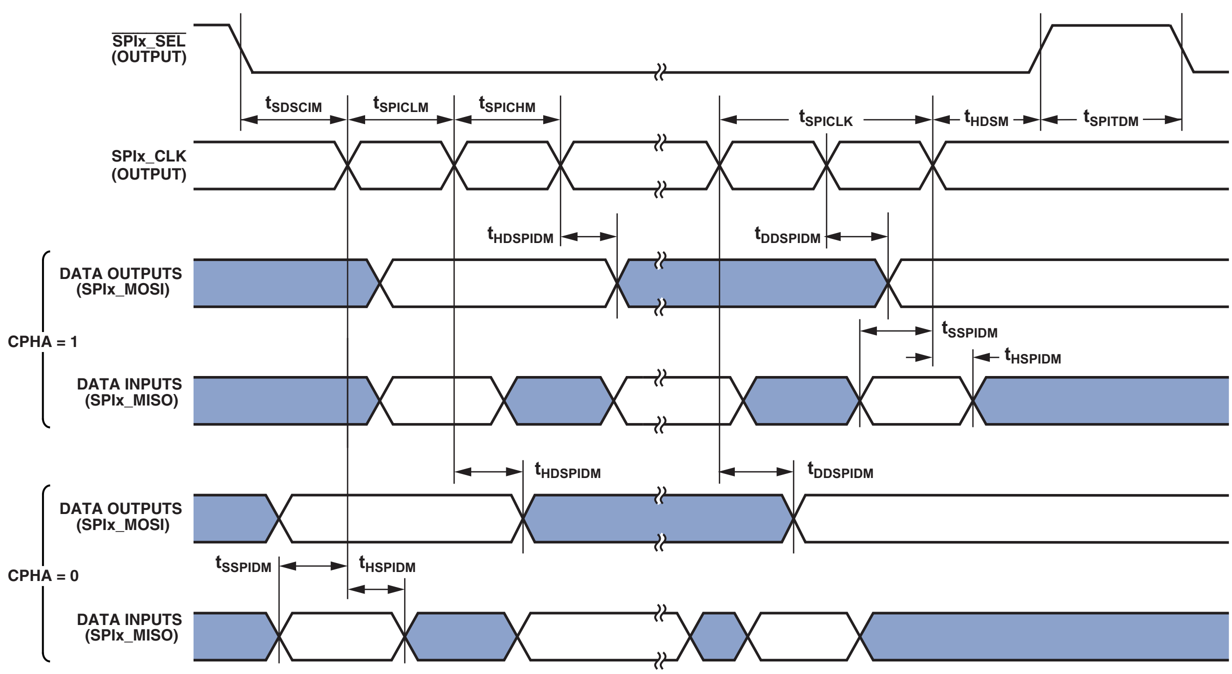

Figure 36. SPI Port—Master Timing

General-Purpose IO Port Timing

Table 72 and Figure 44 describe I/O timing, related to the general-purpose ports (PORT).

Table 72. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$2 \times t_{SCLK0} - 1.5$		ns

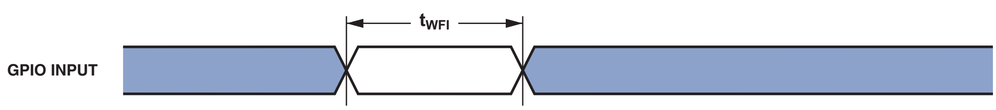

Figure 44. General-Purpose Port Timing

General-Purpose I/O Timer Cycle Timing

Table 73, Table 74, and Figure 45 describe timer expired operations related to the general-purpose timer (TIMER). The input signal is asynchronous in Width Capture Mode and External Clock Mode and has an absolute maximum input frequency of f_{SCLK}/4 MHz. The Width Value value is the timer period assigned in the TMx_TMRn_WIDTH register and can range from 1 to $2^{32} - 1$. When externally generated, the TMx_CLK clock is called $f_{TMRCLKEXT}$:

$$t_{TMRCLKEXT} = \frac{1}{f_{TMRCLKEXT}}$$

Table 73. Timer Cycle Timing—Internal Mode

Parameter		Min	Max	Unit
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[1]	$2 \times t_{SCLK}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)[2]	$t_{SCLK} \times \text{WIDTH} - 1.5$	$t_{SCLK} \times \text{WIDTH} + 1.5$	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 2 to $2^{32} - 1$).

Table 74. Timer Cycle Timing—External Mode

Parameter		Min	Max	Unit
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{EXT_CLK}	Timer External Clock Period[2]	$t_{TMRCLKEXT}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In EXT_CLK Cycles)[3]	$t_{EXT\_CLK} \times \text{WIDTH} - 1.5$	$t_{EXT\_CLK} \times \text{WIDTH} + 1.5$	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external TMR_CLK. For the external TMR_CLK maximum frequency, see the $f_{TMRCLKEXT}$ specification in Table 27.
[3] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

Mobile Storage Interface (MSI) Controller Timing

Table 93 and Figure 65 show I/O timing related to the MSI.

Table 93. MSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	4.8		ns
t_{IH}	Input Hold Time	–0.5		ns
Switching Characteristics				
f_{PP}	Clock Frequency Data Transfer Mode[1]		45	MHz
t_{WL}	Clock Low Time	8		ns
t_{WH}	Clock High Time	8		ns
t_{TLH}	Clock Rise Time		3	ns
t_{THL}	Clock Fall Time		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		2.1	ns
t_{OH}	Output Hold Time	–1.8		ns

[1] $t_{PP} = 1/f_{PP}$.

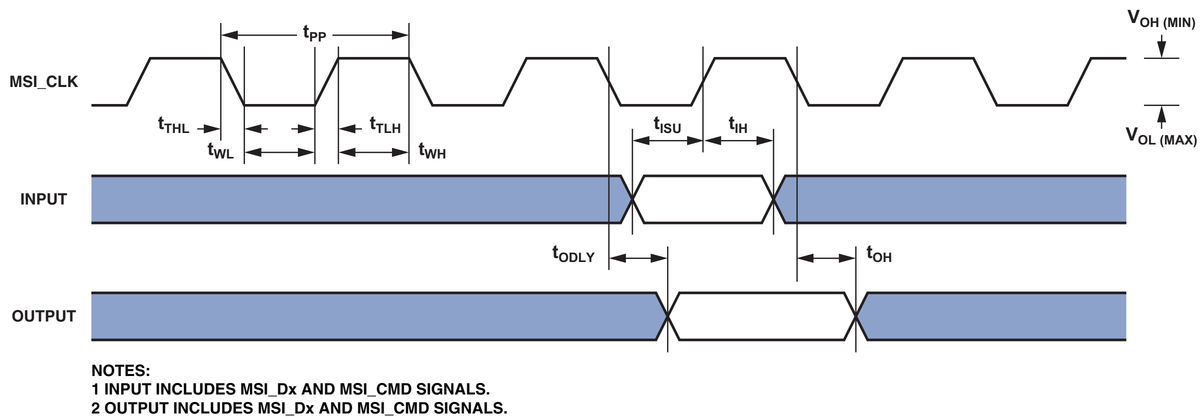

Figure 65. MSI Controller Timing

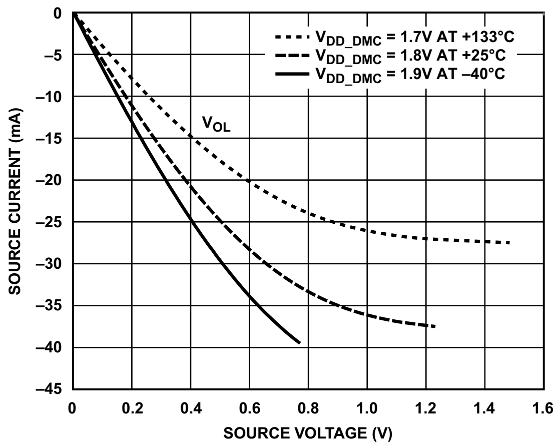

Figure 79. Driver Type B and Device Driver C (LPDDR)

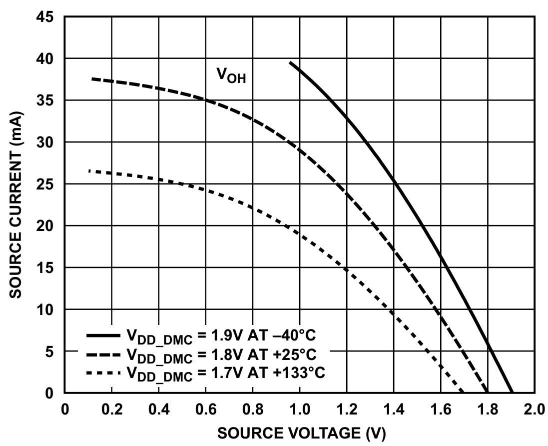

Figure 80. Driver Type B and Device Driver C (LPDDR)

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 81 shows the measurement point for ac measurements (except output enable/disable). The measurement point, V_{MEAS}, is $V_{DD\_EXT}/2$ for V_{DD_EXT} (nominal) = 3.3 V.

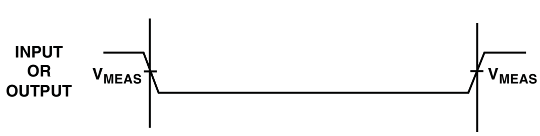

Figure 81. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered enabled when they make a transition from a high impedance state to the point when they start driving.

The output enable time, t_{ENA}, is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving, as shown on the right side of Figure 82. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

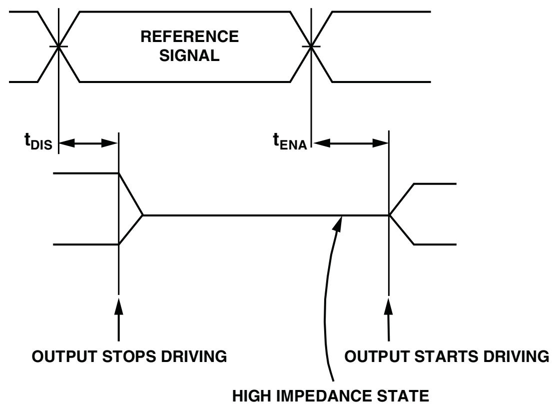

Figure 82. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered disabled when they stop driving, enter a high impedance state, and start to decay from the output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving, as shown on the left side of Figure 82).

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 83). V_{LOAD} is equal to $V_{DD\_EXT}/2$. Figure 84 through Figure 88 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in Figure 84 through Figure 88 cannot be linear outside the ranges shown.

ADSP-SC57x/ADSP-2157x 176-LEAD LQFP LEAD ASSIGNMENTS

The ADSP-SC57x/ADSP-2157x 176-Lead LQFP Lead Assignments (Numerical by Lead Number) table lists the 176-lead LQFP package by lead number.

The ADSP-SC57x/ADSP-2157x 176-Lead LQFP Lead Assignments (Alphabetical by Pin Name) table lists the 176-lead LQFP package by pin name.

ADSP-SC57x/ADSP-2157x 176-LEAD LQFP LEAD ASSIGNMENTS (NUMERICAL BY LEAD NUMBER)

Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name
01	VDD_INT	41	PD_11	81	SYS_RESOUT	121	DAI0_PIN03
02	GND	42	PD_10	82	VDD_INT	122	DAI0_PIN04
03	VDD_INT	43	PD_09	83	GND	123	DAI0_PIN01
04	PA_15	44	GND	84	VDD_EXT	124	VDD_INT
05	PA_14	45	GND	85	SYS_FAULT	125	GND
06	PA_13	46	VDD_EXT	86	SYS_BMODE0	126	VDD_EXT
07	VDD_INT	47	VDD_INT	87	SYS_BMODE1	127	DAI0_PIN02
08	PA_12	48	PD_08	88	VDD_INT	128	PB_15
09	VDD_EXT	49	PD_07	89	GND	129	VDD_INT
10	PA_10	50	PD_06	90	VDD_HADC	130	VDD_INT
11	PA_11	51	PD_05	91	HADC0_VIN0	131	GND
12	PC_15	52	VDD_INT	92	HADC0_VIN1	132	VDD_INT
13	PA_09	53	TWI0_SDA	93	HADC0_VREFN	133	GND
14	VDD_INT	54	TWI0_SCL	94	HADC0_VIN2	134	VDD_INT
15	GND	55	TWI1_SDA	95	HADC0_VIN3	135	JTG_TCK
16	VDD_INT	56	TWI1_SCL	96	HADC0_VREFP	136	JTG_TDO
17	PC_14	57	TWI2_SDA	97	GND	137	JTG_TDI
18	PC_13	58	TWI2_SCL	98	VDD_INT	138	JTG_TMS
19	PC_12	59	VDD_INT	99	GND	139	VDD_INT
20	PC_11	60	VDD_EXT	100	DAI0_PIN20	140	VDD_EXT
21	VDD_EXT	61	PD_04	101	DAI0_PIN19	141	PB_14
22	PC_10	62	PD_03	102	DAI0_PIN18	142	PB_13
23	PC_09	63	PD_02	103	VDD_INT	143	VDD_EXT
24	PC_08	64	PD_01	104	VDD_EXT	144	PB_12
25	PC_07	65	GND	105	DAI0_PIN17	145	VDD_INT
26	PC_06	66	VDD_INT	106	DAI0_PIN16	146	PB_11
27	PC_05	67	PD_00	107	DAI0_PIN15	147	VDD_EXT
28	PC_04	68	PA_08	108	DAI0_PIN14	148	PB_10
29	PC_03	69	PA_07	109	VDD_INT	149	VDD_EXT
30	VDD_INT	70	PA_06	110	DAI0_PIN13	150	VDD_INT
31	VDD_EXT	71	VDD_EXT	111	DAI0_PIN12	151	SYS_HWRST
32	PC_02	72	VDD_INT	112	DAI0_PIN11	152	VDD_EXT
33	PC_01	73	VDD_INT	113	DAI0_PIN10	153	JTG_TRST
34	PC_00	74	PA_05	114	VDD_INT	154	SYS_CLKIN0
35	PD_15	75	PA_04	115	VDD_EXT	155	SYS_XTAL0
36	PD_14	76	PA_03	116	DAI0_PIN09	156	VDD_INT
37	PD_13	77	PA_02	117	DAI0_PIN08	157	SYS_CLKOUT
38	VDD_EXT	78	VDD_EXT	118	DAI0_PIN06	158	VDD_EXT
39	VDD_INT	79	PA_01	119	DAI0_PIN07	159	PB_09
40	PD_12	80	PA_00	120	DAI0_PIN05	160	VDD_EXT

ADSP-SC57X/ADSP-2157X 176-LEAD LQFP LEAD ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.
DAI0_PIN01	123	PA_01	79	PC_15	12	VDD_EXT	149
DAI0_PIN02	127	PA_02	77	PD_00	67	VDD_EXT	152
DAI0_PIN03	121	PA_03	76	PD_01	64	VDD_EXT	158
DAI0_PIN04	122	PA_04	75	PD_02	63	VDD_EXT	160
DAI0_PIN05	120	PA_05	74	PD_03	62	VDD_EXT	164
DAI0_PIN06	118	PA_06	70	PD_04	61	VDD_EXT	167
DAI0_PIN07	119	PA_07	69	PD_05	51	VDD_EXT	171
DAI0_PIN08	117	PA_08	68	PD_06	50	VDD_HADC	90
DAI0_PIN09	116	PA_09	13	PD_07	49	VDD_INT	01
DAI0_PIN10	113	PA_10	10	PD_08	48	VDD_INT	03
DAI0_PIN11	112	PA_11	11	PD_09	43	VDD_INT	07
DAI0_PIN12	111	PA_12	08	PD_10	42	VDD_INT	14
DAI0_PIN13	110	PA_13	06	PD_11	41	VDD_INT	16
DAI0_PIN14	108	PA_14	05	PD_12	40	VDD_INT	30
DAI0_PIN15	107	PA_15	04	PD_13	37	VDD_INT	39
DAI0_PIN16	106	PB_00	174	PD_14	36	VDD_INT	47
DAI0_PIN17	105	PB_01	173	PD_15	35	VDD_INT	52
DAI0_PIN18	102	PB_02	172	SYS_BMODE0	86	VDD_INT	59
DAI0_PIN19	101	PB_03	169	SYS_BMODE1	87	VDD_INT	66
DAI0_PIN20	100	PB_04	168	SYS_CLKIN0	154	VDD_INT	72
GND	02	PB_05	166	SYS_CLKOUT	157	VDD_INT	73
GND	15	PB_06	165	SYS_FAULT	85	VDD_INT	82
GND	44	PB_07	162	SYS_HWRST	151	VDD_INT	88
GND	45	PB_08	161	SYS_RESOUT	81	VDD_INT	98
GND	65	PB_09	159	SYS_XTAL0	155	VDD_INT	103
GND	83	PB_10	148	TWI0_SCL	54	VDD_INT	109
GND	89	PB_11	146	TWI0_SDA	53	VDD_INT	114
GND	97	PB_12	144	TWI1_SCL	56	VDD_INT	124
GND	99	PB_13	142	TWI1_SDA	55	VDD_INT	129
GND	125	PB_14	141	TWI2_SCL	58	VDD_INT	130
GND	131	PB_15	128	TWI2_SDA	57	VDD_INT	132
GND	133	PC_00	34	VDD_EXT	09	VDD_INT	134
GND	176	PC_01	33	VDD_EXT	21	VDD_INT	139
GND	177[1]	PC_02	32	VDD_EXT	31	VDD_INT	145
HADC0_VIN0	91	PC_03	29	VDD_EXT	38	VDD_INT	150
HADC0_VIN1	92	PC_04	28	VDD_EXT	46	VDD_INT	156
HADC0_VIN2	94	PC_05	27	VDD_EXT	60	VDD_INT	163
HADC0_VIN3	95	PC_06	26	VDD_EXT	71	VDD_INT	170
HADC0_VREFN	93	PC_07	25	VDD_EXT	78	VDD_INT	175
HADC0_VREFP	96	PC_08	24	VDD_EXT	84		
JTG_TCK	135	PC_09	23	VDD_EXT	104		
JTG_TDI	137	PC_10	22	VDD_EXT	115		
JTG_TDO	136	PC_11	20	VDD_EXT	126		
JTG_TMS	138	PC_12	19	VDD_EXT	140		
JTG_TRST	153	PC_13	18	VDD_EXT	143		
PA_00	80	PC_14	17	VDD_EXT	147		

[1] Pin 177 is the GND supply (see Figure 91) for the processor; this pad must connect to GND.