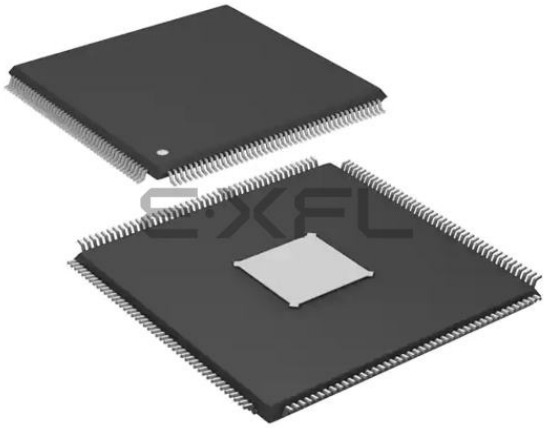

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz, 450MHz
Non-Volatile Memory	External
On-Chip RAM	1.640MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 100°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc570cswz-4

acting as either a master device or a slave device. In a multimaster environment, the SPI peripheral uses open-drain outputs to avoid data bus contention. The flow control features enable slow slave devices to interface with fast master devices by providing an SPI ready pin (SPI_RDY) which flexibly controls the transfers.

The baud rate and clock phase and polarities of the SPI port are programmable. The port has integrated DMA channels for both transmit and receive data streams.

Link Port (LP)

Two 8-bit wide link ports (LPs) for the BGA package (one link port for the LQFP package) can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional and have eight data lines, an acknowledge line, and a clock line.

ADC Control Module (ACM) Interface

The ADC control module (ACM) provides an interface that synchronizes the controls between the processors and an ADC. The analog-to-digital conversions are initiated by the processors, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

The ACM synchronizes the ADC conversion process, generating the ADC controls, the ADC conversion start signal, and other signals. The actual data acquisition from the ADC is done by an internal DAI routing of the ACM with the SPORT0 block.

The processors interface directly to many ADCs without any glue logic required.

Ethernet Media Access Controller (EMAC)

The processor features an ethernet media access controller (EMAC): 10/100/1000 AVB Ethernet with precision time protocol (IEEE 1588).

The processors can directly connect to a network through embedded fast EMAC that supports 10Base-T (10 Mb/sec), 100Base-T (100 Mb/sec) and 1000Base-T (1 Gb/sec) operations.

Some standard features of the EMAC are as follows:

- Support and MII/RMII/RGMII protocols for external PHYs.
- RGMII support for the BGA package only
- Full-duplex and half-duplex modes
- Media access management (in half-duplex operation)
- Flow control
- Station management, including the generation of MDC/MDIO frames for read/write access to PHY registers

Some advanced features of the EMAC include the following:

- Automatic checksum computation of IP header and IP payload fields of receive frames
- Independent 32-bit descriptor driven receive and transmit DMA channels
- Frame status delivery to memory through DMA, including frame completion semaphores for efficient buffer queue management in software
- Transmit DMA support for separate descriptors for MAC header and payload fields to eliminate buffer copy operations
- Convenient frame alignment modes
- 47 MAC management statistics counters with selectable clear on read behavior and programmable interrupts on half maximum value
- Advanced power management
- Magic packet detection and wakeup frame filtering
- Support for 802.3Q tagged VLAN frames
- Programmable MDC clock rate and preamble suppression

Audio Video Bridging (AVB) Support

The 10/100/1000 EMAC supports the following audio video bridging (AVB) features:

- Separate channels or queues for AV data transfer in 100 Mbps and 1000 Mbps modes)
- IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for the additional transmit channels
- Configuring up to two additional channels (Channel 1 and Channel 2) on the transmit and receive paths for AV traffic. Channel 0 is available by default and carries the legacy best effort Ethernet traffic on the transmit side.
- Separate DMA, transmit and receive FIFO for AVB latency class
- Programmable control to route received VLAN tagged non AV packets to channels or queues

Precision Time Protocol (PTP) IEEE 1588 Support

The IEEE 1588 standard is a precision clock synchronization protocol for networked measurement and control systems. The processors include hardware support for IEEE 1588 with an integrated precision time protocol synchronization engine (PTP_TSYNC).

This engine provides hardware assisted time stamping to improve the accuracy of clock synchronization between PTP nodes. The main features of the engine include the following:

- Support for both IEEE 1588-2002 and IEEE 1588-2008 protocol standards
- Hardware assisted time stamping capable of up to 12.5 ns resolution
- Lock adjustment
- Automatic detection of IPv4 and IPv6 packets, as well as PTP messages
- Multiple input clock sources (SCLK0, RGMII, RMII, MII clock, and external clock)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

Table 11. ADSP-SC57x/ADSP-2157x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
SPT_BD1	InOut	**Channel B Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BFS	InOut	**Channel B Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SYS_BMODE[n]	Input	**Boot Mode Control n.** Selects the boot mode of the processor.
SYS_CLKIN0	Input	**Clock/Crystal Input.**
SYS_CLKIN1	Input	**Clock/Crystal Input**.
SYS_CLKOUT	Output	**Processor Clock Output.** Outputs internal clocks. Clocks may be divided down. See the CGU chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for more details.
SYS_FAULT	InOut	**Active-High Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_FAULT}}$	InOut	**Active-Low Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control.** Resets the device when asserted.
$\overline{\text{SYS\_RESOUT}}$	Output	**Reset Output.** Indicates the device is in the reset state.
SYS_XTAL0	Output	**Crystal Output.**
SYS_XTAL1	Output	**Crystal Output.**
TM_ACI[n]	Input	**Alternate Capture Input n.** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TM_ACLK[n]	Input	**Alternate Clock n.** Provides an additional time base for an individual timer.
TM_CLK	Input	**Clock.** Provides an additional global time base for all GP timers.
TM_TMR[n]	InOut	**Timer n.** The main input/output signal for each timer.
TRACE_CLK	Output	**Trace Clock.** Clock output.
TRACE_D[nn]	Output	**Trace Data n.** Unidirectional data bus.
TWI_SCL	InOut	**Serial Clock.** Clock output when master, clock input when slave.
TWI_SDA	InOut	**Serial Data.** Receives or transmits data.
$\overline{\text{UART\_CTS}}$	Input	**Clear to Send.** Flow control signal.
$\overline{\text{UART\_RTS}}$	Output	**Request to Send.** Flow control signal.
$\overline{\text{UART\_RX}}$	Input	**Receive.** Receives input. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
$\overline{\text{UART\_TX}}$	Output	**Transmit.** Transmits output. Typically connects to a transceiver that meets the electrical requirements of the device being communicated with.
USB_CLKIN	Input	**Clock/Crystal Input.** This clock input is multiplied by a PLL to form the USB clock. See data sheet specifications for frequency/tolerance information.
USB_DM	InOut	**Data –.** Bidirectional differential data line.
USB_DP	InOut	**Data +.** Bidirectional differential data line.
USB_ID	Input	**OTG ID.** Senses whether the controller is a host or device. This signal is pulled low when an A type plug is sensed (signifying that the USB controller is the A device). The input is high when a B type plug is sensed (signifying that the USB controller is the B device).
USB_VBC	Output	**VBUS Control.** Controls an external voltage source to supply VBUS when in host mode. Can be configured as open-drain. Polarity is configurable as well.
USB_VBUS	InOut	**Bus Voltage.** Connects to bus voltage in host and device modes.
USB_XTAL	Output	**Crystal.** Drives an external crystal. Must be left unconnected if an external clock is driving USB_CLKIN.

Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DAI0_PIN16	DAI0 Pin 16	Not Muxed	DAI0_PIN16
DAI0_PIN17	DAI0 Pin 17	Not Muxed	DAI0_PIN17
DAI0_PIN18	DAI0 Pin 18	Not Muxed	DAI0_PIN18
DAI0_PIN19	DAI0 Pin 19	Not Muxed	DAI0_PIN19
DAI0_PIN20	DAI0 Pin 20	Not Muxed	DAI0_PIN20
DMC0_A00	DMC0 Address 0	Not Muxed	DMC0_A00
DMC0_A01	DMC0 Address 1	Not Muxed	DMC0_A01
DMC0_A02	DMC0 Address 2	Not Muxed	DMC0_A02
DMC0_A03	DMC0 Address 3	Not Muxed	DMC0_A03
DMC0_A04	DMC0 Address 4	Not Muxed	DMC0_A04
DMC0_A05	DMC0 Address 5	Not Muxed	DMC0_A05
DMC0_A06	DMC0 Address 6	Not Muxed	DMC0_A06
DMC0_A07	DMC0 Address 7	Not Muxed	DMC0_A07
DMC0_A08	DMC0 Address 8	Not Muxed	DMC0_A08
DMC0_A09	DMC0 Address 9	Not Muxed	DMC0_A09
DMC0_A10	DMC0 Address 10	Not Muxed	DMC0_A10
DMC0_A11	DMC0 Address 11	Not Muxed	DMC0_A11
DMC0_A12	DMC0 Address 12	Not Muxed	DMC0_A12
DMC0_A13	DMC0 Address 13	Not Muxed	DMC0_A13
DMC0_A14	DMC0 Address 14	Not Muxed	DMC0_A14
DMC0_A15	DMC0 Address 15	Not Muxed	DMC0_A15
DMC0_BA0	DMC0 Bank Address Input 0	Not Muxed	DMC0_BA0
DMC0_BA1	DMC0 Bank Address Input 1	Not Muxed	DMC0_BA1
DMC0_BA2	DMC0 Bank Address Input 2	Not Muxed	DMC0_BA2
$\overline{\text{DMC0\_CAS}}$	DMC0 Column Address Strobe	Not Muxed	$\overline{\text{DMC0\_CAS}}$
DMC0_CK	DMC0 Clock	Not Muxed	DMC0_CK
$\overline{\text{DMC0\_CK}}$	DMC0 Clock (complement)	Not Muxed	$\overline{\text{DMC0\_CK}}$
DMC0_CKE	DMC0 Clock enable	Not Muxed	DMC0_CKE
$\overline{\text{DMC0\_CS0}}$	DMC0 Chip Select 0	Not Muxed	$\overline{\text{DMC0\_CS0}}$
DMC0_DQ00	DMC0 Data 0	Not Muxed	DMC0_DQ00
DMC0_DQ01	DMC0 Data 1	Not Muxed	DMC0_DQ01
DMC0_DQ02	DMC0 Data 2	Not Muxed	DMC0_DQ02
DMC0_DQ03	DMC0 Data 3	Not Muxed	DMC0_DQ03
DMC0_DQ04	DMC0 Data 4	Not Muxed	DMC0_DQ04
DMC0_DQ05	DMC0 Data 5	Not Muxed	DMC0_DQ05
DMC0_DQ06	DMC0 Data 6	Not Muxed	DMC0_DQ06
DMC0_DQ07	DMC0 Data 7	Not Muxed	DMC0_DQ07
DMC0_DQ08	DMC0 Data 8	Not Muxed	DMC0_DQ08
DMC0_DQ09	DMC0 Data 9	Not Muxed	DMC0_DQ09
DMC0_DQ10	DMC0 Data 10	Not Muxed	DMC0_DQ10
DMC0_DQ11	DMC0 Data 11	Not Muxed	DMC0_DQ11
DMC0_DQ12	DMC0 Data 12	Not Muxed	DMC0_DQ12
DMC0_DQ13	DMC0 Data 13	Not Muxed	DMC0_DQ13
DMC0_DQ14	DMC0 Data 14	Not Muxed	DMC0_DQ14
DMC0_DQ15	DMC0 Data 15	Not Muxed	DMC0_DQ15
DMC0_LDM	DMC0 Data Mask for Lower Byte	Not Muxed	DMC0_LDM
DMC0_LDQS	DMC0 Data Strobe for Lower Byte	Not Muxed	DMC0_LDQS
$\overline{\text{DMC0\_LDQS}}$	DMC0 Data Strobe for Lower Byte (complement)	Not Muxed	$\overline{\text{DMC0\_LDQS}}$

Table 17. Signal Multiplexing for Port E (Continued)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_03	LP0_ACK				
PE_04	LP0_D0				
PE_05	LP0_D1				
PE_06	LP0_D2				
PE_07	LP0_D3				
PE_08	LP0_D4				
PE_09	LP0_D5				
PE_10	LP0_D6				
PE_11	LP0_D7				
PE_12	MSI0_D0		TM0_TMR0		
PE_13	MSI0_D1	C1_FLG0	CNT0_UD		
PE_14	MSI0_D2	$\overline{\text{UART1\_CTS}}$	TM0_TMR6		
PE_15	MSI0_D3	C2_FLG3			

Table 18. Signal Multiplexing for Port F

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PF_00	MSI0_D4	TRACE0_D00			
PF_01	MSI0_D5	TRACE0_D01			
PF_02	MSI0_D6	TRACE0_D02			
PF_03	MSI0_D7	TRACE0_D03			
PF_04	MSI0_CLK	C1_FLG2	$\overline{\text{SPI0\_SEL6}}$		
PF_05	ETH0_PTPCLKIN0	TM0_TMR1	$\overline{\text{SPI0\_SEL5}}$		
PF_06	ETH0_PTPAUXIN2	TRACE0_CLK			TM0_ACLK1
PF_07	ETH0_PTPAUXIN3	TM0_TMR2	MSI0_CMD		
PF_08	$\overline{\text{UART0\_TX}}$				
PF_09	$\overline{\text{UART0\_RX}}$				TM0_ACI0
PF_10	$\overline{\text{UART1\_TX}}$	$\overline{\text{SPI2\_SEL2}}$			
PF_11	$\overline{\text{UART1\_RX}}$	ACM0_A0	$\overline{\text{SPI1\_SEL3}}$	C2_FLG2	TM0_ACI1

Table 19 shows the internal timer signal routing. This table applies to both the 400-ball CSP_BGA and 176-lead LQFP packages.

Table 19. Internal Timer Signal Routing

Timer Input Signal	Internal Source
TM0_ACLK0[1]	SYS_CLKIN1
TM0_ACI5	DAI0_PB04_O
TM0_ACLK5	DAI0_PB03_O
TM0_ACI6	DAI0_PB20_O
TM0_ACLK6	DAI0_PB19_O
TM0_ACI7	CNT0_TO
TM0_ACLK7	SYS_CLKIN0

[1] Not applicable for LQFP package.

GPIO MULTIPLEXING FOR 176-LEAD LQFP PACKAGE

Table 21 through Table 24 identify the pin functions that are multiplexed on the GPIO pins of the 176-lead LQFP package.

Table 21. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00	TRACE0_CLK				TM0_ACLK1
PA_01	TRACE0_D00				
PA_02	TRACE0_D01				
PA_03	TRACE0_D02				
PA_04	TRACE0_D03				
PA_05	UART0_TX				
PA_06	UART0_RX				TM0_ACI0
PA_07	UART1_TX	SPI2_SEL2			
PA_08	UART1_RX	ACM0_A0	SPI1_SEL3		TM0_ACI1
PA_09	ETH0_PTPPPS0	LP1_D6	SPI0_SEL4		
PA_10	ETH0_MDIO	UART2_RTS	SPI2_SEL6		
PA_11	ETH0_MDC	UART2_CTS			
PA_12	ETH0_RXD1				
PA_13	ETH0_RXD0				
PA_14	ETH0_RXD2	ACM0_A3	SPI1_SEL4		
PA_15	ETH0_RXD3	ACM0_T0	SPI2_SEL5		

Table 22. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	ETH0_RXCLK_REFCLK	C2_FLG0			
PB_01	ETH0_CRS	ACM0_A4	LP1_ACK	TM0_TMR3	
PB_02	ETH0_RXCTL_RXDV		SPI1_SEL5		
PB_03	ETH0_RXERR	MLB0_CLKOUT	LP1_CLK	TM0_TMR4	
PB_04	ETH0_TXCLK	MLB0_DAT			
PB_05	ETH0_TXD3	MLB0_SIG			
PB_06	ETH0_TXD2	MLB0_CLK			
PB_07	ETH0_TXD0		SPI2_SEL7		
PB_08	ETH0_TXD1				
PB_09	ETH0_TXCTL_TXEN				
PB_10	SPI2_MISO				
PB_11	SPI2_MOSI				
PB_12	SPI2_D2				
PB_13	SPI2_D3				
PB_14	SPI2_CLK				
PB_15	SPI2_SEL1				SPI2_SS

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
PB_10	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 10 Notes: Connect to VDD_EXT or GND if not used
PB_11	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 11 Notes: Connect to VDD_EXT or GND if not used
PB_12	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 12 Notes: Connect to VDD_EXT or GND if not used
PB_13	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 13 Notes: Connect to VDD_EXT or GND if not used
PB_14	InOut	H	none	none	VDD_EXT	Desc: PORTB Position 14 Notes: Connect to VDD_EXT or GND if not used
PB_15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTB Position 15 Notes: See note[2]
PC_00	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 0 Notes: See note[2]
PC_01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 1 Notes: See note[2]
PC_02	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 2 Notes: See note[2]
PC_03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 3 Notes: See note[2]
PC_04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 4 Notes: See note[2]
PC_05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 5 Notes: See note[2]
PC_06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 6 Notes: See note[2]
PC_07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 7 Notes: See note[2]
PC_08	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 8 Notes: See note[2]
PC_09	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 9 Notes: See note[2]
PC_10	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 10 Notes: See note[2]
PC_11	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 11 Notes: See note[2]
PC_12	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 12 Notes: See note[2]
PC_13	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 13 Notes: See note[2]
PC_14	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 14 Notes: See note[2]
PC_15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTC Position 15 Notes: See note[2]

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
USB0_VBC	InOut	E	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: Add external pull-down if not used[6]
USB0_VBUS	InOut	G	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: Connect to GND when USB is not used[6]
USB0_CLKIN	a		none	none	VDD_USB	Desc: USB0/USB1 Clock/Crystal Input Notes: Connect to GND when USB is not used[6]
USB0_XTAL	a		none	none	VDD_USB	Desc: USB0/USB1 Crystal Notes: No notes
VDD_DMC	s		none	none		Desc: DMC VDD Notes: No notes
VDD_EXT	s		none	none		Desc: External Voltage Domain Notes: No notes
VDD_HADC	s		none	none		Desc: HADC/TMU VDD Notes: Can be left floating if HADC and TMU are not used
VDD_INT	s		none	none		Desc: Internal Voltage Domain Notes: No notes
VDD_USB	s		none	none		Desc: USB VDD Notes: Connect to VDD_EXT when USB is not used

[1] Disabled by default.

[2] Input by default. When unused, terminate externally in hardware or enable the internal pull-up resistor (when applicable) in software. When present, the internal pull-up design holds the internal path from the pins at the expected logic levels. To pull up the external pads to the expected logic levels, use external resistors..

[3] Enabled by default.

[4] All HADC0_VINx pins can be connected directly to GND if HADC and TMU are not used.

[5] Actively driven by processor otherwise.

[6] Guidance also applies to models that do not feature the associated hardware block. See Table 2 or Table 3 for further information.

DDR3 SDRAM Read Cycle Timing

Table 50 and Figure 17 show mobile DDR3 SDRAM read cycle timing, related to the DMC.

Table 50. DDR3 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.5 V

Parameter		450 MHz[1]		Unit
		Min	Max	
Timing Requirements				
t_{DQSQ}	DMC0_DQS to DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQ Signals		0.15	ns
t_{QH}	DMC0_DQ, DMC0_DQS Output Hold Time From DMC0_DQS	0.38		t_{CK}
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.3		t_{CK}

[1] To ensure proper operation of the DDR3, all the DDR3 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

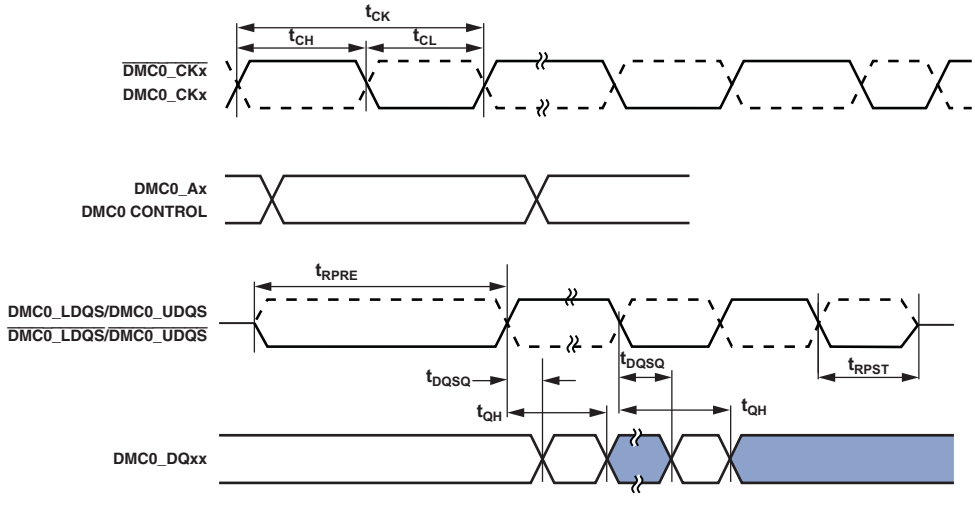

Figure 17. DDR3 SDRAM Controller Input AC Timing

Enhanced Parallel Peripheral Interface (EPPI) Timing

Table 52 and Table 53 and Figure 19 through Figure 27 describe enhanced parallel peripheral interface (EPPI) timing operations. In Figure 19 through Figure 27, POLC[1:0] represents the setting of the EPPI_CTL register, which sets the sampling/driving edges of the EPPI clock.

When internally generated, the programmed PPI clock ($f_{PCLKPROG}$) frequency in megahertz is set by the following equation where VALUE is a field in the EPPI_CLKDIV register that can be set from 0 to 65535:

$$f_{PCLKPROG} = \frac{f_{SCLK0}}{(VALUE + 1)}$$

$$t_{PCLKPROG} = \frac{1}{f_{PCLKPROG}}$$

When externally generated, the EPPI_CLK is called $f_{PCLKEXT}$:

$$t_{PCLKEXT} = \frac{1}{f_{PCLKEXT}}$$

Table 52. Enhanced Parallel Peripheral Interface (EPPI)—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSPI}	External FS Setup Before EPPI_CLK	6.5		ns
t_{HFSPI}	External FS Hold After EPPI_CLK	0		ns
t_{SDRPI}	Receive Data Setup Before EPPI_CLK	6.5		ns
t_{HDRPI}	Receive Data Hold After EPPI_CLK	0		ns
t_{SFS3GI}	External FS3 Input Setup Before EPPI_CLK Fall Edge in Clock Gating Mode	14		ns
t_{HFS3GI}	External FS3 Input Hold Before EPPI_CLK Fall Edge in Clock Gating Mode	0		ns
Switching Characteristics				
t_{PCLKW}	EPPI_CLK Width[1]	$0.5 \times t_{PCLKPROG} - 1.5$		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKPROG} - 1.5$		ns
t_{DFSPI}	Internal FS Delay After EPPI_CLK		3.6	ns
t_{HOFSPI}	Internal FS Hold After EPPI_CLK	–0.72		ns
t_{DDTPI}	Transmit Data Delay After EPPI_CLK		3.5	ns
t_{HDTPI}	Transmit Data Hold After EPPI_CLK	–0.5		ns

[1] See Table 27 for details on the minimum period that can be programmed for $t_{PCLKPROG}$.

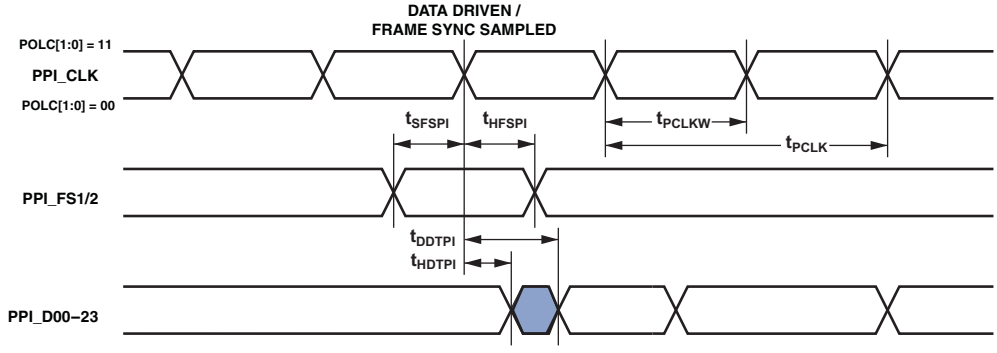

Figure 22. EPPI Internal Clock GP Transmit Mode with External Frame Sync Timing

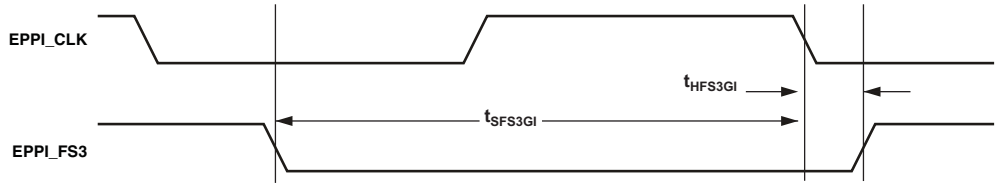

Figure 23. Clock Gating Mode with Internal Clock and External Frame Sync Timing

Asynchronous Sample Rate Converter (ASRC)—Serial Input Port

The ASRC input signals are routed from the DAI0_PINx pins using the SRU. Therefore, the timing specifications provided in Table 61 are valid at the DAI0_PINx pins.

Table 61. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$t_{SCLK0} - 1$		ns
t_{SRCCLK}	Clock Period	$2 \times t_{SCLK0}$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

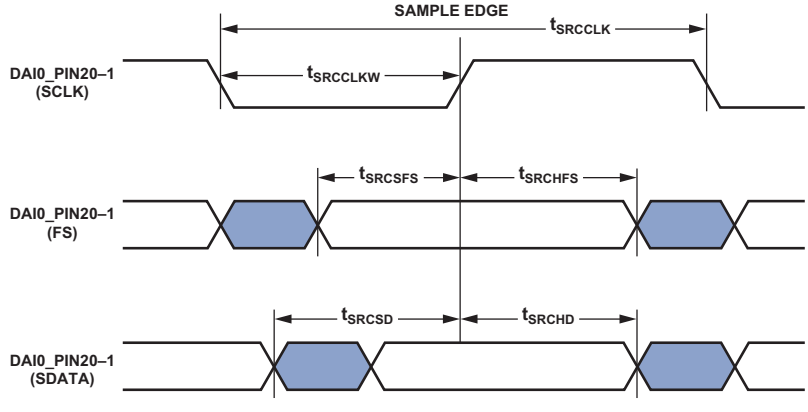

Figure 34. ASRC Serial Input Port Timing

SPI Port—Slave Timing

SPI0, SPI1, and SPI2

Table 65, Table 66, and Figure 37 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPIx_MOSI signal is also an output.
- In quad-mode data transmit, the SPIx_MOSI, SPIx_D2, and SPIx_D3 signals are also outputs.
- In dual-mode data receive, the SPIx_MISO signal is also an input.
- In quad-mode data receive, the SPIx_MISO, SPIx_D2, and SPIx_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

- Quad mode is supported by SPI2 only.
- CPHA is a configuration bit in the SPI_CTL register.

Table 65. SPI0, SPI1 Port—Slave Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	SPIx_CLK High Period[2]	$0.5 \times t_{SPICLKEXT} - 1.5$		ns
t_{SPICLS}	SPIx_CLK Low Period[2]	$0.5 \times t_{SPICLKEXT} - 1.5$		ns
t_{SPICLK}	SPIx_CLK Period[2]	$t_{SPICLKEXT} - 1.5$		ns
t_{HDS}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	$t_{SPICLKEXT} - 1.5$		ns
t_{SDSCI}	$\overline{\text{SPIx\_SS}}$ Assertion to First SPIx_CLK Edge	11.7		ns
t_{SSPID}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPIx_CLK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIx\_SS}}$ Assertion to Data Out Active	0	14.12	ns
t_{DSDHI}	$\overline{\text{SPIx\_SS}}$ Deassertion to Data High Impedance	0	12.6	ns
t_{DDSPID}	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		14.16	ns
t_{HDSPID}	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	1.5		ns

[1] All specifications apply to SPI0 and SPI1.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx_CLK. For the external SPIx_CLK ideal maximum frequency, see the $f_{SPICLKTEXT}$ specification in Table 27.

SPI Port—SPIx_RDY Slave Timing

SPIx_RDY provides flow control. CPOL, CPHA, and FCCH are configuration bits in the SPIx_CTL register.

Table 67. SPI Port—SPIx_RDY Slave Timing[1]

Parameter	Conditions	Min	Max	Unit
Switching Characteristic				
$t_{DSPISCKRDYS}$ SPIx_RDY Deassertion from Last Valid Input SPIx_CLK Edge	FCCH = 0	$3 \times t_{SCLK1}$	$4 \times t_{SCLK1} + 10$	ns
	FCCH = 1	$4 \times t_{SCLK1}$	$5 \times t_{SCLK1} + 10$	ns

[1] All specifications apply to all three SPIs.

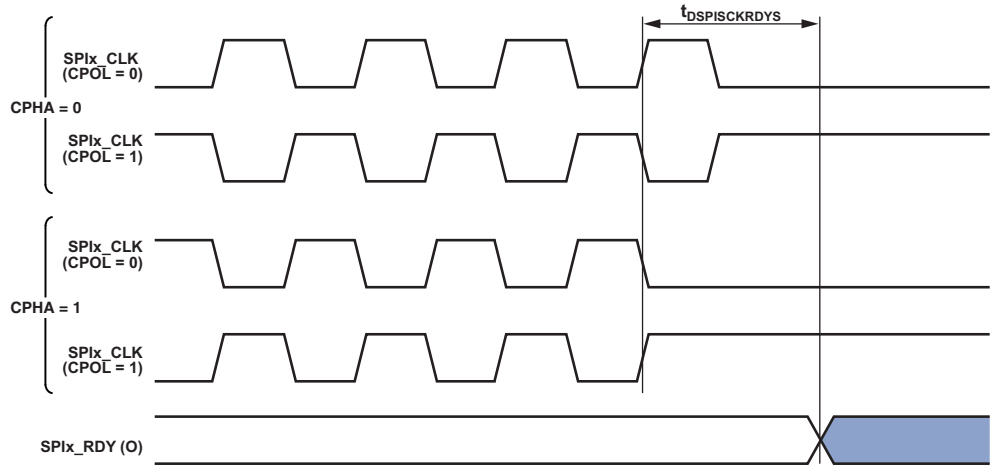

Figure 38. SPIx_RDY Deassertion from Valid Input SPIx_CLK Edge in Slave Mode

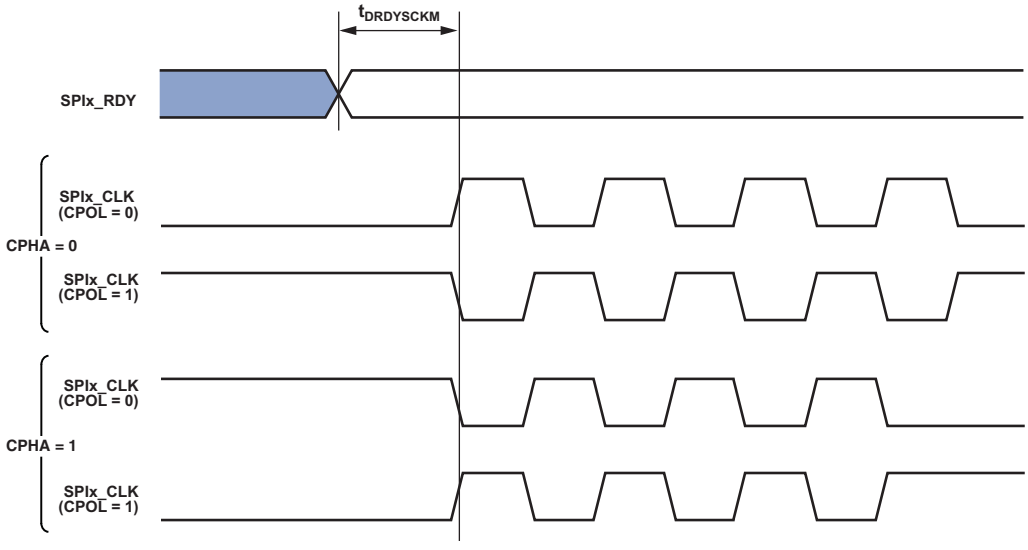

Figure 42. SPIx_CLK Switching Diagram after SPIx_RDY Assertion

Precision Clock Generator (PCG) (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes inputs directly from the DAI pins (via pin buffers) and sends outputs directly to the DAI pins. For the other cases, where the PCG inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI0_PINx).

Table 71. PCG (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{SCLK} \times 2$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	13.5	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$13.5 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$[1]	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$13.5 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[2]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

[1] D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference.
[2] Normal mode of operation.

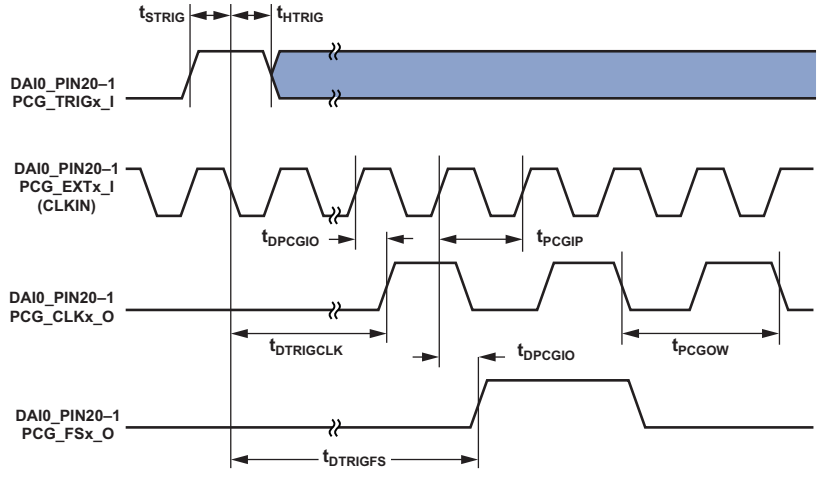

Figure 43. PCG (Direct Pin Routing)

Table 81. 10/100 EMAC Timing—RMII Receive Signal

Parameter[1]		Min	Max	Unit
Timing Requirements				
$t_{REFCLKF}$	ETH0_RXCLK_REFCLK Frequency (f_{SCLK0} = SCLK0 Frequency)	None	50 + 1%	MHz
$t_{REFCLKW}$	ETH0_RXCLK_REFCLK Width ($t_{REFCLKF}$ = ETH0_RXCLK_REFCLK Period)	$t_{REFCLK} \times 35\%$	$t_{REFCLK} \times 65\%$	ns
$t_{REFCLKIS}$	Rx Input Valid to RMII ETH0_RXCLK_REFCLK Rising Edge (Data In Setup)	1.75		ns
$t_{REFCLKIH}$	RMII ETH0_RXCLK_REFCLK Rising Edge to Rx Input Invalid (Data In Hold)	1.6		ns

[1] RMII inputs synchronous to RMII ETH0_RXCLK_REFCLK are ETH0_RXD1–0, RMII ETH0_RXCTL_RXDV, and ETH0_RXERR.

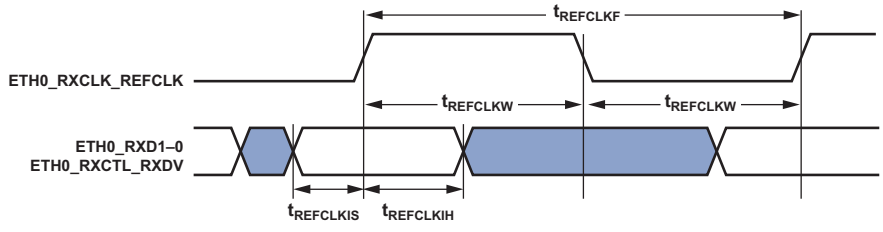

Figure 51. 10/100 EMAC Controller Timing—RMII Receive Signal

Table 82. 10/100 EMAC Timing—RMII Transmit Signal

Parameter[1]		Min	Max	Unit
Switching Characteristics				
$t_{REFCLKOV}$	RMII ETH0_RXCLK_REFCLK Rising Edge to Transmit Output Valid (Data Out Valid)		11.9	ns
$t_{REFCLKOH}$	RMII ETH0_RXCLK_REFCLK Rising Edge to Transmit Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII ETH0_RXCLK_REFCLK are ETH0_TXD1–0.

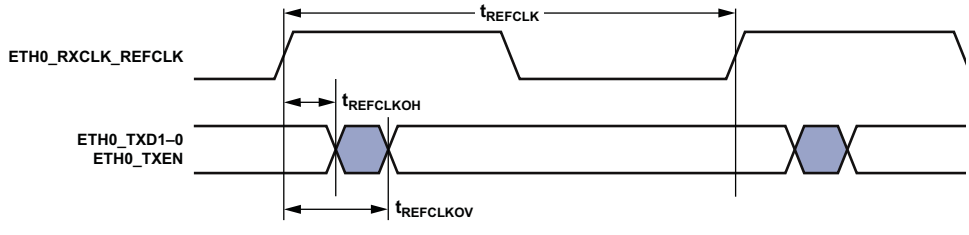

Figure 52. 10/100 EMAC Controller Timing—RMII Transmit Signal

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 88. Input signals are routed to the DAI0_PINx pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI0_PINx pins.

Table 88. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

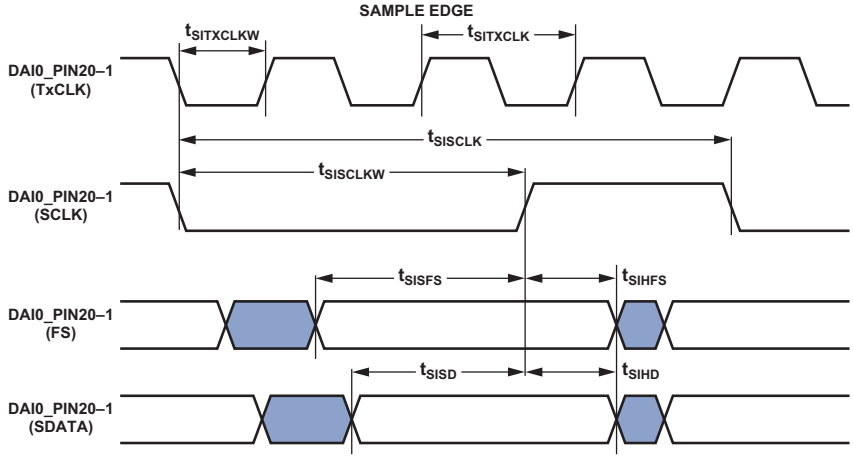

Figure 58. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 89. Oversampling Clock (TxCLK) Switching Characteristics

Parameter		Max	Unit
Switching Characteristics			
f_{TXCLK_384}	Frequency for TxCLK = 384 × Frame Sync	Oversampling ratio × frame sync ≤ $1/t_{SITXCLK}$	MHz
f_{TXCLK_256}	Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
f_{FS}	Frame Rate (FS)	192.0	kHz

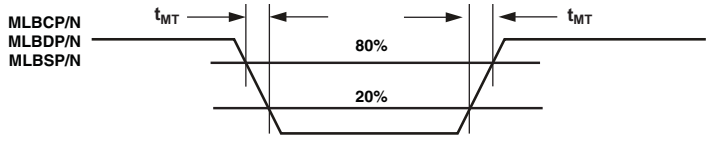

Figure 61. MLB 6-Pin Transition Time

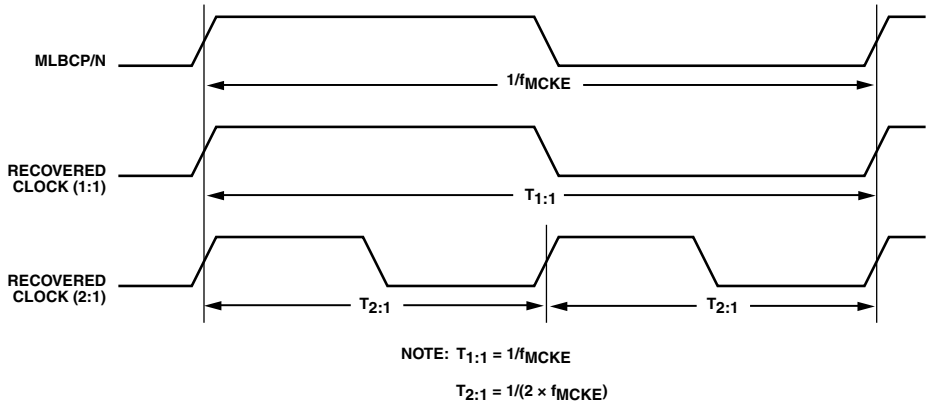

Figure 62. MLB 6-Pin Clock Definitions

Debug Interface (JTAG Emulation Port) Timing

Table 95 and Figure 67 provide I/O timing related to the debug interface (JTAG Emulator Port).

Table 95. JTAG Emulation Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	JTG_TCK Period	20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	12		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (measured in JTG_TCK cycles)[2]	4		T_{CK}
Switching Characteristics				
t_{DTDO}	JTG_TDO Delay From JTG_TCK Low		13.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		17	ns

[1] System Inputs = MLB0_CLKP, MLB0_DATP, MLB0_SIGP, DAI0_PIN20-01, DMC0_A15-0, DMC0_DQ15-0, $\overline{\text{DMC0\_RESET}}$, PA_15-0, PB_15-0, PC_15-0, PD_15-0, PE_15-0, PF_11-0, SYS_BMODE2-0, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$, TWI2-0_SCL, TWI2-0_SDA2.

[2] 50 MHz maximum.

[3] System Outputs = DMC0_A15-0, DMC0_BA2-0, $\overline{\text{DMC0\_CAS}}$, DMC0_CK, DMC0_CKE, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ15-0, DMC0_LDM, DMC0_LDQS, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_RESET}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0\_WE}}$, MLB0_DATP, MLB0_SIGP, PA_15-0, PB_15-0, PC_15-0, PD_15-0, PE_15-0, PF_11-0, SYS_BMODE2-0, SYS_CLKOUT, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$.

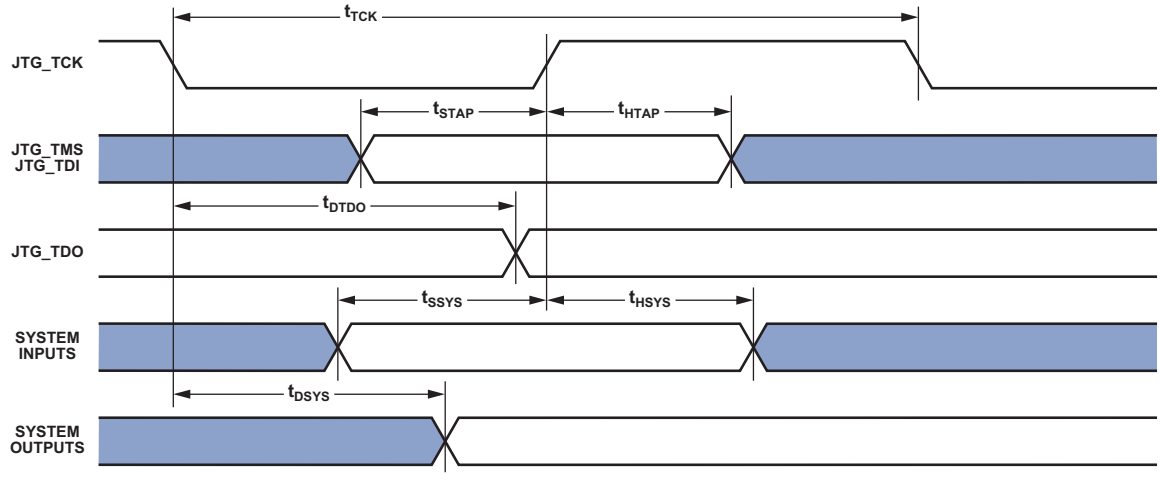

Figure 67. JTAG Port Timing

CONFIGURATION OF THE 176-LEAD LQFP LEAD CONFIGURATION

Figure 90 shows the top view of the 176-lead LQFP lead configuration and Figure 91 shows the bottom view of the 176-lead LQFP lead configuration.

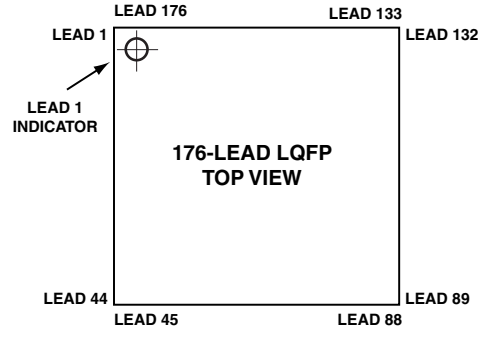

Figure 90. 176-Lead LQFP Lead Configuration (Top View)

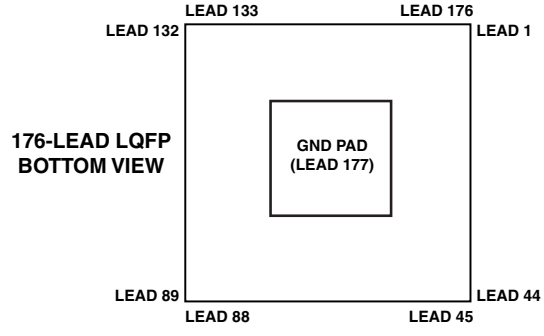

Figure 91. 176-Lead LQFP Lead Configuration (Bottom View)