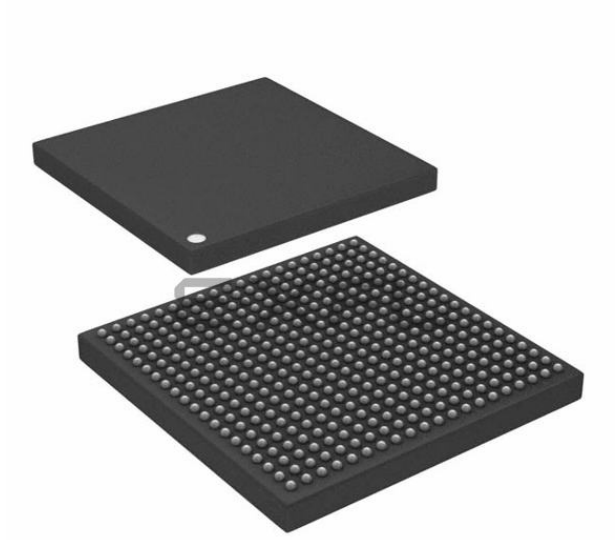

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz, 225MHz
Non-Volatile Memory	External
On-Chip RAM	1.640MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 100°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc572cbcz-42

GPIO MULTIPLEXING FOR 400-BALL CSP_BGA PACKAGE

Table 13 through Table 18 identify the pin functions that are multiplexed on the GPIO pins of the 400-ball CSP_BGA package.

Table 13. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00					
PA_01					
PA_02					
PA_03					
PA_04					
PA_05					
PA_06					
PA_07					
PA_08					
PA_09	ETH0_PTPPPS0	LP1_D6	$\overline{\text{SPI0\_SEL4}}$		
PA_10	ETH0_MDIO	$\overline{\text{UART2\_RTS}}$	$\overline{\text{SPI2\_SEL6}}$		
PA_11	ETH0_MDC	$\overline{\text{UART2\_CTS}}$			
PA_12	ETH0_RXD1				
PA_13	ETH0_RXD0				
PA_14	ETH0_RXD2	ACM0_A3	$\overline{\text{SPI1\_SEL4}}$		
PA_15	ETH0_RXD3	ACM0_T0	$\overline{\text{SPI2\_SEL5}}$		

Table 14. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	ETH0_RXCLK_REFCLK	C2_FLG0			
PB_01	ETH0_CRS	ACM0_A4	LP1_ACK	TM0_TMR3	
PB_02	ETH0_RXCTL_RXDV		$\overline{\text{SPI1\_SEL5}}$		
PB_03	ETH0_RXERR	MLB0_CLKOUT	LP1_CLK	TM0_TMR4	
PB_04	ETH0_TXCLK	MLB0_DAT			
PB_05	ETH0_TXD3	MLB0_SIG			
PB_06	ETH0_TXD2	MLB0_CLK			
PB_07	ETH0_TXD0		$\overline{\text{SPI2\_SEL7}}$		
PB_08	ETH0_TXD1				
PB_09	ETH0_TXCTL_TXEN				
PB_10	SPI2_MISO				
PB_11	SPI2_MOSI				
PB_12	SPI2_D2				
PB_13	SPI2_D3				
PB_14	SPI2_CLK				
PB_15	$\overline{\text{SPI2\_SEL1}}$				$\overline{\text{SPI2\_SS}}$

Table 17. Signal Multiplexing for Port E (Continued)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_03	LP0_ACK				
PE_04	LP0_D0				
PE_05	LP0_D1				
PE_06	LP0_D2				
PE_07	LP0_D3				
PE_08	LP0_D4				
PE_09	LP0_D5				
PE_10	LP0_D6				
PE_11	LP0_D7				
PE_12	MSI0_D0		TM0_TMR0		
PE_13	MSI0_D1	C1_FLG0	CNT0_UD		
PE_14	MSI0_D2	$\overline{\text{UART1\_CTS}}$	TM0_TMR6		
PE_15	MSI0_D3	C2_FLG3			

Table 18. Signal Multiplexing for Port F

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PF_00	MSI0_D4	TRACE0_D00			
PF_01	MSI0_D5	TRACE0_D01			
PF_02	MSI0_D6	TRACE0_D02			
PF_03	MSI0_D7	TRACE0_D03			
PF_04	MSI0_CLK	C1_FLG2	$\overline{\text{SPI0\_SEL6}}$		
PF_05	ETH0_PTPCLKIN0	TM0_TMR1	$\overline{\text{SPI0\_SEL5}}$		
PF_06	ETH0_PTPAUXIN2	TRACE0_CLK			TM0_ACLK1
PF_07	ETH0_PTPAUXIN3	TM0_TMR2	MSI0_CMD		
PF_08	$\overline{\text{UART0\_TX}}$				
PF_09	$\overline{\text{UART0\_RX}}$				TM0_ACI0
PF_10	$\overline{\text{UART1\_TX}}$	$\overline{\text{SPI2\_SEL2}}$			
PF_11	$\overline{\text{UART1\_RX}}$	ACM0_A0	$\overline{\text{SPI1\_SEL3}}$	C2_FLG2	TM0_ACI1

Table 19 shows the internal timer signal routing. This table applies to both the 400-ball CSP_BGA and 176-lead LQFP packages.

Table 19. Internal Timer Signal Routing

Timer Input Signal	Internal Source
TM0_ACLK0[1]	SYS_CLKIN1
TM0_ACI5	DAI0_PB04_O
TM0_ACLK5	DAI0_PB03_O
TM0_ACI6	DAI0_PB20_O
TM0_ACLK6	DAI0_PB19_O
TM0_ACI7	CNT0_TO
TM0_ACLK7	SYS_CLKIN0

[1] Not applicable for LQFP package.

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
HADC0_VIN7	a	NA	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 7 Notes: Connect to GND through a resistor if not used[4]
HADC0_VREFN	s	NA	none	none	VDD_HADC	Desc: HADC0 Ground Reference for ADC Notes: Connect to GND if HADC and TMU are not used
HADC0_VREFP	s	NA	none	none	VDD_HADC	Desc: HADC0 External Reference for ADC Notes: No notes
JTG_TCK	Input		PullUp	none	VDD_EXT	Desc: JTAG Clock Notes: No notes
JTG_TDI	Input		PullUp	none	VDD_EXT	Desc: JTAG Serial Data In Notes: No notes
JTG_TDO	Output	A	none	High-Z when $\overline{\text{JTG\_TRST}}$ is low, not affected by $\overline{\text{SYS\_HWRST}}$	VDD_EXT	Desc: JTAG Serial Data Out Notes: No notes
JTG_TMS	InOut	A	PullUp	none	VDD_EXT	Desc: JTAG Mode Select Notes: No notes
$\overline{\text{JTG\_TRST}}$	Input		PullDown	none	VDD_EXT	Desc: JTAG Reset Notes: No notes
MLB0_CLKN	Input	NA	Internal logic ensures that input signal does not float	none	VDD_EXT	Desc: MLB0 Differential Clock (–) Notes: No notes
MLB0_CLKP	Input	NA	Internal logic ensures that input signal does not float	none	VDD_EXT	Desc: MLB0 Differential Clock (+) Notes: No notes
MLB0_DATN	InOut	I	Internal logic ensures that input signal does not float	none	VDD_EXT	Desc: MLB0 Differential Data (–) Notes: No notes
MLB0_DATP	InOut	I	Internal logic ensures that input signal does not float	none	VDD_EXT	Desc: MLB0 Differential Data (+) Notes: No notes
MLB0_SIGN	InOut	I	Internal logic ensures that input signal does not float	none	VDD_EXT	Desc: MLB0 Differential Signal (–) Notes: No notes
MLB0_SIGP	InOut	I	Internal logic ensures that input signal does not float	none	VDD_EXT	Desc: MLB0 Differential Signal (+) Notes: No notes
PA_00	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTA Position 0 Notes: See note[2]
PA_01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTA Position 1 Notes: See note[2]
PA_02	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTA Position 2 Notes: See note[2]
PA_03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTA Position 3 Notes: See note[2]
PA_04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTA Position 4 Notes: See note[2]

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
USB0_VBC	InOut	E	none	none	VDD_USB	Desc: USB0 VBUS Control Notes: Add external pull-down if not used[6]
USB0_VBUS	InOut	G	none	none	VDD_USB	Desc: USB0 Bus Voltage Notes: Connect to GND when USB is not used[6]
USB0_CLKIN	a		none	none	VDD_USB	Desc: USB0/USB1 Clock/Crystal Input Notes: Connect to GND when USB is not used[6]
USB0_XTAL	a		none	none	VDD_USB	Desc: USB0/USB1 Crystal Notes: No notes
VDD_DMC	s		none	none		Desc: DMC VDD Notes: No notes
VDD_EXT	s		none	none		Desc: External Voltage Domain Notes: No notes
VDD_HADC	s		none	none		Desc: HADC/TMU VDD Notes: Can be left floating if HADC and TMU are not used
VDD_INT	s		none	none		Desc: Internal Voltage Domain Notes: No notes
VDD_USB	s		none	none		Desc: USB VDD Notes: Connect to VDD_EXT when USB is not used

[1] Disabled by default.

[2] Input by default. When unused, terminate externally in hardware or enable the internal pull-up resistor (when applicable) in software. When present, the internal pull-up design holds the internal path from the pins at the expected logic levels. To pull up the external pads to the expected logic levels, use external resistors..

[3] Enabled by default.

[4] All HADC0_VINx pins can be connected directly to GND if HADC and TMU are not used.

[5] Actively driven by processor otherwise.

[6] Guidance also applies to models that do not feature the associated hardware block. See Table 2 or Table 3 for further information.

Table 28. PLL Operating Conditions

Parameter		Min	Max	Unit
f_{PLLCLK}	PLL Clock Frequency	200	1000	MHz

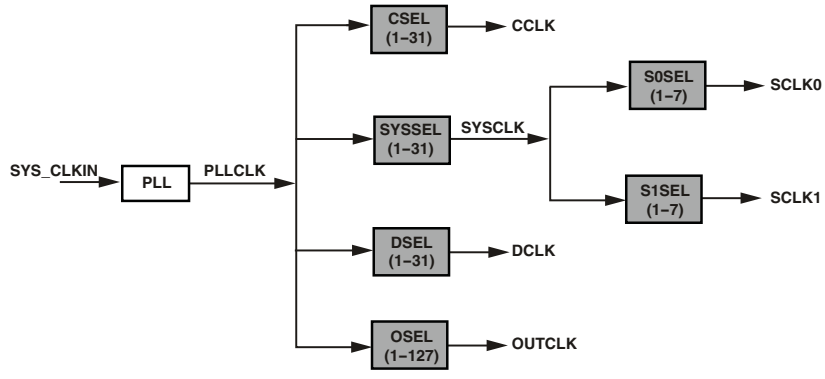

Figure 7. Clock Relationships and Divider Values

Parameter		Conditions	Min	Typ	Max	Unit
I_{DD_IDLE}	V_{DD_INT} Current in Idle	f_{CCLK} = 500 MHz ASF_{SHARC1} = 0.32 ASF_{SHARC2} = 0.32 ASF_{A5} = 0.25 f_{SYSCLK} = 250 MHz $f_{SCLK0/1}$ = 125 MHz (Other clocks are disabled) No Peripheral or DMA activity T_J = 25°C V_{DD_INT} = 1.15 V		477		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 450 MHz ASF_{SHARC1} = 1.0 ASF_{SHARC2} = 1.0 ASF_{A5} = 0.67 f_{SYSCLK} = 225 MHz $f_{SCLK0/1}$ = 112.5 MHz (Other clocks are disabled) DMA data rate = 600 MB/s T_J = 25°C V_{DD_INT} = 1.1 V		890		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 500 MHz ASF_{SHARC1} = 1.0 ASF_{SHARC2} = 1.0 ASF_{A5} = 0.67 f_{SYSCLK} = 250 MHz $f_{SCLK0/1}$ = 125 MHz (Other clocks are disabled) DMA data rate = 600 MB/s T_J = 25°C V_{DD_INT} = 1.15 V		1031		mA
I_{DD_INT}[11]	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK0/1} \geq 0$ MHz			See $I_{DD\_INT\_TOT}$ equation in the Total Internal Power Dissipation section.	mA

[1] Applies to all output and bidirectional pins except TWI, DMC, USB, and MLB.
[2] See the Output Drive Currents section for typical drive current capabilities.
[3] Applies to all DMC output and bidirectional signals in DDR2 mode.
[4] Applies to all DMC output and bidirectional signals in DDR3 mode.
[5] Applies to all DMC output and bidirectional signals in LPDDR mode.
[6] Applies to input pins: SYS_BMODE0-2, SYS_CLKIN0, SYS_CLKIN1, $\overline{\text{SYS\_HWRST}}$, JTG_TDI, JTG_TMS, and USB0_CLKIN.
[7] Applies to input pins with internal pull-ups: JTG_TDI, JTG_TMS, and JTG_TCK.
[8] Applies to signals: JTAG_TRST, USB0_VBUS.
[9] Applies to signals: PA0-15, PB0-15, PC0-15, PD0-15, PE0-15, PF0-11, DAI0_PINx, DMC0_DQx, DMC0_LDQS, DMC0_UDQS, $\overline{\text{DMC0\_LDQS}}$, $\overline{\text{DMC0\_UDQS}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, JTG_TDO, USB0_ID, USB0_DM, USB0_DP, and USB0_VBC.
[10] Applies to all signal pins.
[11] See "Estimating Power for ADSP-SC57x/2157x SHARC+ Processors" (EE-397) for further information.

Table 32. Dynamic Current for Each SHARC+®Core (mA, with ASF = 1.00)[1]

f_{CCLK} (MHz)	Voltage (V_{DD_INT})			
	1.05	1.10	1.15	1.20
500	N/A	347	362	378
450	298	312	326	340
400	265	277	290	302
350	232	243	254	265
300	198	208	217	227
250	165	173	181	189
200	132	139	145	151
150	99	104	109	113
100	66	69	72	76

[1] N/A means not applicable.

Table 33. Dynamic Current for the ARM® Cortex®-A5 Core (mA, with ASF = 1.00)[1]

f_{CCLK} (MHz)	Voltage (V_{DD_INT})			
	1.05	1.10	1.15	1.20
500	N/A	88	92	96
450	76	79	83	86
400	67	70	74	77
350	59	62	64	67
300	50	53	55	58
250	42	44	46	48
200	34	35	37	39
150	25	26	28	29
100	17	18	18	19

[1] N/A means not applicable.

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency, and a unique scaling factor.

$I_{DD\_INT\_SYSCLK\_DYN}$ (mA) = 0.52 × f_{SYSCLK} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_SCLK0\_DYN}$ (mA) = 0.28 × f_{SCLK0} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_SCLK1\_DYN}$ (mA) = 0.013 × f_{SCLK1} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_DCLK\_DYN}$ (mA) = 0.08 × f_{DCLK} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_OCLK\_DYN}$ (mA) = 0.015 × f_{OCLK} (MHz) × V_{DD_INT} (V)

Current from High Speed Peripheral Operation

The following modules contribute significantly to power dissipation, and a single term is added when they are used.

$I_{DD\_INT\_USB\_DYN}$ = 9.6 mA (if USB is enabled in HS mode)

$I_{DD\_INT\_MLB\_DYN}$ = 10 mA (if MLB 6-pin interface is enabled)

$I_{DD\_INT\_EMAC\_DYN}$ = 10 mA (if EMAC is enabled)

Data Transmission Current

The data transmission current represents the power dissipated when moving data throughout the system via DMA. This current is proportional to the data rate. Refer to the power calculator available with "Estimating Power for ADSP-SC57x/2157x SHARC+ Processors" (EE-397) to estimate $I_{DD\_INT\_DMA\_DR\_DYN}$ based on the bandwidth of the data transfer.

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Power-Up Reset Timing

Table 41 and Figure 8 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU).

In Figure 8, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, and V_{DD_HADC}.

Table 41. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{SYS\_HWRST}$ Deasserted after $V_{DD\_SUPPLIES}$ (V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}) and SYS_CLKINx are Stable and within Specification	$11 \times t_{CKIN}$		ns

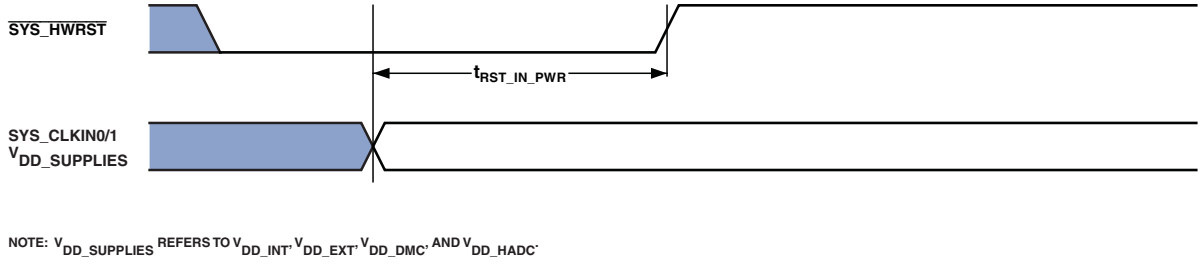

Figure 8. Power-Up Reset Timing

Mobile DDR SDRAM Write Cycle Timing

Table 48 and Figure 15 show mobile DDR SDRAM write cycle timing, related to the DMC.

Table 48. Mobile DDR SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1]		Unit
		Min	Max	
Switching Characteristics				
t_{DQSS}[2]	DMC0_DQS Latching Rising Transitions to Associated Clock Edges	0.75	1.25	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay (Slew > 1 V/ns)	0.48		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay (Slew > 1 V/ns)	0.48		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.4		t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.4		t_{CK}
t_{WPRE}	Write Preamble	0.25		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	2.3		ns
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	1.8		ns

[1] To ensure proper operation of LPDDR, all the LPDDR requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

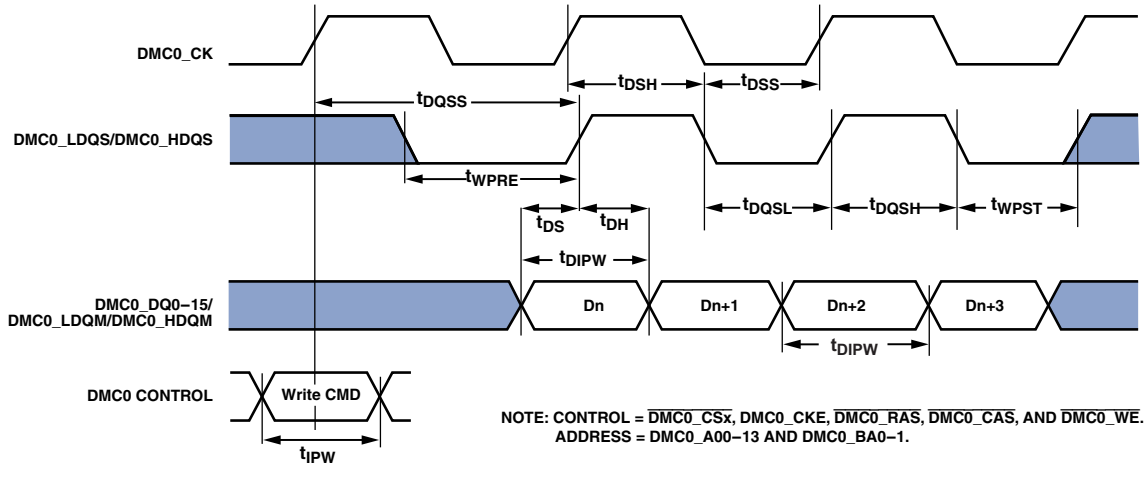

Figure 15. Mobile DDR SDRAM Controller Output AC Timing

Table 53. Enhanced Parallel Peripheral Interface (EPPI)—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	EPPI_CLK Width[1]	0.5 × $t_{PCLKEXT}$ – 0.5		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKEXT}$ – 1		ns
t_{SFSPE}	External FS Setup Before EPPI_CLK	2		ns
t_{HFSPE}	External FS Hold After EPPI_CLK	3.7		ns
t_{SDRPE}	Receive Data Setup Before EPPI_CLK	2		ns
t_{HDRPE}	Receive Data Hold After EPPI_CLK	3.7		ns
Switching Characteristics				
t_{DFSPE}	Internal FS Delay After EPPI_CLK		15.3	ns
t_{HOFSPE}	Internal FS Hold After EPPI_CLK	2.4		ns
t_{DDTPE}	Transmit Data Delay After EPPI_CLK		15.3	ns
t_{HDTPE}	Transmit Data Hold After EPPI_CLK	2.4		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external EPPI_CLK. For the external EPPI_CLK ideal maximum frequency, see the $f_{PCLKEXT}$ specification in Table 27.

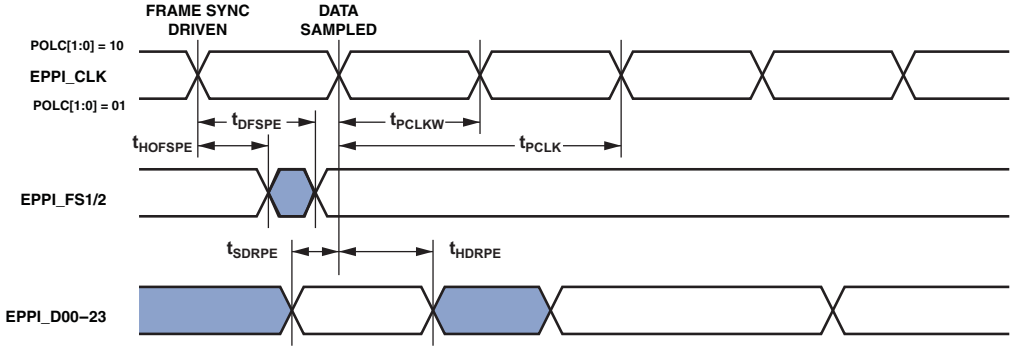

Figure 24. EPPI External Clock GP Receive Mode with Internal Frame Sync Timing

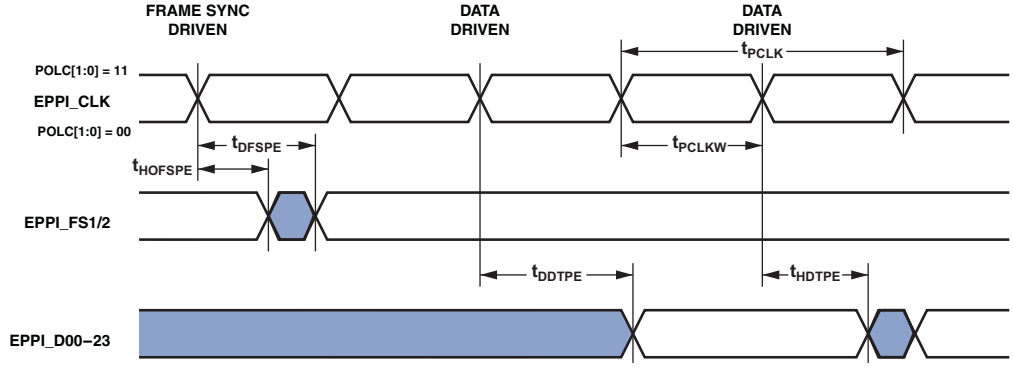

Figure 25. EPPI External Clock GP Transmit Mode with Internal Frame Sync Timing

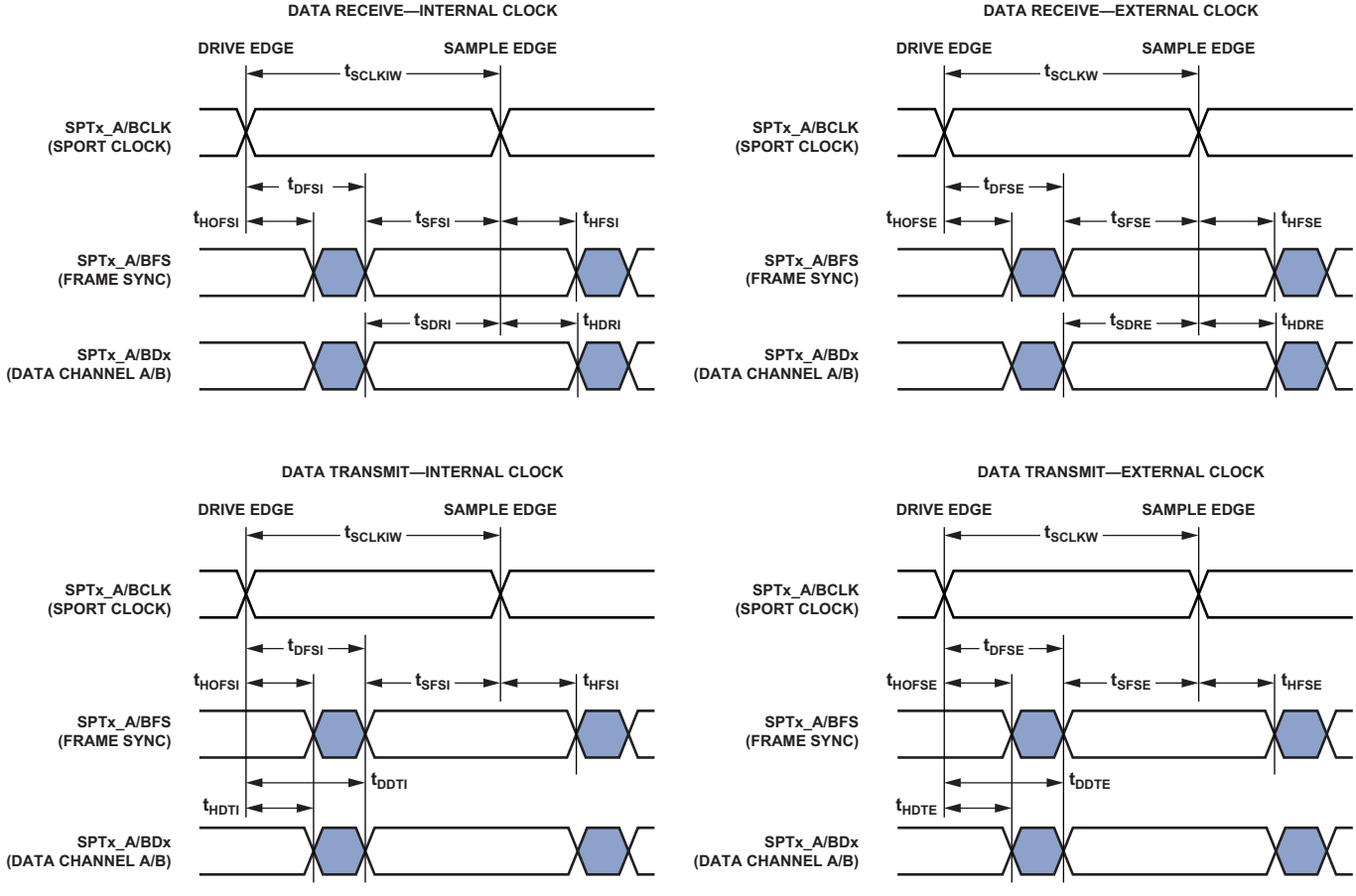

Figure 30. SPORTs

Asynchronous Sample Rate Converter (ASRC)—Serial Output Port

For the serial output port, the frame sync is an input and it must meet setup and hold times with regard to SCLK on the output port. The serial data output has a hold time and delay specification with regard to serial clock. The serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

Table 62. ASRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$t_{SCLK0} - 1$		ns
t_{SRCCLK}	Clock Period	$2 \times t_{SCLK0}$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After Serial Clock Falling Edge		13	ns
t_{SRCTDH}[1]	Transmit Data Hold After Serial Clock Falling Edge	1		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN, SCLK0, or any of the DAI pins.

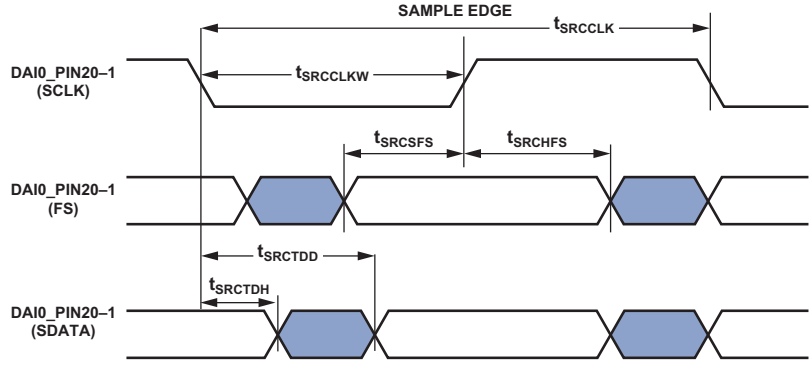

Figure 35. ASRC Serial Output Port Timing

SPI Port—Open Drain Mode (ODM) Timing

In Figure 39 and Figure 40, the outputs can be SPIx_MOSI, SPIx_MISO, SPIx_D2, and/or SPIx_D3, depending on the mode of operation. CPOL and CPHA are configuration bits in the SPI_CTL register.

Table 68. SPI Port—ODM Master Mode Timing[1]

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{HDSPIODMM}$	SPIx_CLK Edge to High Impedance from Data Out Valid	–1.1		ns
$t_{DDSPIODMM}$	SPIx_CLK Edge to Data Out Valid from High Impedance	–1	6	ns

[1] All specifications apply to all three SPIs.

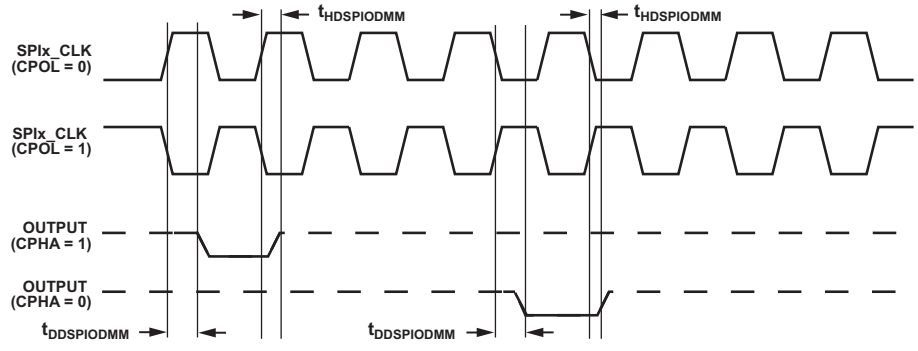

Figure 39. ODM Master Mode

Table 69. SPI Port—ODM Slave Mode[1]

Parameter		Min	Max	Unit
Timing Requirements				
$t_{HDSPIODMS}$	SPIx_CLK Edge to High Impedance from Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPIx_CLK Edge to Data Out Valid from High Impedance		11	ns

[1] All specifications apply to all three SPIs.

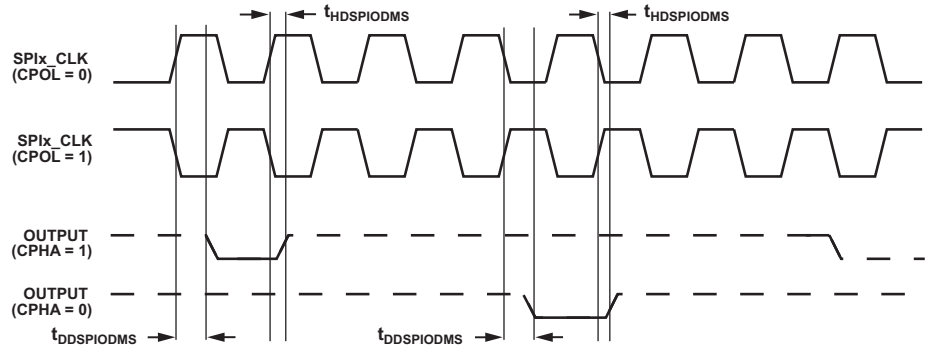

Figure 40. ODM Slave Mode

Precision Clock Generator (PCG) (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes inputs directly from the DAI pins (via pin buffers) and sends outputs directly to the DAI pins. For the other cases, where the PCG inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI0_PINx).

Table 71. PCG (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{SCLK} \times 2$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	13.5	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$13.5 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$[1]	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$13.5 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[2]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

[1] D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference.
[2] Normal mode of operation.

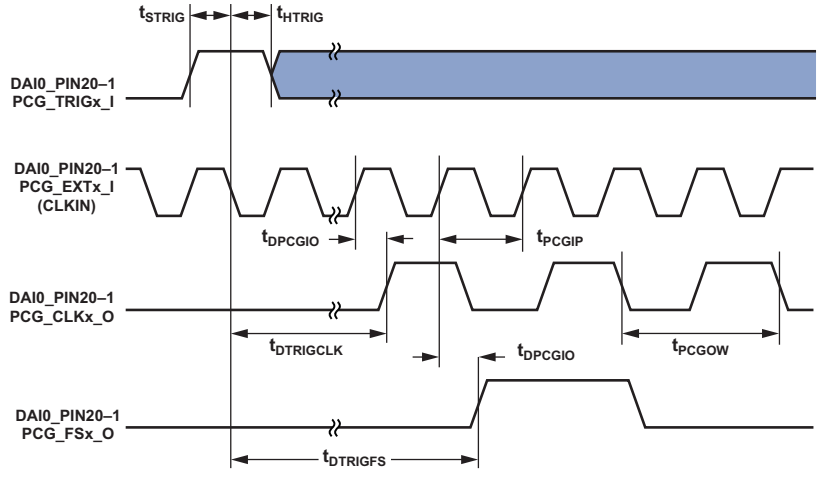

Figure 43. PCG (Direct Pin Routing)

10/100/1000 EMAC Timing

Table 84 and Figure 54 describe the RGMII EMAC timing.

Table 84. 10/100/1000 EMAC Timing—RGMII Receive and Transmit Signals

Parameter		Min	Max	Unit
Timing Requirements				
t_{SETUPR}	Data to Clock Input Setup at Receiver	1		ns
t_{HOLDR}	Data to Clock Input Hold at Receiver	1		ns
$t_{GREFCLKF}$	RGMII Receive Clock Period	8		ns
$t_{GREFCLKW}$	RGMII Receive Clock Pulse Width	4		ns
Switching Characteristics				
t_{SKEWT}	Data to Clock Output Skew at Transmitter	–0.5	+0.5	ns
t_{CYC}	Clock Cycle Duration	7.2	8.8	ns
t_{DUTY_G}	Duty Cycle for RGMII Minimum	$t_{GREFCLKF} \times 45\%$	$t_{GREFCLKF} \times 55\%$	ns

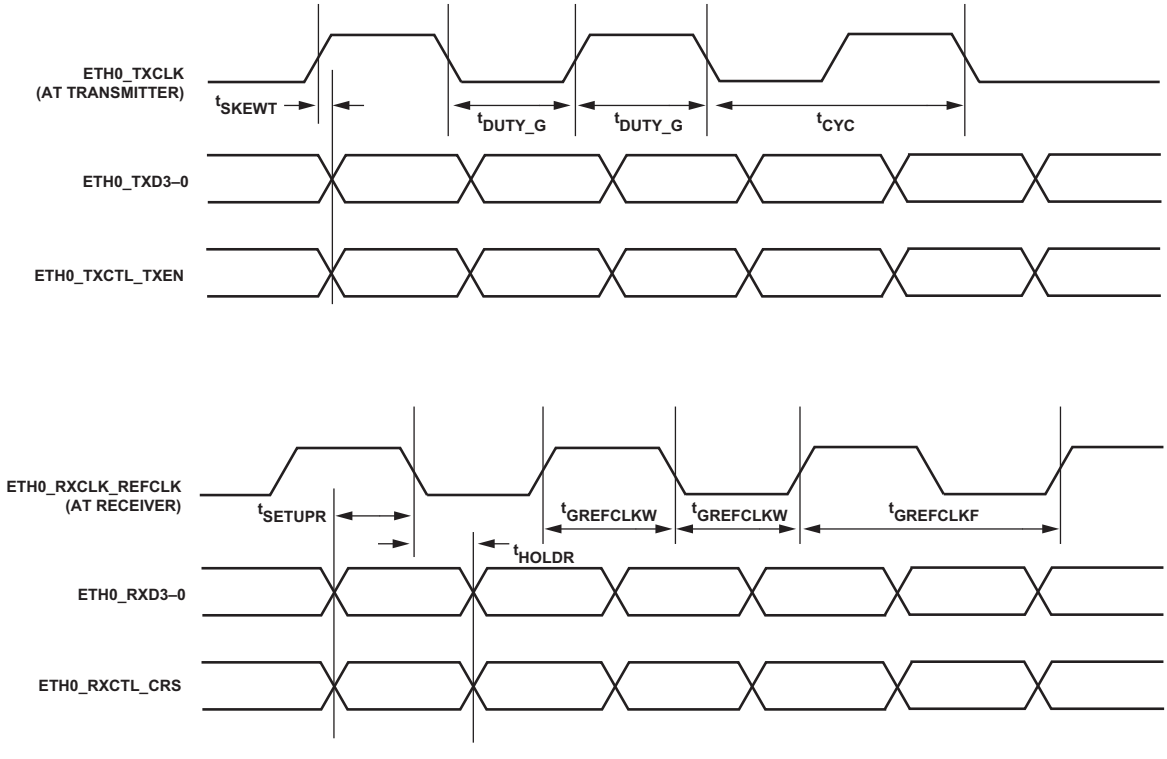

Figure 54. EMAC Timing—RGMII

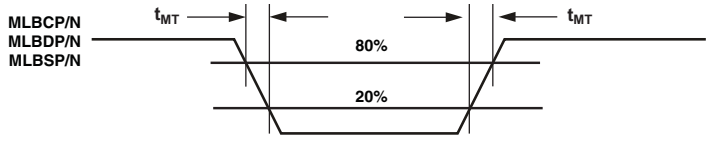

Figure 61. MLB 6-Pin Transition Time

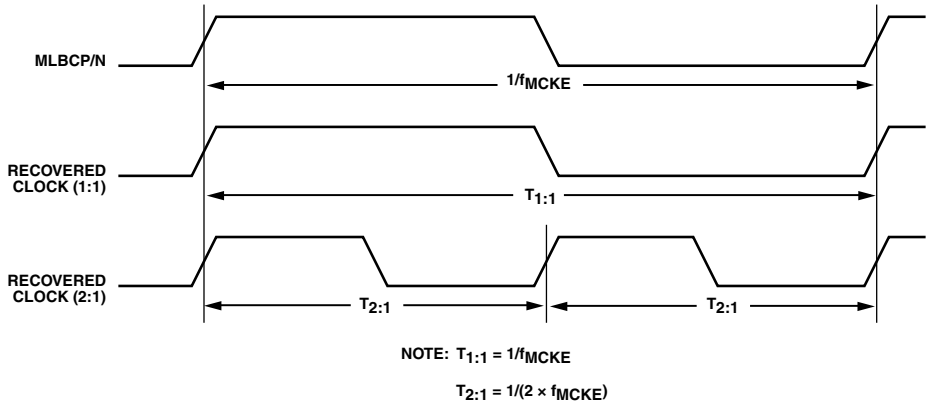

Figure 62. MLB 6-Pin Clock Definitions

Mobile Storage Interface (MSI) Controller Timing

Table 93 and Figure 65 show I/O timing related to the MSI.

Table 93. MSI Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	Input Setup Time	4.8		ns
t_{IH}	Input Hold Time	–0.5		ns
Switching Characteristics				
f_{PP}	Clock Frequency Data Transfer Mode[1]		45	MHz
t_{WL}	Clock Low Time	8		ns
t_{WH}	Clock High Time	8		ns
t_{TLH}	Clock Rise Time		3	ns
t_{THL}	Clock Fall Time		3	ns
t_{ODLY}	Output Delay Time During Data Transfer Mode		2.1	ns
t_{OH}	Output Hold Time	–1.8		ns

[1] $t_{PP} = 1/f_{PP}$.

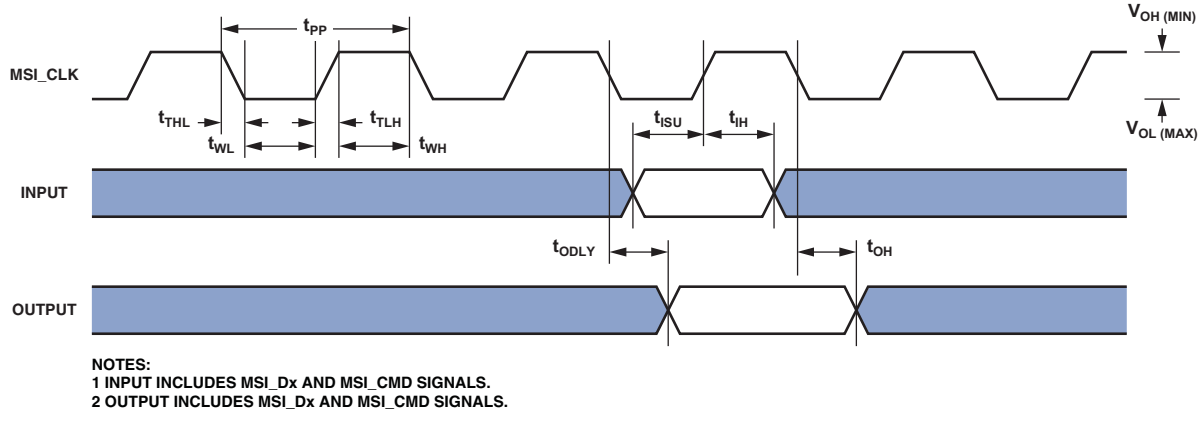

Figure 65. MSI Controller Timing

Program Trace Macrocell (PTM) Timing

Table 94 and Figure 66 provide I/O timing related to the PTM.

Table 94. Trace Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTRD}	TRACE Data Delay From Trace Clock Maximum		$0.5 \times t_{SCLK0} + 4$	ns
t_{HTRD}	TRACE Data Hold From Trace Clock Minimum	$0.5 \times t_{SCLK0} - 2.2$		ns
t_{PTRCK}	TRACE Clock Period Minimum	$2 \times t_{SCLK0} - 1$		ns

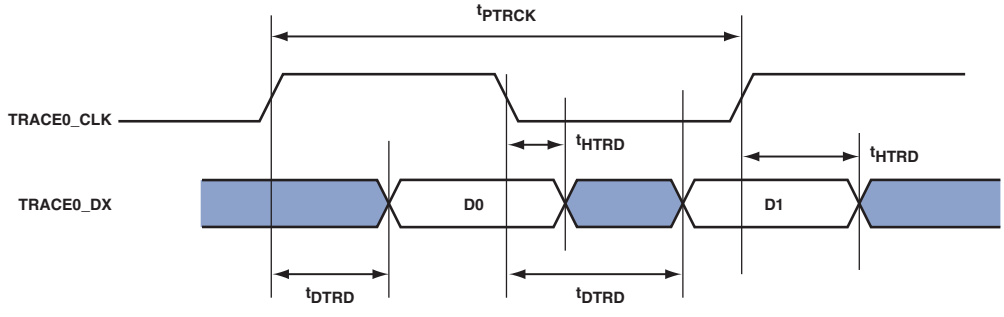

Figure 66. Trace Timing

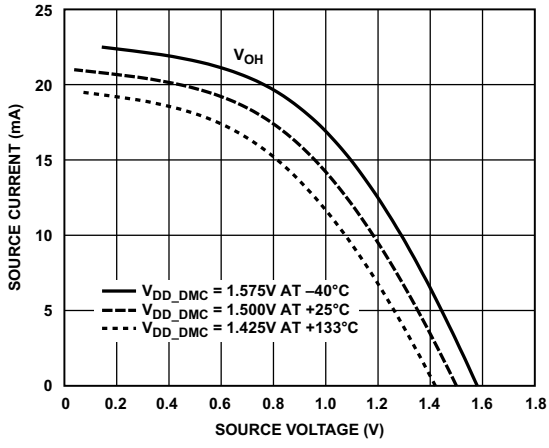

Figure 73. Driver Type B and Driver Type C (DDR3 Drive Strength 40 Ω)

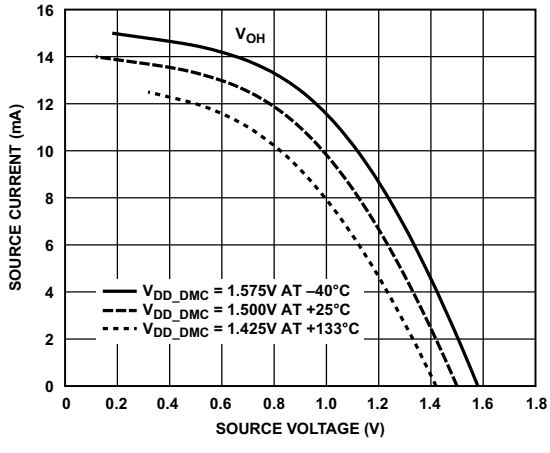

Figure 74. Driver Type B and Driver Type C (DDR3 Drive Strength 60 Ω)

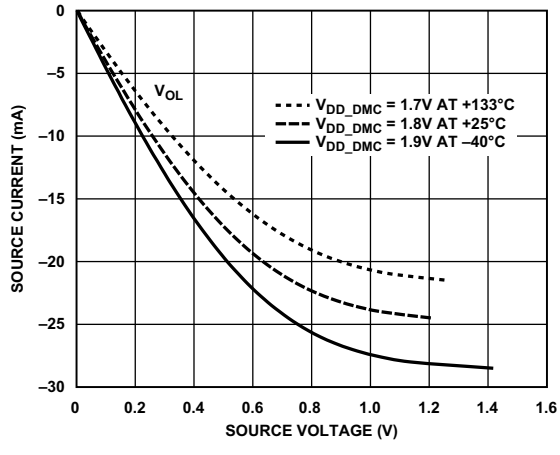

Figure 75. Driver Type B and Driver Type C (DDR2 Drive Strength 40 Ω)

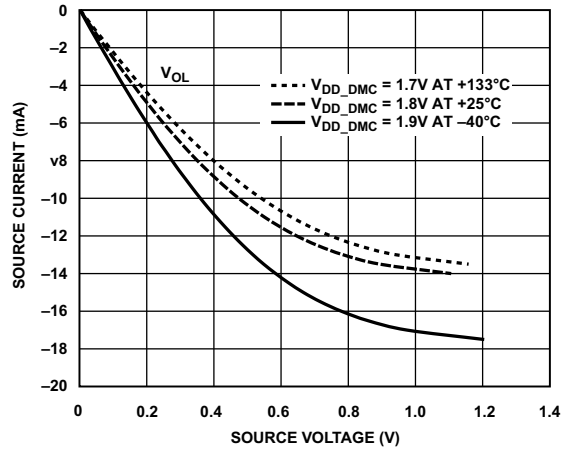

Figure 76. Driver Type B and Driver Type C (DDR2 Drive Strength 60 Ω)

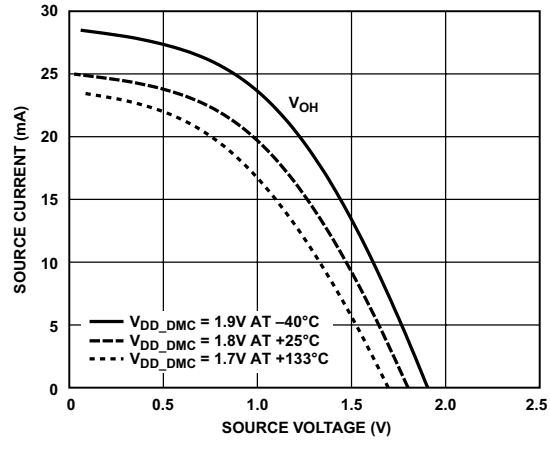

Figure 77. Driver Type B and Driver Type C (DDR2 Drive Strength 40 Ω)

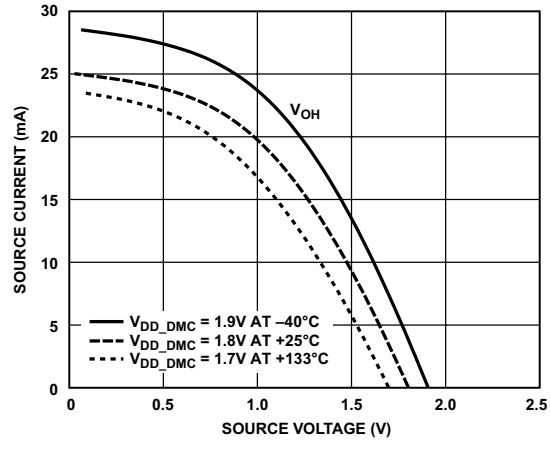

Figure 78. Driver Type B and Driver Type C (DDR2 Drive Strength 60 Ω)

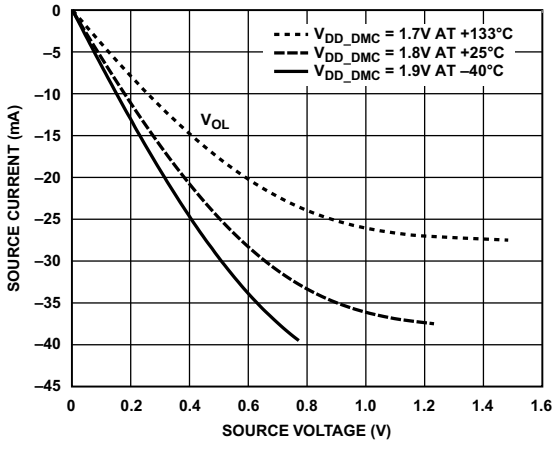

Figure 79. Driver Type B and Device Driver C (LPDDR)

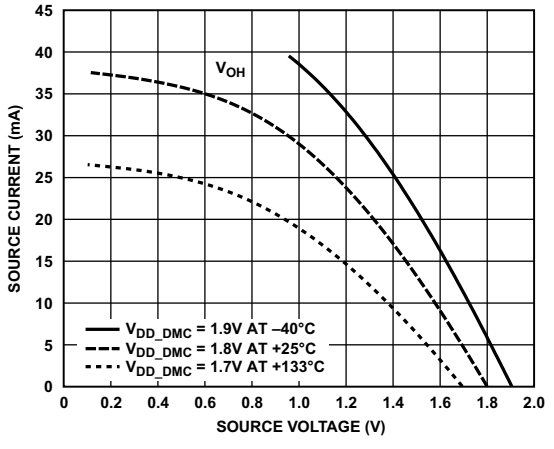

Figure 80. Driver Type B and Device Driver C (LPDDR)

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 81 shows the measurement point for ac measurements (except output enable/disable). The measurement point, V_{MEAS}, is $V_{DD\_EXT}/2$ for V_{DD_EXT} (nominal) = 3.3 V.

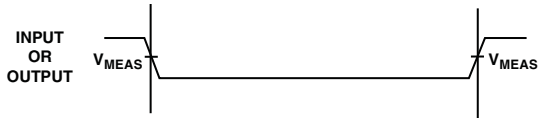

Figure 81. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered enabled when they make a transition from a high impedance state to the point when they start driving.

The output enable time, $t_{ENA,}$ is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving, as shown on the right side of Figure 82. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

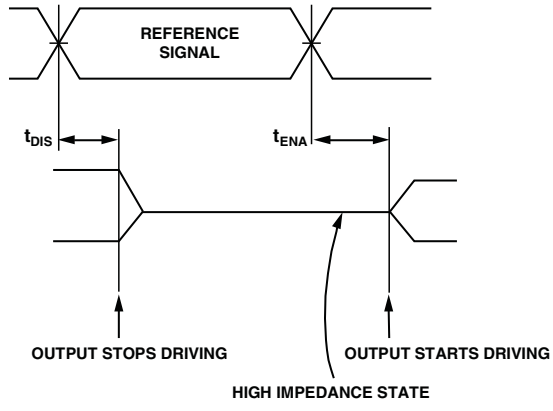

Figure 82. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered disabled when they stop driving, enter a high impedance state, and start to decay from the output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving, as shown on the left side of Figure 82).

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 83). V_{LOAD} is equal to $V_{DD\_EXT}/2$. Figure 84 through Figure 88 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in Figure 84 through Figure 88 cannot be linear outside the ranges shown.