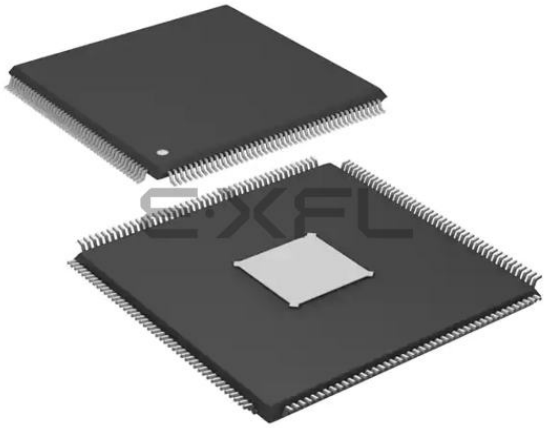

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz, 450MHz
Non-Volatile Memory	External
On-Chip RAM	1.640MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc572kbcz-4

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6/2018—Rev. A to Rev. B

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SYSTEM MEMORY MAP

Table 4. L1 Block 0, Block 1, Block 2, and Block 3 SHARC+® Addressing Memory Map (Private Address Space)

Memory	Long Word (64 Bits)	Extended Precision/ ISA Code (48 Bits)	Normal Word (32 Bits)	Short Word/ VISA Code (16 Bits)	Byte Access (8 Bits)
L1 Block 0 SRAM (1 Mb)	0x00048000–0x0004BFFF	0x00090000–0x00095554	0x00090000–0x00097FFF	0x00120000–0x0012FFFF	0x00240000–0x0025FFFF
L1 Block 1 SRAM (1 Mb)	0x00058000–0x0005BFFF	0x000B0000–0x000B5554	0x000B0000–0x000B7FFF	0x00160000–0x0016FFFF	0x002C0000–0x002DFFFF
L1 Block 2 SRAM (0.5 Mb)	0x00060000–0x00061FFF	0x000C0000–0x000C2AA9	0x000C0000–0x000C3FFF	0x00180000–0x00187FFF	0x00300000–0x0030FFFF
L1 Block 3 SRAM (0.5 Mb)	0x00070000–0x00071FFF	0x000E0000–0x000E2AA9	0x000E0000–0x000E3FFF	0x001C0000–0x001C7FFF	0x00380000–0x0038FFFF

Table 5. L2 Memory Addressing Map

Memory[1]	Byte Address Space ARM Cortex-A5—Data Access and Instruction Fetch SHARC+—Data Access	Normal Word Address Space SHARC+ Data Access	VISA Address Space SHARC+ Instruction Fetch	ISA Address Space SHARC+ Instruction Fetch
L2 Boot ROM0[2]	ARM: 0x00000000–0x00007FFF SHARC/DMA: 0x20100000–0x20107FFF	0x08040000–0x08041FFF	0x00B20000–0x00B23FFF	0x00580000–0x00581555
L2 RAM (8 Mb)	0x20000000–0x200FFFFF	0x08000000–0x0803FFFF	0x00B80000–0x00BFFFFF	0x005C0000–0x005EAAAA
L2 Boot ROM1	0x20108000–0x2010FFFF	0x08042000–0x08043FFF	0x00B00000–0x00B03FFF	0x00500000–0x00501555
L2 Boot ROM2[3]	0x20110000–0x20117FFF	0x08044000–0x08045FFF	0x00B40000–0x00B43FFF	0x00540000–0x00541555

[1] All L2 RAM blocks are subdivided into eight banks.
[2] For ADSP-SC57x products, the L2 Boot ROM0 byte address space is 0x00000000–0x00007FFF.
[3] L2 Boot ROM address for ADSP-2157x products.

Table 6. SHARC+® L1 Memory in Multiprocessor Space

		Memory Block	Byte Address Space ARM Cortex-A5 and SHARC+	Normal Word Address Space SHARC+
L1 memory of SHARC1 in multiprocessor space	Address via Slave1 Port	Block 0	0x28240000–0x2825FFFF	0x0A090000–0x0A097FFF
		Block 1	0x282C0000–0x282DFFFF	0x0A0B0000–0x0A0B7FFF
		Block 2	0x28300000–0x2830FFFF	0x0A0C0000–0x0A0C3FFF
		Block 3	0x28380000–0x2838FFFF	0x0A0E0000–0x0A0E3FFF
L1 memory of SHARC2 in multiprocessor space	Address via Slave1 Port	Block 0	0x28A40000–0x28A5FFFF	0x0A290000–0x0A297FFF
		Block 1	0x28AC0000–0x28ADFFFF	0x0A2B0000–0x0A2B7FFF
		Block 2	0x28B00000–0x28B0FFFF	0x0A2C0000–0x0A2C3FFF
		Block 3	0x28B80000–0x28B8FFFF	0x0A2E0000–0x0A2E3FFF

Table 7. Memory Map of Mapped I/Os[1]

	Byte Address Space ARM Cortex-A5—Data Access and Instruction Fetch SHARC+—Data Access	Normal Word Address Space SHARC+ Data Access	VISA Address Space SHARC+ Instruction Fetch	ISA Address Space SHARC+ Instruction Fetch
SPI2 Memory (512 MB)	0x60000000–0x600FFFFF	0x04000000–0x07FFFFFF	0x00F80000–0x00FFFFFF	0x00780000–0x007FFFFF
	0x60100000–0x602FFFFF		Not applicable	
	0x60300000–0x6FFFFFFF		Not applicable	Not applicable
	0x70000000–0x7FFFFFFF	Not applicable	Not applicable	Not applicable

[1] The ARM Cortex-A5 can access the entire byte address space. The SHARC+ VISA/ISA address space for instruction fetch and the normal word address space for data access do not cover the entire byte address space.

acting as either a master device or a slave device. In a multimaster environment, the SPI peripheral uses open-drain outputs to avoid data bus contention. The flow control features enable slow slave devices to interface with fast master devices by providing an SPI ready pin (SPI_RDY) which flexibly controls the transfers.

The baud rate and clock phase and polarities of the SPI port are programmable. The port has integrated DMA channels for both transmit and receive data streams.

Link Port (LP)

Two 8-bit wide link ports (LPs) for the BGA package (one link port for the LQFP package) can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional and have eight data lines, an acknowledge line, and a clock line.

ADC Control Module (ACM) Interface

The ADC control module (ACM) provides an interface that synchronizes the controls between the processors and an ADC. The analog-to-digital conversions are initiated by the processors, based on external or internal events.

The ACM allows for flexible scheduling of sampling instants and provides precise sampling signals to the ADC.

The ACM synchronizes the ADC conversion process, generating the ADC controls, the ADC conversion start signal, and other signals. The actual data acquisition from the ADC is done by an internal DAI routing of the ACM with the SPORT0 block.

The processors interface directly to many ADCs without any glue logic required.

Ethernet Media Access Controller (EMAC)

The processor features an ethernet media access controller (EMAC): 10/100/1000 AVB Ethernet with precision time protocol (IEEE 1588).

The processors can directly connect to a network through embedded fast EMAC that supports 10Base-T (10 Mb/sec), 100Base-T (100 Mb/sec) and 1000Base-T (1 Gb/sec) operations.

Some standard features of the EMAC are as follows:

- Support and MII/RMII/RGMII protocols for external PHYs.
- RGMII support for the BGA package only
- Full-duplex and half-duplex modes
- Media access management (in half-duplex operation)
- Flow control
- Station management, including the generation of MDC/MDIO frames for read/write access to PHY registers

Some advanced features of the EMAC include the following:

- Automatic checksum computation of IP header and IP payload fields of receive frames
- Independent 32-bit descriptor driven receive and transmit DMA channels
- Frame status delivery to memory through DMA, including frame completion semaphores for efficient buffer queue management in software
- Transmit DMA support for separate descriptors for MAC header and payload fields to eliminate buffer copy operations
- Convenient frame alignment modes
- 47 MAC management statistics counters with selectable clear on read behavior and programmable interrupts on half maximum value
- Advanced power management
- Magic packet detection and wakeup frame filtering
- Support for 802.3Q tagged VLAN frames
- Programmable MDC clock rate and preamble suppression

Audio Video Bridging (AVB) Support

The 10/100/1000 EMAC supports the following audio video bridging (AVB) features:

- Separate channels or queues for AV data transfer in 100 Mbps and 1000 Mbps modes)
- IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for the additional transmit channels
- Configuring up to two additional channels (Channel 1 and Channel 2) on the transmit and receive paths for AV traffic. Channel 0 is available by default and carries the legacy best effort Ethernet traffic on the transmit side.
- Separate DMA, transmit and receive FIFO for AVB latency class
- Programmable control to route received VLAN tagged non AV packets to channels or queues

Precision Time Protocol (PTP) IEEE 1588 Support

The IEEE 1588 standard is a precision clock synchronization protocol for networked measurement and control systems. The processors include hardware support for IEEE 1588 with an integrated precision time protocol synchronization engine (PTP_TSYNC).

This engine provides hardware assisted time stamping to improve the accuracy of clock synchronization between PTP nodes. The main features of the engine include the following:

- Support for both IEEE 1588-2002 and IEEE 1588-2008 protocol standards
- Hardware assisted time stamping capable of up to 12.5 ns resolution
- Lock adjustment
- Automatic detection of IPv4 and IPv6 packets, as well as PTP messages
- Multiple input clock sources (SCLK0, RGMII, RMII, MII clock, and external clock)
- Programmable pulse per second (PPS) output
- Auxiliary snapshot to time stamp external events

The USB clock is provided through a dedicated external crystal or crystal oscillator.

The USB OTG dual-role device controller includes a phase-locked loop (PLL) with programmable multipliers to generate the necessary internal clocking frequency for the USB.

Media Local Bus (MediaLB)

The automotive model has a Microchip MediaLB (MLB) slave interface that allows the processors to function as a media local bus device. It includes support for both 3-pin and 6-pin media local bus protocols. The MLB 3-pin configuration supports speeds up to 1024 × FS. The MLB 6-pin configuration supports speed of 2048 × FS. The MLB also supports up to 64 logical channels with up to 468 bytes of data per MLB frame.

The MLB interface supports MOST25, MOST50, and MOST150 data rates and operates in slave mode only.

2-Wire Controller Interface (TWI)

The processors include three 2-wire interface (TWI) modules that provide a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^2C bus standard. The TWI module offers the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400 kb/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulating the port control, status, and interrupt registers:

- GPIO direction control register specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers have a write one to modify mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processors. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers specify whether individual pins are level or edge sensitive and specify, if edge sensitive, whether the rising edge or both the rising and falling edges of the signal are significant.

Pin Interrupts

Every port pin on the processors can request interrupts in either an edge sensitive or a level sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Five system level interrupt channels (PINT0–PINT4) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin by pin basis. Rather, groups of eight pins (half ports) can be flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half-port assignment and interrupt management. This includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked or not. Most control registers feature multiple MMR address entries to write one to set or write one to clear them individually.

Mobile Storage Interface (MSI)

The mobile storage interface (MSI) controller acts as the host interface for multimedia cards (MMC), secure digital memory cards (SD), and secure digital input/output cards (SDIO). The MSI controller has the following features:

- Support for a single MMC, SD memory, and SDIO card
- Support for 1-bit and 4-bit SD modes
- Support for 1-bit, 4-bit, and 8-bit MMC modes
- Support for eMMC 4.3 embedded NAND flash devices
- An 11-signal external interface with clock, command, optional interrupt, and up to eight data lines
- Integrated DMA controller
- Card interface clock generation in the clock distribution unit (CDU)
- SDIO interrupt and read wait features

SYSTEM ACCELERATION

The following sections describe the system acceleration blocks of the ADSP-SC57x/ADSP-2157x processors.

Finite Impulse Response (FIR) Accelerator

The finite impulse response (FIR) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency. The FIR accelerator can access all memory spaces and can run concurrently with the other accelerators on the processor.

Infinite Impulse Response (IIR) Accelerator

The infinite impulse response (IIR) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency. The IIR accelerator can access all memory spaces and run concurrently with the other accelerators on the processor.

The two capacitors and the series resistor, shown in Figure 6, fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 6 are typical values only. The capacitor values are dependent upon the load capacitance recommendations of the crystal manufacturer and the physical layout of the printed circuit board (PCB). The resistor value depends on the drive level specified by the crystal manufacturer. The user must verify the customized values based on careful investigations on multiple devices over the required temperature range.

A third overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit, shown in Figure 6. A design procedure for third overtone operation is discussed in detail in "Using Third Overtone Crystals with the ADSP-218x DSP" (EE-168). The same recommendations can be used for the USB crystal oscillator.

Clock Distribution Unit (CDU)

The two CGUs each provide outputs which feed a clock distribution unit (CDU). The clock outputs CLKO0–CLKO9 are connected to various targets. For more information, refer to the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference.

Power-Up

SYS_XTALx oscillations (SYS_CLKINx) start when power is applied to the VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ starts on-chip PLL locking (PLL lock counter). The deassertion must apply only if all voltage supplies and SYS_CLKINx oscillations are valid (refer to the Power-Up Reset Timing section).

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_ CLKIN0 input. Refer to the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference to change the default mapping of clocks.

Booting

The processors have several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE[n] input pins. There are two categories of boot modes. In master boot mode, the processors actively load data from serial memories. In slave boot modes, the processors receive data from external host devices.

The boot modes are shown in Table 9. These modes are implemented by the SYS_BMODE[n] bits of the reset configuration register and are sampled during power-on resets and software initiated resets.

In the ADSP-SC57x processors, the ARM Cortex-A5 (Core 0) controls the boot process, including loading all internal and external memory. Likewise, in the ADSP-2157x processors, the SHARC+ (Core 1) controls the boot function. The option for secure boot is available on all models.

Table 9. Boot Modes

SYS_BMODE[n] Setting[1, 2]	Boot Mode
000	No boot
001	SPI2 master
010	SPI2 slave
011	UART0 slave
100	Reserved
101	Reserved
110	Link0 slave

[1] SYS_BMODE2 pin is applicable only for the BGA package.
[2] Link0 slave boot is supported only on the BGA package.

Thermal Monitoring Unit (TMU)

The thermal monitoring unit (TMU) provides on-chip temperature measurement for applications that require substantial power consumption. The TMU is integrated into the processor die and digital infrastructure using an MMR-based system access to measure the die temperature variations in real-time.

TMU features include the following:

- On-chip temperature sensing
- Programmable over temperature and under temperature limits
- Programmable conversion rate
- Programmable clock source selection to run the sensor off an independent local clock
- Averaging feature available

Power Supplies

The processors have separate power supply connections for

- Internal (VDD_INT)
- External (VDD_EXT)
- USB (VDD_USB)
- HADC/TMU (VDD_HADC)
- DMC (VDD_DMC)

All power supplies must meet the specifications provided in Operating Conditions section. All external supply pins must be connected to the same power supply.

Power Management

As shown in Table 10, the processors support four different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate specifications (see the Specifications section for processor operating conditions). If the feature or the peripheral is not used, refer to Table 25.

Table 11. ADSP-SC57x/ADSP-2157x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
MLB_DATN	InOut	**Differential Data (–).**
MLB_DATP	InOut	**Differential Data (+).**
MLB_SIG	InOut	**Single Ended Signal.**
MLB_SIGN	InOut	**Differential Signal (–).**
MLB_SIGP	InOut	**Differential Signal (+).**
$\overline{\text{MSI\_CD}}$	Input	**Card Detect.** Connects to a pull-up resistor and to the card detect output of an SD socket.
MSI_CLK	Output	**Clock.** The clock signal applied to the connected device from the MSI.
MSI_CMD	InOut	**Command.** Sends commands to and receive responses from the connected device.
MSI_D[n]	InOut	**Data n.** Bidirectional data bus.
$\overline{\text{MSI\_INT}}$	Input	**eSDIO Interrupt Input.** Used only for eSDIO. Connects to an eSDIO card interrupt output. An interrupt can be sampled even when the MSI clock to the card is switched off.
PPI_CLK	InOut	**Clock.** Input in external clock mode, output in internal clock mode.
PPI_D[nn]	InOut	**Data n.** Bidirectional data bus.
PPI_FS1	InOut	**Frame Sync 1 (HSYNC).** Behavior depends on EPPI mode. See the EPPI chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for more details.
PPI_FS2	InOut	**Frame Sync 2 (VSYNC).** Behavior depends on EPPI mode. See the EPPI chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for more details.
PPI_FS3	InOut	**Frame Sync 3 (FIELD).** Behavior depends on EPPI mode. See the EPPI chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for more details.
P_[nn]	InOut	**Position n.** General-purpose input/output. See the GP Ports chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for more details.
SPI_CLK	InOut	**Clock.** Input in slave mode, output in master mode.
SPI_D2	InOut	**Data 2.** Transfers serial data in quad mode. Open-drain when ODM mode is enabled.
SPI_D3	InOut	**Data 3.** Transfers serial data in quad mode. Open-drain when ODM mode is enabled.
SPI_MISO	InOut	**Master In, Slave Out.** Transfers serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_MOSI	InOut	**Master Out, Slave In.** Transfers serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_RDY	InOut	**Ready.** Optional flow signal. Output in slave mode, input in master mode.
$\overline{\text{SPI\_SEL[n]}}$	Output	**Slave Select Output n.** Used in master mode to enable the desired slave.
$\overline{\text{SPI\_SS}}$	Input	**Slave Select Input.** Slave mode—acts as the slave select input. Master mode—optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	InOut	**Channel A Clock.** Data and frame sync are driven or sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	InOut	**Channel A Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AD1	InOut	**Channel A Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AFS	InOut	**Channel A Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_ATDV	Output	**Channel A Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SPT_BCLK	InOut	**Channel B Clock.** Data and frame sync are driven or sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	InOut	**Channel B Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.

Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TRACE0_D03	TRACE0 Trace Data 3	F	PF_03
TRACE0_D04	TRACE0 Trace Data 4	D	PD_10
TRACE0_D05	TRACE0 Trace Data 5	D	PD_11
TRACE0_D06	TRACE0 Trace Data 6	D	PD_12
TRACE0_D07	TRACE0 Trace Data 7	D	PD_13
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
TWI1_SCL	TWI1 Serial Clock	Not Muxed	TWI1_SCL
TWI1_SDA	TWI1 Serial Data	Not Muxed	TWI1_SDA
TWI2_SCL	TWI2 Serial Clock	Not Muxed	TWI2_SCL
TWI2_SDA	TWI2 Serial Data	Not Muxed	TWI2_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	D	PD_06
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	D	PD_05
$\overline{\text{UART0\_RX}}$	UART0 Receive	F	PF_09
$\overline{\text{UART0\_TX}}$	UART0 Transmit	F	PF_08
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	E	PE_14
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	E	PE_00
$\overline{\text{UART1\_RX}}$	UART1 Receive	F	PF_11
$\overline{\text{UART1\_TX}}$	UART1 Transmit	F	PF_10
$\overline{\text{UART2\_CTS}}$	UART2 Clear to Send	A	PA_11
$\overline{\text{UART2\_RTS}}$	UART2 Request to Send	A	PA_10
$\overline{\text{UART2\_RX}}$	UART2 Receive	C	PC_13
$\overline{\text{UART2\_TX}}$	UART2 Transmit	C	PC_12
USB0_CLKIN	USB0 Clock/Crystal Input	Not Muxed	USB_CLKIN
USB0_DM	USB0 Data –	Not Muxed	USB0_DM
USB0_DP	USB0 Data +	Not Muxed	USB0_DP
USB0_ID	USB0 OTG ID	Not Muxed	USB0_ID
USB0_VBC	USB0 VBUS Control	Not Muxed	USB0_VBC
USB0_VBUS	USB0 Bus Voltage	Not Muxed	USB0_VBUS
USB0_XTAL	USB0 Crystal	Not Muxed	USB_XTAL
VDD_EXT	External Voltage Domain	Not Muxed	VDD_EXT
VDD_INT	Internal Voltage Domain	Not Muxed	VDD_INT
VDD_DMC	DMC VDD	Not Muxed	VDD_DMC
VDD_HADC	HADC/TMU VDD	Not Muxed	VDD_HADC
VDD_USB	USB VDD	Not Muxed	VDD_USB

[1] Signal is routed to the DAI0_PINnn pin through the DAI0_PBnn pin buffers using the SRU.

Table 15. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	SPI2_SEL3	SPI2_RDY			
PC_01	SPI0_CLK	PPI0_D08			TM0_ACLK2
PC_02	SPI0_MISO	PPI0_D09			
PC_03	SPI0_MOSI	PPI0_D10			TM0_CLK
PC_04	SPI0_SEL1	PPI0_D11			SPI0_SS
PC_05	SPI0_SEL2	PPI0_D06	SPI0_RDY		
PC_06	SPI0_SEL3	ETH0_COL	PPI0_FS3		
PC_07	SPI1_CLK	PPI0_D13			
PC_08	SPI1_MISO	PPI0_D14			
PC_09	SPI1_MOSI				
PC_10	SPI1_SEL1				SPI1_SS
PC_11	SPI1_SEL2	PPI0_CLK	SPI1_RDY		TM0_ACLK4
PC_12	CAN0_RX	MSI0_CD	UART2_TX		TM0_ACI2
PC_13	CAN0_TX	MSI0_INT	UART2_RX		TM0_ACI4
PC_14	CAN1_RX	PPI0_FS1	ACM0_A1	C2_FLG1	TM0_ACI3
PC_15	CAN1_TX	PPI0_FS2	ACM0_A2	TM0_TMR5	

Table 16. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00					
PD_01					
PD_02					
PD_03					
PD_04					
PD_05	SPI0_SEL7		UART0_RTS		
PD_06	SPI1_SEL7	C1_FLG3	UART0_CTS		
PD_07	SPI1_SEL6	CNT0_ZM	TM0_TMR7		
PD_08	ETH0_PTPPPS1	CNT0_DG	SPI2_SEL4		
PD_09	LP1_D7	PPI0_D07	HADC0_EOC_DOUT		TM0_ACLK3
PD_10	LP1_D0	PPI0_D00	TRACE0_D04		
PD_11	LP1_D1	PPI0_D01	TRACE0_D05		
PD_12	LP1_D2	PPI0_D02	TRACE0_D06		
PD_13	LP1_D3	PPI0_D03	TRACE0_D07		
PD_14	LP1_D4	PPI0_D04	ETH0_PTPAUXIN0		
PD_15	LP1_D5	PPI0_D05	ETH0_PTPAUXIN1		

Table 17. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_00	ETH0_PTPPPS2	PPI0_D12	UART1_RTS		
PE_01	ETH0_PTPPPS3	PPI0_D15	C1_FLG1		
PE_02	LP0_CLK				

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
PD_00	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 0 Notes: See note[2]
PD_01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 1 Notes: See note[2]
PD_02	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 2 Notes: See note[2]
PD_03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 3 Notes: See note[2]
PD_04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 4 Notes: See note[2]
PD_05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 5 Notes: See note[2]
PD_06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 6 Notes: See note[2]
PD_07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 7 Notes: See note[2]
PD_08	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 8 Notes: See note[2]
PD_09	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 9 Notes: See note[2]
PD_10	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 10 Notes: See note[2]
PD_11	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 11 Notes: See note[2]
PD_12	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 12 Notes: See note[2]
PD_13	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 13 Notes: See note[2]
PD_14	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 14 Notes: See note[2]
PD_15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTD Position 15 Notes: See note[2]
PE_00	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 0 Notes: See note[2]
PE_01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 1 Notes: See note[2]
PE_02	InOut	H	none	none	VDD_EXT	Desc: PORTE Position 2 Notes: Connect to VDD_EXT or GND if not used
PE_03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 3 Notes: See note[2]
PE_04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 4 Notes: See note[2]
PE_05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 5 Notes: See note[2]
PE_06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 6 Notes: See note[2]
PE_07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: PORTE Position 7 Notes: See note[2]

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
SYS_CLKIN1	a	NA	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: Connect to GND if not used
SYS_CLKOUT	a	H	none	High-Z when $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ are both active[5]	VDD_EXT	Desc: Processor Clock Output Notes: No notes
SYS_FAULT	InOut	A	none	none	VDD_EXT	Desc: Active-High Fault Output Notes: Pull down if not used
$\overline{\text{SYS\_FAULT}}$	InOut	A	none	none	VDD_EXT	Desc: Active-Low Fault Output Notes: Pull up if not used
$\overline{\text{SYS\_HWRST}}$	Input	NA	none	none	VDD_EXT	Desc: Processor Hardware Reset Control Notes: No connection not allowed
$\overline{\text{SYS\_RESOUT}}$	Output	A	none	High-Z when $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ are both active[5]	VDD_EXT	Desc: Reset Output Notes: No notes
SYS_XTAL0	a	NA	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
SYS_XTAL1	a	NA	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
TWI0_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI0_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
TWI1_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI1 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI1_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI1 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
TWI2_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI2 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI2_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI2 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
USB0_DM	InOut	F	none	none	VDD_USB	Desc: USB0 Data– Notes: Add external pull-down if not used[6]
USB0_DP	InOut	F	none	none	VDD_USB	Desc: USB0 Data + Notes: Add external pull-down if not used[6]
USB0_ID	InOut		none	none	VDD_USB	Desc: USB0 OTG ID Notes: Connect to GND when USB is not used[6]

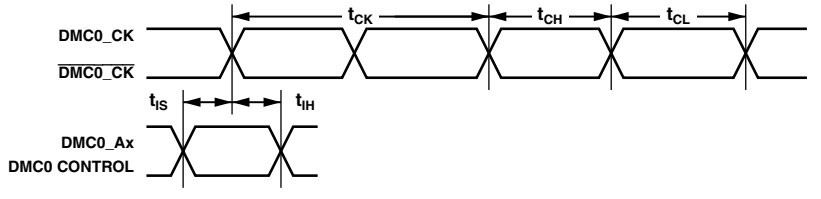
Mobile DDR (LPDDR) SDRAM Clock and Control Cycle Timing

Table 46 and Figure 13 show mobile DDR SDRAM clock and control cycle timing, related to the DMC.

Table 46. Mobile DDR SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1]		Unit
		Min	Max	
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	1		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	1		ns

[1] To ensure proper operation of LPDDR, all the LPDDR requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).



NOTE: CONTROL = DMC0_CS0, DMC0_CKE, DMC0_RAS, DMC0_CAS, AND DMC0_WE.
ADDRESS = DMC0_A0–A15 AND DMC0_BA0–BA2.

Figure 13. Mobile DDR SDRAM Clock and Control Cycle Timing

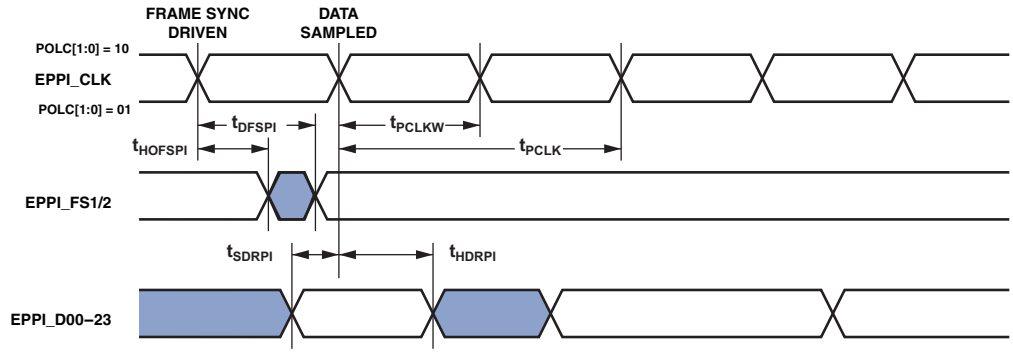


Figure 19. EPPI Internal Clock GP Receive Mode with Internal Frame Sync Timing

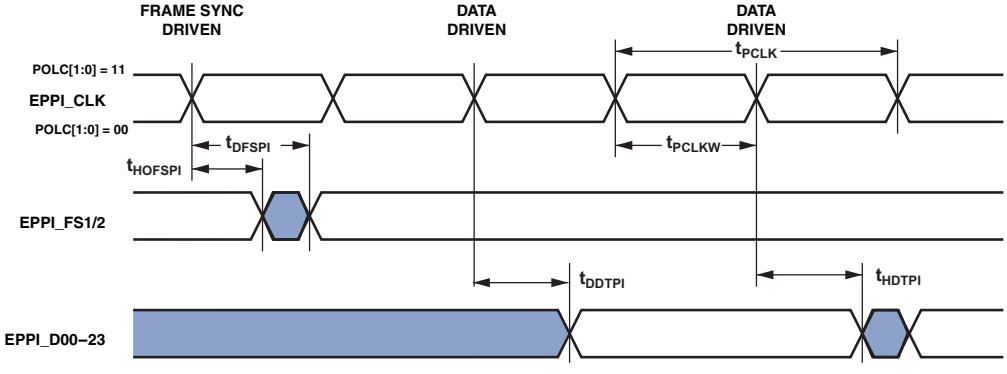


Figure 20. EPPI Internal Clock GP Transmit Mode with Internal Frame Sync Timing

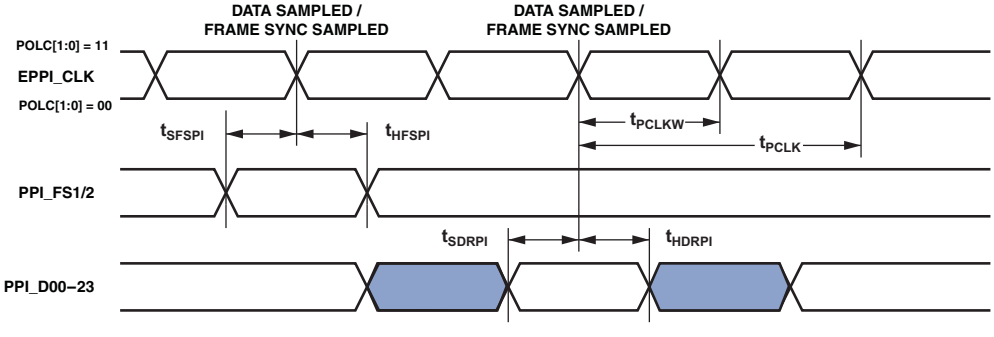


Figure 21. EPPI Internal Clock GP Receive Mode with External Frame Sync Timing

Link Ports (LPs)

In LP receive mode, the LP clock is supplied externally and is called $f_{LCLKREXT}$, therefore the period can be represented by

$$t_{LCLKREXT} = \frac{1}{f_{LCLKREXT}}$$

In LP transmit mode, the programmed LP clock ($f_{LCLKTPROG}$) frequency in megahertz is set by the following equation where VALUE is a field in the LP_DIV register that can be set from 1 to 255:

$$f_{LCLKTPROG} = \frac{f_{SCLK0}}{(VALUE \times 2)}$$

In the case where VALUE = 0, $f_{LCLKTPROG} = f_{SCLK0}$. For all settings of VALUE, the following equation is true:

$$t_{LCLKTPROG} = \frac{1}{f_{LCLKTPROG}}$$

Calculation of the link receiver data setup and hold relative to the link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LPx_Dx and LPx_CLK. Setup skew is the maximum delay that can be introduced in LPx_Dx relative to LPx_CLK (setup skew = $t_{LCLKTWH}$ minimum − t_{DLDCH} − t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LPx_CLK relative to LPx_Dx (hold skew = $t_{LCLKTWL}$ minimum − t_{HLDCH} − t_{HLDCL}).

Table 54. LPs—Receive[1]

Parameter		Min	Max	Unit
Timing Requirements				
$f_{LCLKREXT}$	LPx_CLK Frequency		112.5	MHz
t_{SLDCL}	Data Setup Before LPx_CLK Low	0.9		ns
t_{HLDCL}	Data Hold After LPx_CLK Low	1.4		ns
t_{LCLKEW}	LPx_CLK Period[2]	$t_{LCLKREXT}$ − 0.8		ns
$t_{LCLKRWL}$	LPx_CLK Width Low[2]	0.5 × $t_{LCLKREXT}$		ns
$t_{LCLKRWH}$	LPx_CLK Width High[2]	0.5 × $t_{LCLKREXT}$		ns
Switching Characteristic				
t_{DLALC}	LPx_ACK Low Delay After LPx_CLK Low[3]	1.5 × t_{SCLK0} + 4	2.5 × t_{SCLK0} + 12	ns

[1] Specifications apply to LP0 and LP1.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external LPx_CLK. For the external LPx_CLK ideal maximum frequency, see the $f_{LCLKTEXT}$ specification in Table 27.
[3] LPx_ACK goes low with t_{DLALC} relative to rise of LPx_CLK after first byte, but does not go low if the link buffer of the receiver is not about to fill.

SPI Port—SPIx_RDY Master Timing

SPIx_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx_CTL register, while LEADX, LAGX, and STOP are configuration bits in the SPIx_DLY register.

Table 70. SPI Port—SPIx_RDY Master Timing[1]

Parameter		Conditions	Min	Max	Unit
Timing Requirement					
$t_{SRDYSCKM}$	Setup Time for SPIx_RDY Deassertion Before Last Valid Data SPIx_CLK Edge		$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$		ns
Switching Characteristic					
$t_{DRDYSCKM}$[3]	Assertion of SPIx_RDY to First SPIx_CLK Edge of Next Transfer	BAUD = 0, CPHA = 0	$4.5 \times t_{SCLK1}$	$5.5 \times t_{SCLK1} + 10$	ns
		BAUD = 0, CPHA = 1	$4 \times t_{SCLK1}$	$5 \times t_{SCLK1} + 10$	ns
		BAUD > 0, CPHA = 0	$(1 + 1.5 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2.5 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns
		BAUD > 0, CPHA = 1	$(1 + 1 \times BAUD^{2}) \times t_{SCLK1}$	$(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$	ns

[1] All specifications apply to all three SPIs.
[2] BAUD value is set using the SPIx_CLK.BAUD bits. BAUD value = SPIx_CLK.BAUD bits + 1.
[3] Specification assumes the LEADX, LAGX, and STOP bits in the SPI_DLY register are zero.

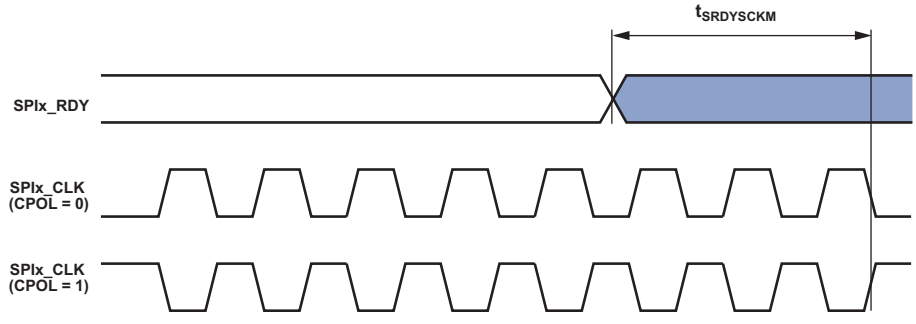


Figure 41. SPIx_RDY Setup Before SPIx_CLK

10/100 EMAC Timing

Table 79 through Table 83 and Figure 49 through Figure 53 describe the MII and RMII EMAC operations.

Table 79. 10/100 EMAC Timing: MII Receive Signal

Parameter[1]		V_{DDEXT} 3.3 V Nominal		Unit
		Min	Max	
Timing Requirements				
$t_{ERXCLKF}$	ETH0_RXCLK_REFCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1%	MHz
$t_{ERXCLKW}$	ETH0_RXCLK_REFCLK Width (t_{ERxCLK} = ETH0_RXCLK_REFCLK Period)	t_{ERxCLK} × 35%	t_{ERxCLK} × 65%	ns
$t_{ERXCLKIS}$	Rx Input Valid to ETH0_RXCLK_REFCLK Rising Edge (Data In Setup)	1.75		ns
$t_{ERXCLKIH}$	ETH0_RXCLK_REFCLK Rising Edge to Rx Input Invalid (Data In Hold)	1.5		ns

[1] MII inputs synchronous to ETH0_RXCLK_REFCLK are ETH0_RXD3-0, ETH0_RXCTL_RXDV, and ETH0_RXERR.

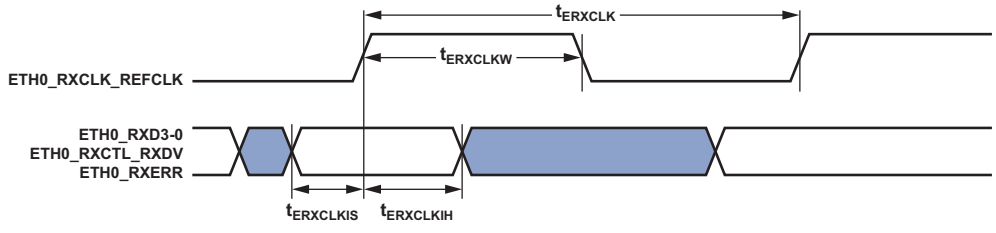


Figure 49. 10/100 EMAC Timing: MII Receive Signal

Table 80. 10/100 EMAC Timing: MII Transmit Signal

Parameter[1]		V_{DDEXT} 3.3 V Nominal		Unit
		Min	Max	
Timing Requirements				
$t_{ETXCLKF}$	ETH0_TXCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1%	MHz
$t_{ETXCLKW}$	ETH0_TXCLK Width (t_{ETxCLK} = ETH0_TXCLK Period)	t_{ETxCLK} × 35%	t_{ETxCLK} × 65%	ns
Switching Characteristics				
$t_{ETXCLKOV}$	ETH0_TXCLK Rising Edge to Tx Output Valid (Data Out Valid)		11.4	ns
$t_{ETXCLKOH}$	ETH0_TXCLK Rising Edge to Tx Output Invalid (Data Out Hold)	2		ns

[1] MII outputs synchronous to ETH0_TXCLK are ETH0_TXD3-0.

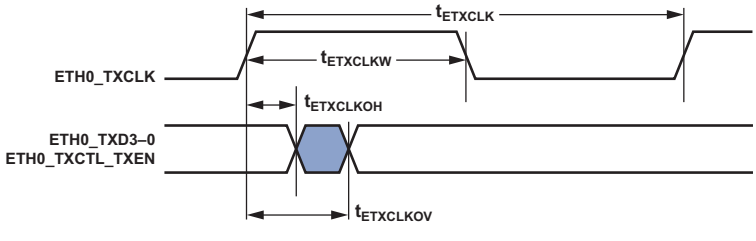


Figure 50. 10/100 EMAC Timing: MII Transmit Signal

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 88. Input signals are routed to the DAI0_PINx pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI0_PINx pins.

Table 88. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

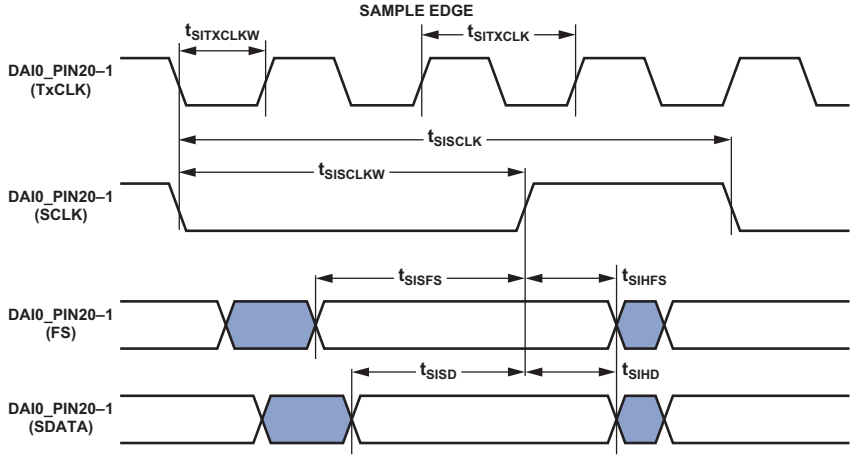


Figure 58. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 89. Oversampling Clock (TxCLK) Switching Characteristics

Parameter		Max	Unit
Switching Characteristics			
f_{TXCLK_384}	Frequency for TxCLK = 384 × Frame Sync	Oversampling ratio × frame sync ≤ $1/t_{SITXCLK}$	MHz
f_{TXCLK_256}	Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
f_{FS}	Frame Rate (FS)	192.0	kHz

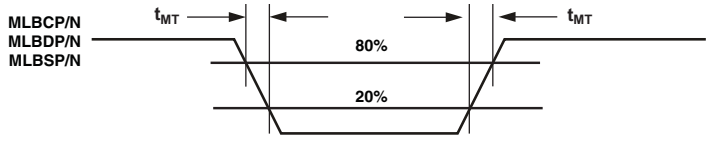


Figure 61. MLB 6-Pin Transition Time

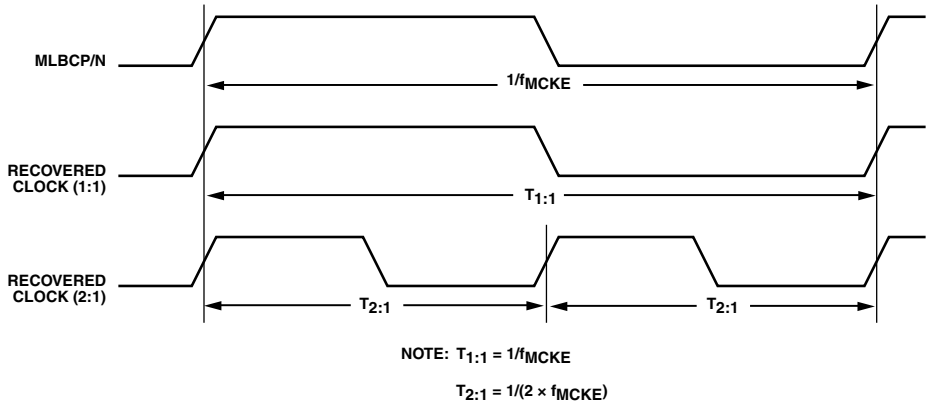


Figure 62. MLB 6-Pin Clock Definitions

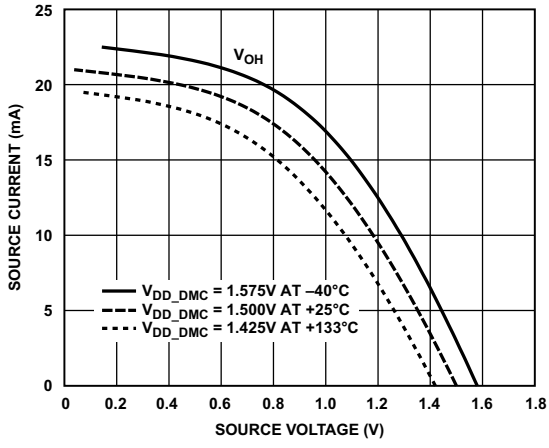


Figure 73. Driver Type B and Driver Type C (DDR3 Drive Strength 40 Ω)

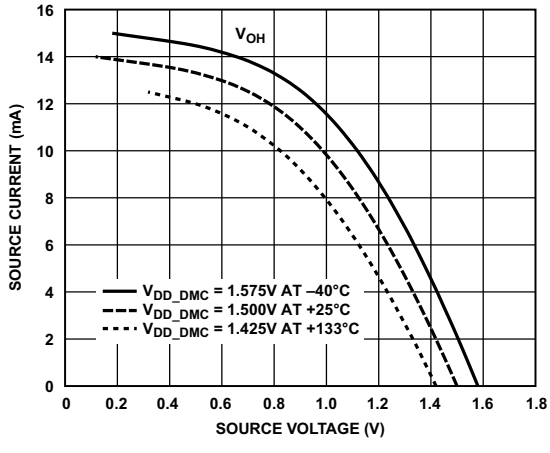


Figure 74. Driver Type B and Driver Type C (DDR3 Drive Strength 60 Ω)

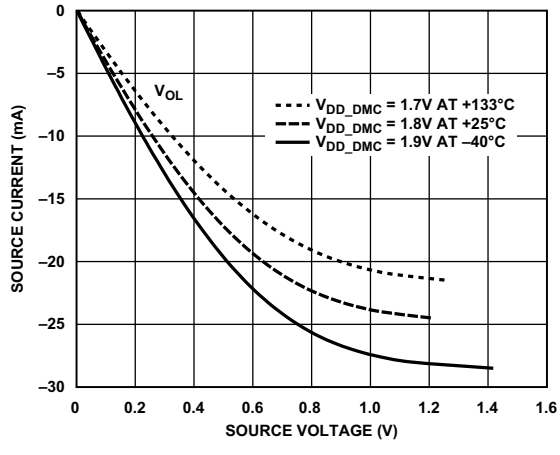


Figure 75. Driver Type B and Driver Type C (DDR2 Drive Strength 40 Ω)

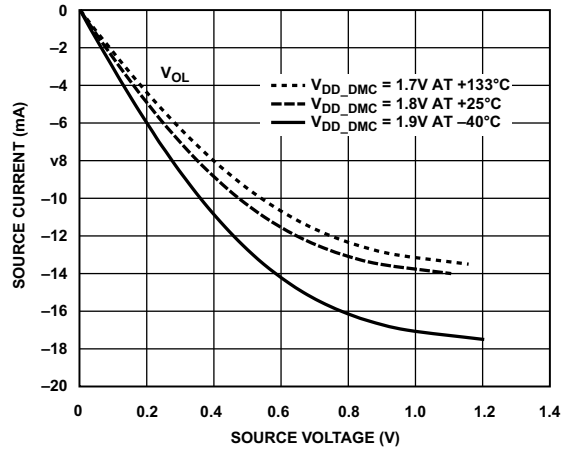


Figure 76. Driver Type B and Driver Type C (DDR2 Drive Strength 60 Ω)

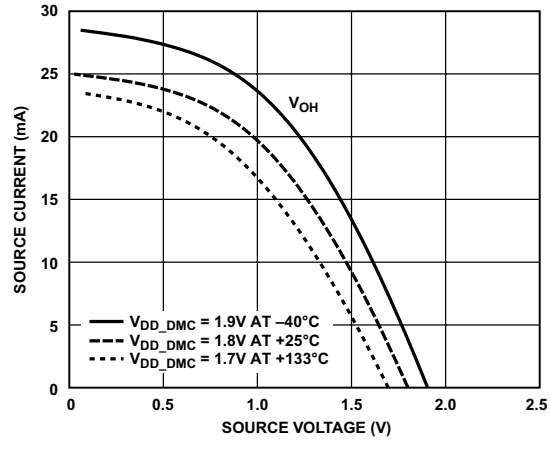


Figure 77. Driver Type B and Driver Type C (DDR2 Drive Strength 40 Ω)

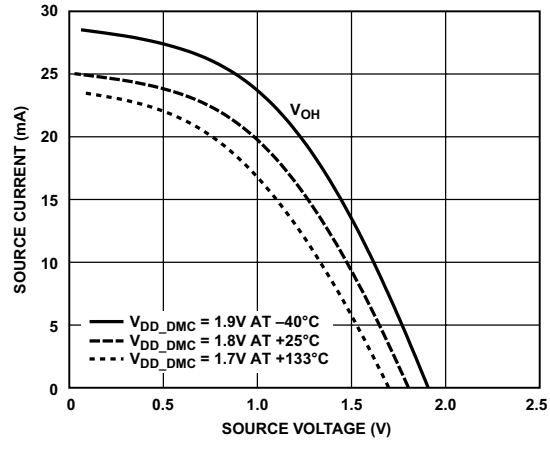


Figure 78. Driver Type B and Driver Type C (DDR2 Drive Strength 60 Ω)

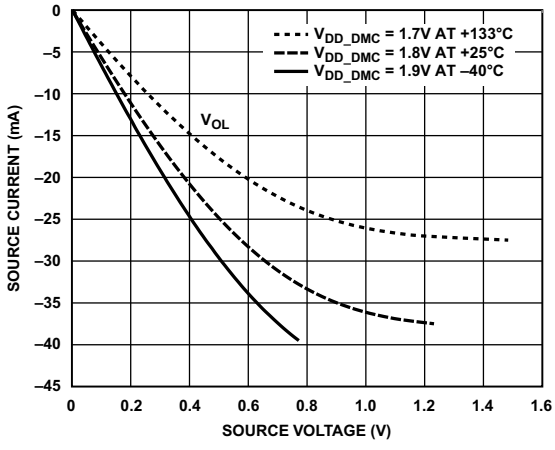


Figure 79. Driver Type B and Device Driver C (LPDDR)

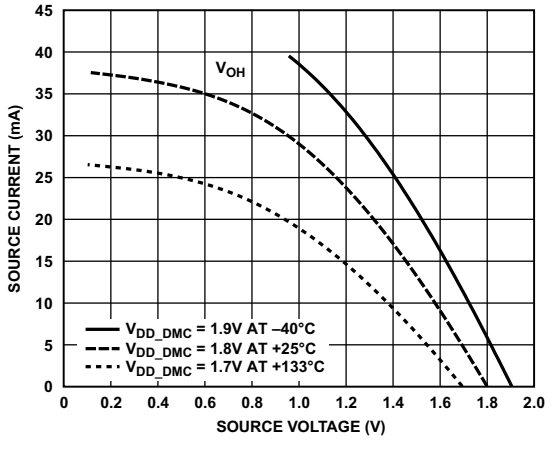


Figure 80. Driver Type B and Device Driver C (LPDDR)

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 81 shows the measurement point for ac measurements (except output enable/disable). The measurement point, V_{MEAS}, is $V_{DD\_EXT}/2$ for V_{DD_EXT} (nominal) = 3.3 V.

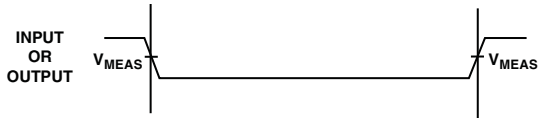


Figure 81. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered enabled when they make a transition from a high impedance state to the point when they start driving.

The output enable time, $t_{ENA,}$ is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving, as shown on the right side of Figure 82. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

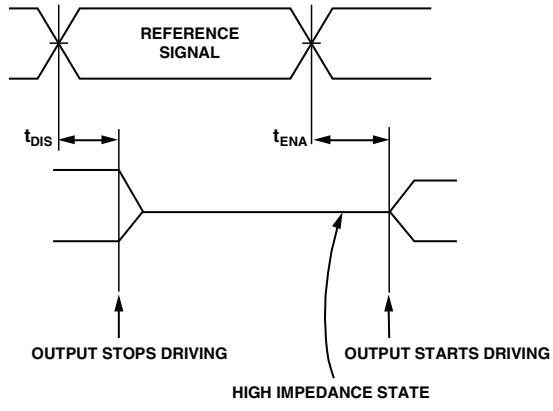


Figure 82. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered disabled when they stop driving, enter a high impedance state, and start to decay from the output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving, as shown on the left side of Figure 82).

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 83). V_{LOAD} is equal to $V_{DD\_EXT}/2$. Figure 84 through Figure 88 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in Figure 84 through Figure 88 cannot be linear outside the ranges shown.

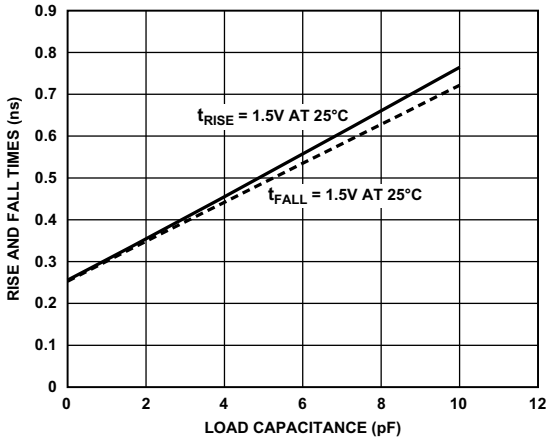


Figure 88. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance (V_{DD_DMC} = 1.5 V) for DDR3

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application PCB, use the following equation:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J = junction temperature (°C).
T_{CASE} = case temperature (°C) measured at the top center of the package.
Ψ_{JT} = from Table 96 and Table 97.
P_D = power dissipation (see the Total Internal Power Dissipation section for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A = ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

In Table 96 and Table 97, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction to case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 6 layer PCB with 101.6 mm × 152.4 mm dimensions.

Table 96. Thermal Characteristics for 400 CSP_BGA

Parameter	Conditions	Typical	Unit
θ_{JA}	0 linear m/s air flow	14.24	°C/W
θ_{JA}	1 linear m/s air flow	12.61	°C/W
θ_{JA}	2 linear m/s air flow	12.09	°C/W
θ_{JC}		5.71	°C/W
Ψ_{JT}	0 linear m/s air flow	0.08	°C/W
Ψ_{JT}	1 linear m/s air flow	0.14	°C/W
Ψ_{JT}	2 linear m/s air flow	0.17	°C/W

Table 97. Thermal Characteristics for 176 LQFP_EP

Parameter	Conditions	Typical	Unit
θ_{JA}	0 linear m/s air flow	11.95	°C/W
θ_{JA}	1 linear m/s air flow	10.43	°C/W
θ_{JA}	2 linear m/s air flow	9.98	°C/W
θ_{JC}		11.10	°C/W
Ψ_{JT}	0 linear m/s air flow	0.15	°C/W
Ψ_{JT}	1 linear m/s air flow	0.24	°C/W
Ψ_{JT}	2 linear m/s air flow	0.29	°C/W