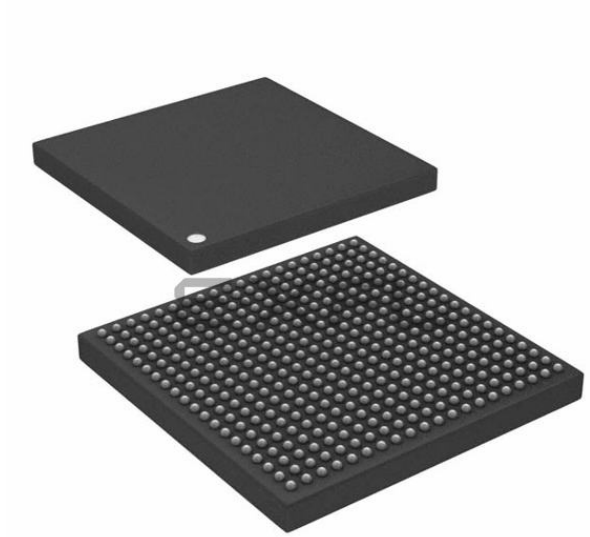

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz, 450MHz
Non-Volatile Memory	External
On-Chip RAM	2MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc573bbcz-4

Generic Interrupt Controller (GIC), PL390 (ADSP-SC57x Only)

The generic interrupt controller (GIC) is a centralized resource for supporting and managing interrupts. The GIC splits into the distributor block (GICPORT0) and the central processing unit (CPU) interface block (GICPORT1).

Generic Interrupt Controller Port0 (GICPORT0)

The GICPORT0 distributor block performs interrupt prioritization and distribution to the GICPORT1 CPU interface blocks that connect to the processors in the system. It centralizes all interrupt sources, determines the priority of each interrupt, and forwards the interrupt with the highest priority to the interface, for priority masking and preemption handling.

Generic Interrupt Controller Port1 (GICPORT1)

The GICPORT1 CPU interface block performs priority masking and preemption handling for a connected processor in the system. GICPORT1 supports 8 software generated interrupts (SGIs) and 212 shared peripheral interrupts (SPIs).

L2 Cache Controller, PL310 (ADSP-SC57x Only)

The Level 2 (L2) cache controller, PL310 (see Figure 2), works efficiently with the ARM Cortex-A5 processors that implement system fabric. The cache controller directly interfaces on the data and instruction interface. The internal pipelining of the cache controller is optimized to enable the processors to operate at the same clock frequency. The cache controller supports the following:

- Two read/write 64-bit slave ports, one connected to the ARM Cortex-A5 instruction and data interfaces, and one connecting the ARM Cortex-A5 and SHARC+ cores for data coherency.
- Two read/write 64-bit master ports for interfacing with the system fabric.

SHARC PROCESSOR

Figure 3 shows the SHARC processor integrates a SHARC+ SIMD core, L1 memory crossbar, I/D cache controller, L1 memory blocks, and the master/slave ports. Figure 4 shows the SHARC+ SIMD core block diagram.

The SHARC processor supports a modified Harvard architecture in combination with a hierarchical memory structure. L1 memories typically operate at the full processor speed with little or no latency.

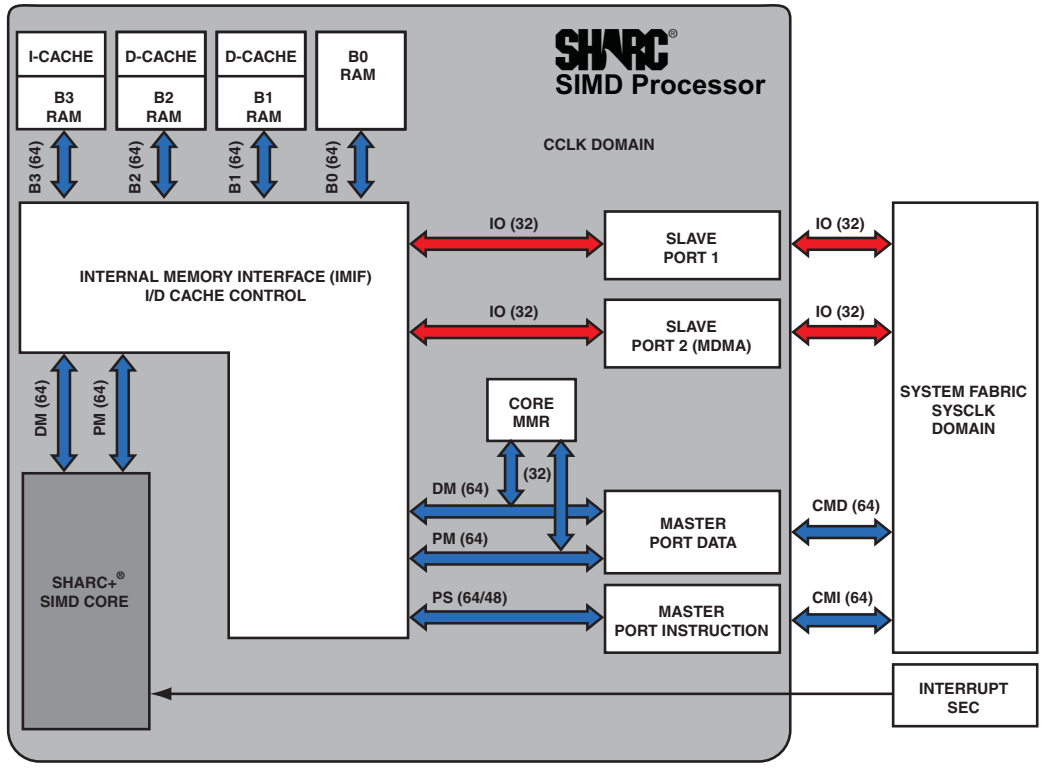

Figure 3. SHARC Processor Block Diagram

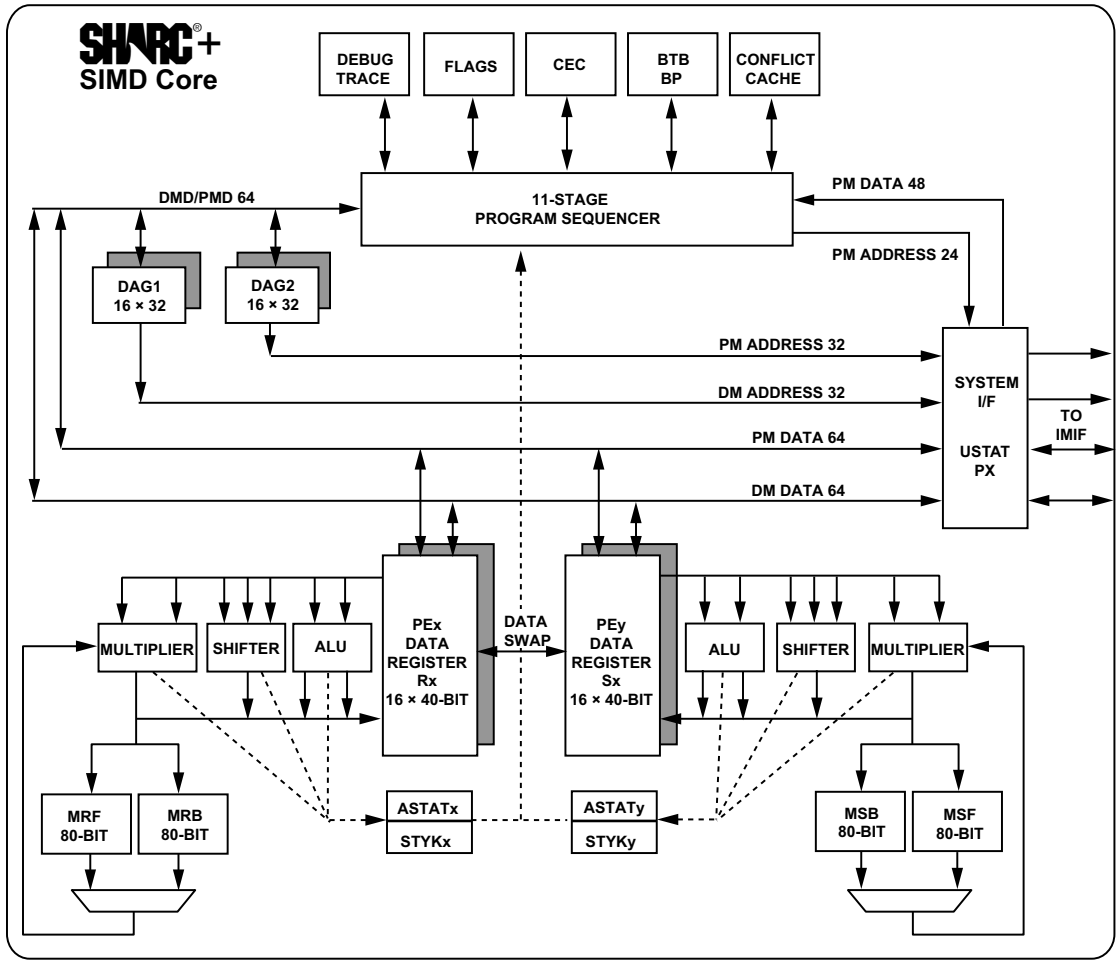

Figure 4. SHARC+ SIMD Core Block Diagram

L1 Memory

Figure 5 shows the ADSP-SC57x/ADSP-2157x memory map. Each SHARC+ core has a tightly coupled L1 SRAM of up to 3 Mb. Each SHARC+ core can access code and data in a single cycle from this memory space. The ARM Cortex-A5 core can also access this memory space with multicycle accesses.

In the SHARC+ core private address space, both cores have L1 memory.

SHARC+ core memory-mapped register (CMMR) address space is 0x00000000 through 0x0003FFFF in normal word (32-bit). Each block can be configured for different combinations of code and data storage. Of the 3 Mb SRAM, up to 1024 Kb/512 Kb can be configured for data memory (DM), program memory (PM), and instruction cache. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the direct memory access (DMA) engine in a single cycle.

The SRAM of the processor can be configured as a maximum of 96k words of 32-bit data, 192k words of 16-bit data, 64k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 3 Mb. All of the memory can be accessed as 8-bit, 16-bit, 32-bit, 48-bit, or 64-bit words. Support of a 16-bit floating-point storage format doubles the amount of data that can be stored on chip.

Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM and PM buses, with each bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The two capacitors and the series resistor, shown in Figure 6, fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in Figure 6 are typical values only. The capacitor values are dependent upon the load capacitance recommendations of the crystal manufacturer and the physical layout of the printed circuit board (PCB). The resistor value depends on the drive level specified by the crystal manufacturer. The user must verify the customized values based on careful investigations on multiple devices over the required temperature range.

A third overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit, shown in Figure 6. A design procedure for third overtone operation is discussed in detail in "Using Third Overtone Crystals with the ADSP-218x DSP" (EE-168). The same recommendations can be used for the USB crystal oscillator.

Clock Distribution Unit (CDU)

The two CGUs each provide outputs which feed a clock distribution unit (CDU). The clock outputs CLKO0–CLKO9 are connected to various targets. For more information, refer to the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference.

Power-Up

SYS_XTALx oscillations (SYS_CLKINx) start when power is applied to the VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ starts on-chip PLL locking (PLL lock counter). The deassertion must apply only if all voltage supplies and SYS_CLKINx oscillations are valid (refer to the Power-Up Reset Timing section).

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided-down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_ CLKIN0 input. Refer to the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference to change the default mapping of clocks.

Booting

The processors have several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE[n] input pins. There are two categories of boot modes. In master boot mode, the processors actively load data from serial memories. In slave boot modes, the processors receive data from external host devices.

The boot modes are shown in Table 9. These modes are implemented by the SYS_BMODE[n] bits of the reset configuration register and are sampled during power-on resets and software initiated resets.

In the ADSP-SC57x processors, the ARM Cortex-A5 (Core 0) controls the boot process, including loading all internal and external memory. Likewise, in the ADSP-2157x processors, the SHARC+ (Core 1) controls the boot function. The option for secure boot is available on all models.

Table 9. Boot Modes

SYS_BMODE[n] Setting[1, 2]	Boot Mode
000	No boot
001	SPI2 master
010	SPI2 slave
011	UART0 slave
100	Reserved
101	Reserved
110	Link0 slave

[1] SYS_BMODE2 pin is applicable only for the BGA package.
[2] Link0 slave boot is supported only on the BGA package.

Thermal Monitoring Unit (TMU)

The thermal monitoring unit (TMU) provides on-chip temperature measurement for applications that require substantial power consumption. The TMU is integrated into the processor die and digital infrastructure using an MMR-based system access to measure the die temperature variations in real-time.

TMU features include the following:

- On-chip temperature sensing
- Programmable over temperature and under temperature limits
- Programmable conversion rate
- Programmable clock source selection to run the sensor off an independent local clock
- Averaging feature available

Power Supplies

The processors have separate power supply connections for

- Internal (VDD_INT)
- External (VDD_EXT)
- USB (VDD_USB)
- HADC/TMU (VDD_HADC)
- DMC (VDD_DMC)

All power supplies must meet the specifications provided in Operating Conditions section. All external supply pins must be connected to the same power supply.

Power Management

As shown in Table 10, the processors support four different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions. There are no sequencing requirements for the various power domains, but all domains must be powered according to the appropriate specifications (see the Specifications section for processor operating conditions). If the feature or the peripheral is not used, refer to Table 25.

Table 11. ADSP-SC57x/ADSP-2157x Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
$\overline{\text{DMC\_UDQS}}$	InOut	**Data Strobe for Upper Byte (Complement).** Complement of DMC_UDQS. Not used in single-ended mode.
DMC_VREF	Input	**Voltage Reference.** Connects to half of the VDD_DMC voltage. Applies to the DMC0_VREF pin.
$\overline{\text{DMC\_WE}}$	Output	**Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory.
ETH_COL	Input	**MII Collision Detect.** Collision detect input signal valid only in MII.
ETH_CRS	Input	**MII Carrier Sense.** Asserted by the PHY when either the transmit or receive medium is not idle. Deasserted when both are idle. This signal is not used in RMII/RGMII modes.
ETH_MDC	Output	**Management Channel Clock.** Clocks the MDC input of the PHY for RMII/RGMII.
ETH_MDIO	InOut	**Management Channel Serial Data.** Bidirectional data bus for PHY control for RMII/RGMII.
ETH_PTPAUXIN[n]	Input	**PTP Auxiliary Trigger Input.** Assert this signal to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO.
ETH_PTPCLKIN[n]	Input	**PTP Clock Input.** Optional external PTP clock input.
ETH_PTPPPS[n]	Output	**PTP Pulse Per Second Output.** When the advanced time stamp feature enables, this signal is asserted based on the PPS mode selected. Otherwise, this signal is asserted every time the seconds counter is incremented.
ETH_RXCLK_REFCLK	InOut	**RXCLK (10/100/1000) or REFCLK (10/100).**
ETH_RXCTL_RXDV	InOut	**RXCTL (10/100/1000) or RXDV (10/100).** In RGMII mode, RX_CTL multiplexes receive data valid and receiver error. In RMII mode, RXDV is carrier sense and receive data valid (CRS_DV), multiplexed on alternating clock cycles. In MII mode, RXDV is receive data valid (RX_DV), asserted by the PHY when the data on ETH_RXD[n] is valid.
ETH_RXD[n]	Input	**Receive Data n.** Receive data bus.
ETH_RXERR	Input	**Receive Error.**
ETH_TXCLK	Input	**Reference Clock.** Externally supplied Ethernet clock
ETH_TXCTL_TXEN	InOut	**TXCTL (10/100/1000) or TXEN (10/100).**
ETH_TXD[n]	Output	**Transmit Data n.** Transmit data bus.
HADC_EOC_DOUT	Output	**End of Conversion/Serial Data Out.** Transitions high for one cycle of the HADC internal clock at the end of every conversion. Alternatively, HADC serial data out can be seen by setting the appropriate bit in HADC_CTL.
HADC_VIN[n]	Input	**Analog Input at Channel n.** Analog voltage inputs for digital conversion.
HADC_VREFN	Input	**Ground Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications.
HADC_VREFP	Input	**External Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications.
JTG_TCK	Input	**JTAG Clock.** JTAG test access port clock.
JTG_TDI	Input	**JTAG Serial Data In.** JTAG test access port data input.
JTG_TDO	Output	**JTAG Serial Data Out.** JTAG test access port data output.
JTG_TMS	Input	**JTAG Mode Select.** JTAG test access port mode select.
$\overline{\text{JTG\_TRST}}$	Input	**JTAG Reset.** JTAG test access port reset.
LP_ACK	InOut	**Acknowledge.** Provides handshaking. When the link port is configured as a receiver, ACK is an output. When the link port is configured as a transmitter, ACK is an input.
LP_CLK	InOut	**Clock.** When the link port is configured as a receiver, CLK is an input. When the link port is configured as a transmitter, CLK is an output.
LP_D[n]	InOut	**Data n.** Data bus. Input when receiving, output when transmitting.
MLB_CLK	InOut	**Single Ended Clock.**
MLB_CLKN	InOut	**Differential Clock (–).**
MLB_CLKOUT	InOut	**Single Ended Clock Out.**
MLB_CLKP	InOut	**Differential Clock (+).**
MLB_DAT	InOut	**Single Ended Data.**

Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
PPI0_D02	EPPI0 Data 2	D	PD_12
PPI0_D03	EPPI0 Data 3	D	PD_13
PPI0_D04	EPPI0 Data 4	D	PD_14
PPI0_D05	EPPI0 Data 5	D	PD_15
PPI0_D06	EPPI0 Data 6	C	PC_05
PPI0_D07	EPPI0 Data 7	D	PD_09
PPI0_D08	EPPI0 Data 8	C	PC_01
PPI0_D09	EPPI0 Data 9	C	PC_02
PPI0_D10	EPPI0 Data 10	C	PC_03
PPI0_D11	EPPI0 Data 11	C	PC_04
PPI0_D12	EPPI0 Data 12	E	PE_00
PPI0_D13	EPPI0 Data 13	C	PC_07
PPI0_D14	EPPI0 Data 14	C	PC_08
PPI0_D15	EPPI0 Data 15	E	PE_01
PPI0_FS1	EPPI0 Frame Sync 1 (HSYNC)	C	PC_14
PPI0_FS2	EPPI0 Frame Sync 2 (VSYNC)	C	PC_15
PPI0_FS3	EPPI0 Frame Sync 3 (FIELD)	C	PC_06
SPI0_CLK	SPI0 Clock	C	PC_01
SPI0_MISO	SPI0 Master In, Slave Out	C	PC_02
SPI0_MOSI	SPI0 Master Out, Slave In	C	PC_03
SPI0_RDY	SPI0 Ready	C	PC_05
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	C	PC_04
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	C	PC_05
$\overline{\text{SPI0\_SEL3}}$	SPI0 Slave Select Output 3	C	PC_06
$\overline{\text{SPI0\_SEL4}}$	SPI0 Slave Select Output 4	A	PA_09
$\overline{\text{SPI0\_SEL5}}$	SPI0 Slave Select Output 5	F	PF_05
$\overline{\text{SPI0\_SEL6}}$	SPI0 Slave Select Output 6	F	PF_04
$\overline{\text{SPI0\_SEL7}}$	SPI0 Slave Select Output 7	D	PD_05
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	C	PC_04
SPI1_CLK	SPI1 Clock	C	PC_07
SPI1_MISO	SPI1 Master In, Slave Out	C	PC_08
SPI1_MOSI	SPI1 Master Out, Slave In	C	PC_09
SPI1_RDY	SPI1 Ready	C	PC_11
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	C	PC_10
$\overline{\text{SPI1\_SEL2}}$	SPI1 Slave Select Output 2	C	PC_11
$\overline{\text{SPI1\_SEL3}}$	SPI1 Slave Select Output 3	F	PF_11
$\overline{\text{SPI1\_SEL4}}$	SPI1 Slave Select Output 4	A	PA_14
$\overline{\text{SPI1\_SEL5}}$	SPI1 Slave Select Output 5	B	PB_02
$\overline{\text{SPI1\_SEL6}}$	SPI1 Slave Select Output 6	D	PD_07
$\overline{\text{SPI1\_SEL7}}$	SPI1 Slave Select Output 7	D	PD_06
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	C	PC_10
SPI2_CLK	SPI2 Clock	B	PB_14
SPI2_D2	SPI2 Data 2	B	PB_12
SPI2_D3	SPI2 Data 3	B	PB_13
SPI2_MISO	SPI2 Master In, Slave Out	B	PB_10
SPI2_MOSI	SPI2 Master Out, Slave In	B	PB_11
SPI2_RDY	SPI2 Ready	C	PC_00
$\overline{\text{SPI2\_SEL1}}$	SPI2 Slave Select Output 1	B	PB_15

Table 17. Signal Multiplexing for Port E (Continued)

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_03	LP0_ACK				
PE_04	LP0_D0				
PE_05	LP0_D1				
PE_06	LP0_D2				
PE_07	LP0_D3				
PE_08	LP0_D4				
PE_09	LP0_D5				
PE_10	LP0_D6				
PE_11	LP0_D7				
PE_12	MSI0_D0		TM0_TMR0		
PE_13	MSI0_D1	C1_FLG0	CNT0_UD		
PE_14	MSI0_D2	$\overline{\text{UART1\_CTS}}$	TM0_TMR6		
PE_15	MSI0_D3	C2_FLG3			

Table 18. Signal Multiplexing for Port F

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PF_00	MSI0_D4	TRACE0_D00			
PF_01	MSI0_D5	TRACE0_D01			
PF_02	MSI0_D6	TRACE0_D02			
PF_03	MSI0_D7	TRACE0_D03			
PF_04	MSI0_CLK	C1_FLG2	$\overline{\text{SPI0\_SEL6}}$		
PF_05	ETH0_PTPCLKIN0	TM0_TMR1	$\overline{\text{SPI0\_SEL5}}$		
PF_06	ETH0_PTPAUXIN2	TRACE0_CLK			TM0_ACLK1
PF_07	ETH0_PTPAUXIN3	TM0_TMR2	MSI0_CMD		
PF_08	$\overline{\text{UART0\_TX}}$				
PF_09	$\overline{\text{UART0\_RX}}$				TM0_ACI0
PF_10	$\overline{\text{UART1\_TX}}$	$\overline{\text{SPI2\_SEL2}}$			
PF_11	$\overline{\text{UART1\_RX}}$	ACM0_A0	$\overline{\text{SPI1\_SEL3}}$	C2_FLG2	TM0_ACI1

Table 19 shows the internal timer signal routing. This table applies to both the 400-ball CSP_BGA and 176-lead LQFP packages.

Table 19. Internal Timer Signal Routing

Timer Input Signal	Internal Source
TM0_ACLK0[1]	SYS_CLKIN1
TM0_ACI5	DAI0_PB04_O
TM0_ACLK5	DAI0_PB03_O
TM0_ACI6	DAI0_PB20_O
TM0_ACLK6	DAI0_PB19_O
TM0_ACI7	CNT0_TO
TM0_ACLK7	SYS_CLKIN0

[1] Not applicable for LQFP package.

Table 20. ADSP-SC57x/ADSP-2157x 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
DAI0_PIN15	DAI0 Pin 15	Not Muxed	DAI0_PIN15
DAI0_PIN16	DAI0 Pin 16	Not Muxed	DAI0_PIN16
DAI0_PIN17	DAI0 Pin 17	Not Muxed	DAI0_PIN17
DAI0_PIN18	DAI0 Pin 18	Not Muxed	DAI0_PIN18
DAI0_PIN19	DAI0 Pin 19	Not Muxed	DAI0_PIN19
DAI0_PIN20	DAI0 Pin 20	Not Muxed	DAI0_PIN20
ETH0_COL	EMAC0 MII Collision detect	C	PC_06
ETH0_CRS	EMAC0 Carrier Sense/RMII Receive Data Valid	B	PB_01
ETH0_MDC	EMAC0 Management Channel Clock	A	PA_11
ETH0_MDIO	EMAC0 Management Channel Serial Data	A	PA_10
ETH0_PTPAUXIN0	EMAC0 PTP Auxiliary Trigger Input 0	D	PD_14
ETH0_PTPAUXIN1	EMAC0 PTP Auxiliary Trigger Input 1	D	PD_15
ETH0_PTPPPS0	EMAC0 PTP Pulse Per Second Output 0	A	PA_09
ETH0_PTPPPS1	EMAC0 PTP Pulse Per Second Output 1	D	PD_08
ETH0_RXCLK_REFCLK	EMAC0 RXCLK (10/100/1000) or REFCLK (10/100)	B	PB_00
ETH0_RXCTL_RXDV	EMAC0 RXCTL (10/100/1000) or CRS (10/100)	B	PB_01
ETH0_RXD0	EMAC0 Receive Data 0	A	PA_13
ETH0_RXD1	EMAC0 Receive Data 1	A	PA_12
ETH0_RXD2	EMAC0 Receive Data 2	A	PA_14
ETH0_RXD3	EMAC0 Receive Data 3	A	PA_15
ETH0_RXERR	EMAC0 Receive Error	B	PB_03
ETH0_TXCLK	EMAC0 Transmit Clock	B	PB_04
ETH0_TXCTL_TXEN	EMAC0 TXCTL (10/100/1000) or TXEN (10/100)	B	PB_09
ETH0_TXD0	EMAC0 Transmit Data 0	B	PB_07
ETH0_TXD1	EMAC0 Transmit Data 1	B	PB_08
ETH0_TXD2	EMAC0 Transmit Data 2	B	PB_06
ETH0_TXD3	EMAC0 Transmit Data 3	B	PB_05
HADC0_EOC_DOUT	HADC0 End of Conversion/Serial Data Out	D	PD_09
HADC0_VIN0	HADC0 Analog Input at channel 0	Not Muxed	HADC0_VIN0
HADC0_VIN1	HADC0 Analog Input at channel 1	Not Muxed	HADC0_VIN1
HADC0_VIN2	HADC0 Analog Input at channel 2	Not Muxed	HADC0_VIN2
HADC0_VIN3	HADC0 Analog Input at channel 3	Not Muxed	HADC0_VIN3
HADC0_VREFN	HADC0 Ground Reference for ADC	Not Muxed	HADC0_VREFN
HADC0_VREFP	HADC0 External Reference for ADC	Not Muxed	HADC0_VREFP
JTG_TCK	JTAG Clock	Not Muxed	JTG_TCK
JTG_TDI	JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	JTAG Serial Data Out	Not Muxed	JTG_TDO
JTG_TMS	JTAG Mode Select	Not Muxed	JTG_TMS
$\overline{\text{JTG\_TRST}}$	JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$
LP1_ACK	LP1 Acknowledge	B	PB_01
LP1_CLK	LP1 Clock	B	PB_03
LP1_D0	LP1 Data 0	D	PD_10
LP1_D1	LP1 Data 1	D	PD_11
LP1_D2	LP1 Data 2	D	PD_12
LP1_D3	LP1 Data 3	D	PD_13
LP1_D4	LP1 Data 4	D	PD_14
LP1_D5	LP1 Data 5	D	PD_15
LP1_D6	LP1 Data 6	A	PA_09

Table 20. ADSP-SC57x/ADSP-2157x 176-Lead LQFP Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TRACE0_D05	TRACE0 Trace Data	D	PD_11
TRACE0_D06	TRACE0 Trace Data	D	PD_12
TRACE0_D07	TRACE0 Trace Data 7	D	PD_13
TWI0_SCL	TWI0 Serial Clock	Not Muxed	TWI0_SCL
TWI0_SDA	TWI0 Serial Data	Not Muxed	TWI0_SDA
TWI1_SCL	TWI1 Serial Clock	Not Muxed	TWI1_SCL
TWI1_SDA	TWI1 Serial Data	Not Muxed	TWI1_SDA
TWI2_SCL	TWI2 Serial Clock	Not Muxed	TWI2_SCL
TWI2_SDA	TWI2 Serial Data	Not Muxed	TWI2_SDA
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	D	PD_06
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	D	PD_05
$\overline{\text{UART0\_RX}}$	UART0 Receive	A	PA_06
$\overline{\text{UART0\_TX}}$	UART0 Transmit	A	PA_05
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	D	PD_01
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	D	PD_00
$\overline{\text{UART1\_RX}}$	UART1 Receive	A	PA_08
$\overline{\text{UART1\_TX}}$	UART1 Transmit	A	PA_07
$\overline{\text{UART2\_CTS}}$	UART2 Clear to Send	A	PA_11
$\overline{\text{UART2\_RTS}}$	UART2 Request to Send	A	PA_10
$\overline{\text{UART2\_RX}}$	UART2 Receive	C	PC_13
$\overline{\text{UART2\_TX}}$	UART2 Transmit	C	PC_12

Table 23. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	SPI2_SEL3	SPI2_RDY			
PC_01	SPI0_CLK	PPI0_D08			TM0_ACLK2
PC_02	SPI0_MISO	PPI0_D09			
PC_03	SPI0_MOSI	PPI0_D10			TM0_CLK
PC_04	SPI0_SEL1	PPI0_D11			SPI0_SS
PC_05	SPI0_SEL2	PPI0_D06	SPI0_RDY		
PC_06	SPI0_SEL3	ETH0_COL	PPI0_FS3		
PC_07	SPI1_CLK				
PC_08	SPI1_MISO				
PC_09	SPI1_MOSI	C1_FLG2			
PC_10	SPI1_SEL1	C2_FLG2			SPI1_SS
PC_11	SPI1_SEL2	PPI0_CLK	SPI1_RDY		TM0_ACLK4
PC_12	CAN0_RX		UART2_TX		TM0_ACI2
PC_13	CAN0_TX		UART2_RX		TM0_ACI4
PC_14	CAN1_RX	PPI0_FS1	ACM0_A1	C2_FLG1	TM0_ACI3
PC_15	CAN1_TX	PPI0_FS2	ACM0_A2	TM0_TMR5	

Table 24. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00	C1_FLG0	UART1_RTS	CNT0_UD		
PD_01	C1_FLG1	UART1_CTS	TM0_TMR6		
PD_02	TM0_TMR0				
PD_03	TM0_TMR1	SPI0_SEL5			
PD_04	TM0_TMR2		SPI0_SEL6		
PD_05	SPI0_SEL7	C2_FLG3	UART0_RTS		
PD_06	SPI1_SEL7	C1_FLG3	UART0_CTS		
PD_07	SPI1_SEL6	CNT0_ZM	TM0_TMR7		
PD_08	ETH0_PTPPPS1	CNT0_DG	SPI2_SEL4		
PD_09	LP1_D7	PPI0_D07	HADC0_EOC_DOUT		TM0_ACLK3
PD_10	LP1_D0	PPI0_D00	TRACE0_D04		
PD_11	LP1_D1	PPI0_D01	TRACE0_D05		
PD_12	LP1_D2	PPI0_D02	TRACE0_D06		
PD_13	LP1_D3	PPI0_D03	TRACE0_D07		
PD_14	LP1_D4	PPI0_D04	ETH0_PTPAUXIN0		
PD_15	LP1_D5	PPI0_D05	ETH0_PTPAUXIN1		

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
DMC0_LDQS	InOut	C	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Lower Byte (complement) Notes: No notes
DMC0_ODT	Output	B	none	L	VDD_DMC	Desc: DMC0 On-die termination Notes: No notes
DMC0_RAS	Output	B	none	L	VDD_DMC	Desc: DMC0 Row Address Strobe Notes: No notes
DMC0_RESET	Output	B	none	L	VDD_DMC	Desc: DMC0 Reset (DDR3 only) Notes: No notes
DMC0_RZQ	a	B	none	none	VDD_DMC	Desc: DMC0 External calibration resistor connection Notes: Applicable for DDR2 and DDR3 only. Pull down using a 34 Ohm resistor.
DMC0_UDM	Output	B	none	L	VDD_DMC	Desc: DMC0 Data Mask for Upper Byte Notes: No notes
DMC0_UDQS	InOut	C	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte Notes: External weak pull-down required in LPDDR mode
DMC0_UDQS	InOut	C	none	none	VDD_DMC	Desc: DMC0 Data Strobe for Upper Byte (complement) Notes: No notes
DMC0_VREF	a		none	none	VDD_DMC	Desc: DMC0 Voltage Reference Notes: No notes
DMC0_WE	Output	B	none	L	VDD_DMC	Desc: DMC0 Write Enable Notes: No notes
GND	g		none	none		Desc: Ground Notes: No notes
HADC0_VIN0	a	NA	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 0 Notes: Connect to GND through a resistor if not used[4]
HADC0_VIN1	a	NA	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 1 Notes: Connect to GND through a resistor if not used[4]
HADC0_VIN2	a	NA	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 2 Notes: Connect to GND through a resistor if not used[4]
HADC0_VIN3	a	NA	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 3 Notes: Connect to GND through a resistor if not used[4]
HADC0_VIN4	a	NA	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 4 Notes: Connect to GND through a resistor if not used[4]
HADC0_VIN5	a	NA	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 5 Notes: Connect to GND through a resistor if not used[4]
HADC0_VIN6	a	NA	none	none	VDD_HADC	Desc: HADC0 Analog Input at channel 6 Notes: Connect to GND through a resistor if not used[4]

SPECIFICATIONS

For information about product specifications, contact your Analog Devices representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	CCLK ≤ 450 MHz	1.05	1.10	1.15	V
		CCLK ≤ 500 MHz	1.10	1.15	1.20	V
V_{DD_EXT}	External (I/O) Supply Voltage		3.13	3.3	3.47	V
V_{DD_HADC}	Analog Power Supply Voltage		3.13	3.3	3.47	V
V_{DD_DMC}[1]	DDR2/LPDDR Controller Supply Voltage		1.7	1.8	1.9	V
	DDR3 Controller Supply Voltage		1.425	1.5	1.575	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage Applies to the DMC0_VREF pin		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{HADC0_VINx}	HADC Input Voltage		0		V_{HADC_REF} + 0.2	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.0			V
V_{IHTWI}[5, 6]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{ILTWI}[5, 6]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.3 × $V_{VBUSTWI}$	V
V_{IL_DDR2}[7]	Low Level Input Voltage	V_{DD_DMC} = 1.7 V			V_{REF} – 0.25	V
V_{IL_DDR3}[7]	Low Level Input Voltage	V_{DD_DMC} = 1.425 V			V_{REF} – 0.175	V
V_{IH_DDR2}[7]	High Level Input Voltage	V_{DD_DMC} = 1.9 V	V_{REF} + 0.25			V
V_{IH_DDR3}[7]	High Level Input Voltage	V_{DD_DMC} = 1.575 V	V_{REF} + 0.175			V
V_{IL_LPDDR}[8]	Low Level Input Voltage	V_{DD_DMC} = 1.7 V			0.2 × V_{DD_DMC}	V
V_{IH_LPDDR}[8]	High Level Input Voltage	V_{DD_DMC} = 1.9 V	0.8 × V_{DD_DMC}			V
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 450 MHz	0		95	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = –40°C to +100°C CCLK ≤ 450 MHz	–40		+125	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 450 MHz	0		90	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = –40°C to +105°C CCLK ≤ 450 MHz	–40		+125	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 500 MHz	0		100	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = –40°C to +95°C CCLK ≤ 500 MHz	–40		+125	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 500 MHz	0		95	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = –40°C to +100°C CCLK ≤ 500 MHz	–40		+125	°C

Clock and Reset Timing

Table 42 and Figure 9 describe clock and reset operations related to the CGU and RCU. Per the CCLK, SYSCLK, SCLK, DCLK, and OCLK timing specifications in Table 27, combinations of SYS_CLKIN and clock multipliers must not select clock rates in excess of the maximum instruction rate of the processor.

Table 42. Clock and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
f_{CKIN}	SYS_CLKINx Frequency (Crystal)[1, 2, 3]	20	50	MHz
	SYS_CLKINx Frequency (External CLKIN)[1, 2, 3]	20	50	MHz
t_{CKINL}	CLKIN Low Pulse[1]	10		ns
t_{CKINH}	CLKIN High Pulse[1]	10		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[4]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 9) equals $1/f_{CKIN}$.
[3] If the CGU_CTL.DF bit is set, the minimum f_{CKIN} specification is 40 MHz.
[4] Applies after power-up sequence is complete. See Table 41 and Figure 8 for power-up reset timing.

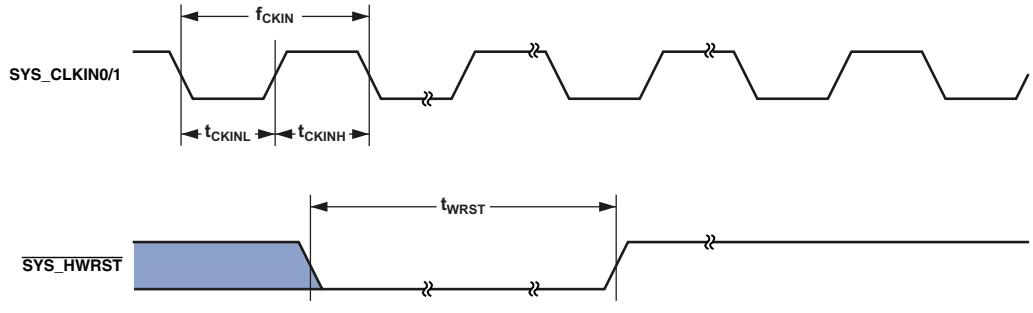

Figure 9. Clock and Reset Timing

DDR2 SDRAM Read Cycle Timing

Table 44 and Figure 11 show DDR2 SDRAM read cycle timing, related to the DMC.

Table 44. DDR2 SDRAM Read Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		400 MHz[1]		Unit
		Min	Max	
Timing Requirements				
t_{DQSQ}	DMC0_DQS to DMC0_DQ Skew for DMC0_DQS and Associated DMC0_DQxx Signals		0.2	ns
t_{QH}	DMC0_DQxx, DMC0_DQS Output Hold Time From DMC0_DQS	0.8		ns
t_{RPRE}	Read Preamble	0.9		t_{CK}
t_{RPST}	Read Postamble	0.4		t_{CK}

[1] To ensure proper operation of DDR2, all the DDR2 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).

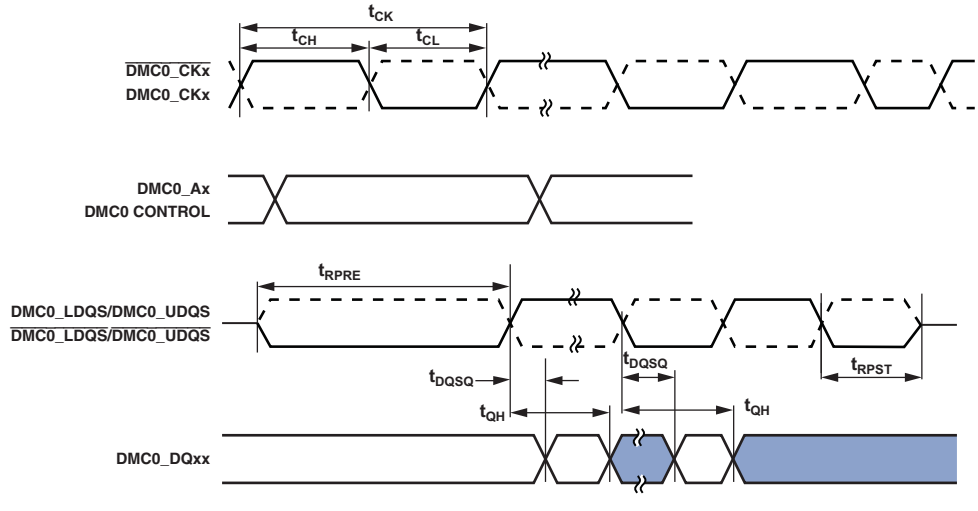

Figure 11. DDR2 SDRAM Controller Input AC Timing

DDR3 SDRAM Clock and Control Cycle Timing

Table 49 and Figure 16 show mobile DDR3 SDRAM clock and control cycle timing, related to the DMC.

Table 49. DDR3 SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.5 V

Parameter		450 MHz[1]		Unit
		Min	Max	
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.22		ns
$t_{CH(abs)}$[2]	Minimum Clock Pulse Width	0.47	0.53	t_{CK}
$t_{CL(abs)}$[2]	Maximum Clock Pulse Width	0.47	0.53	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	0.2		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	0.275		ns

[1] To ensure proper operation of the DDR3, all the DDR3 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[2] As per JESD79-3F definition.

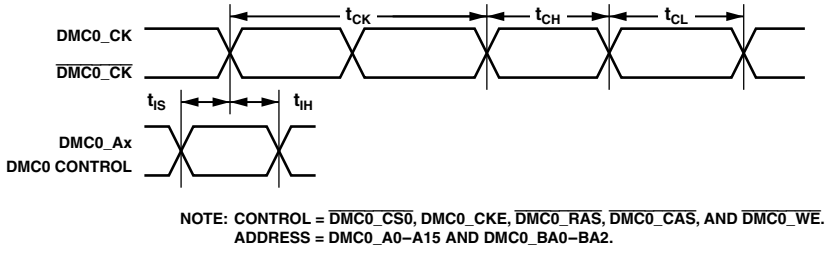

Figure 16. DDR3 SDRAM Clock and Control Cycle Timing

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 88. Input signals are routed to the DAI0_PINx pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI0_PINx pins.

Table 88. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

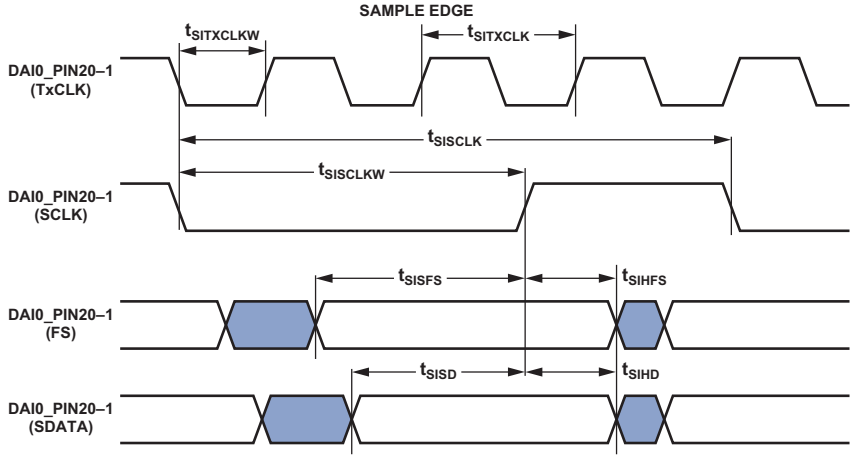

Figure 58. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 89. Oversampling Clock (TxCLK) Switching Characteristics

Parameter		Max	Unit
Switching Characteristics			
f_{TXCLK_384}	Frequency for TxCLK = 384 × Frame Sync	Oversampling ratio × frame sync ≤ $1/t_{SITXCLK}$	MHz
f_{TXCLK_256}	Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
f_{FS}	Frame Rate (FS)	192.0	kHz

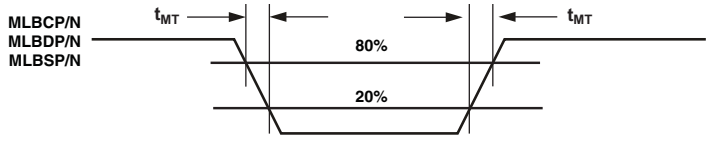

Figure 61. MLB 6-Pin Transition Time

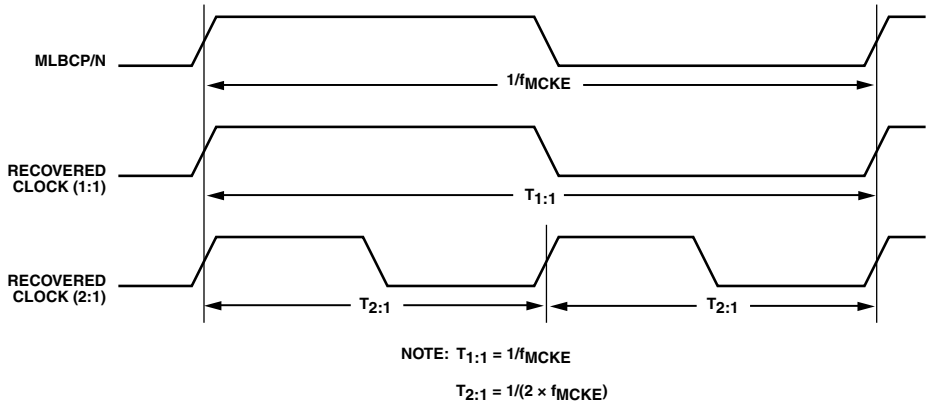

Figure 62. MLB 6-Pin Clock Definitions

Debug Interface (JTAG Emulation Port) Timing

Table 95 and Figure 67 provide I/O timing related to the debug interface (JTAG Emulator Port).

Table 95. JTAG Emulation Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	JTG_TCK Period	20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	12		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (measured in JTG_TCK cycles)[2]	4		T_{CK}
Switching Characteristics				
t_{DTDO}	JTG_TDO Delay From JTG_TCK Low		13.5	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		17	ns

[1] System Inputs = MLB0_CLKP, MLB0_DATP, MLB0_SIGP, DAI0_PIN20-01, DMC0_A15-0, DMC0_DQ15-0, $\overline{\text{DMC0\_RESET}}$, PA_15-0, PB_15-0, PC_15-0, PD_15-0, PE_15-0, PF_11-0, SYS_BMODE2-0, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$, TWI2-0_SCL, TWI2-0_SDA2.

[2] 50 MHz maximum.

[3] System Outputs = DMC0_A15-0, DMC0_BA2-0, $\overline{\text{DMC0\_CAS}}$, DMC0_CK, DMC0_CKE, $\overline{\text{DMC0\_CS0}}$, DMC0_DQ15-0, DMC0_LDM, DMC0_LDQS, DMC0_ODT, $\overline{\text{DMC0\_RAS}}$, $\overline{\text{DMC0\_RESET}}$, DMC0_UDM, DMC0_UDQS, $\overline{\text{DMC0\_WE}}$, MLB0_DATP, MLB0_SIGP, PA_15-0, PB_15-0, PC_15-0, PD_15-0, PE_15-0, PF_11-0, SYS_BMODE2-0, SYS_CLKOUT, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$.

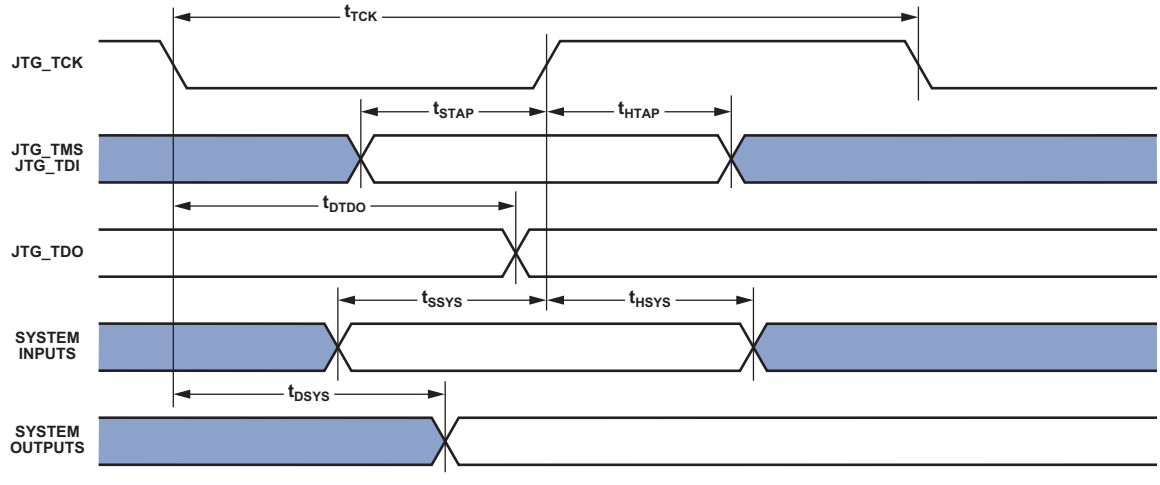

Figure 67. JTAG Port Timing

Ball No.	Pin Name
V17	DMC0_BA1
V18	GND
V19	DMC0_A04
V20	DMC0_A05
W01	TWI2_SCL
W02	GND
W03	DMC0_DQ12
W04	DMC0_DQ11
W05	DMC0_DQ09
W06	PD_02
W07	PD_00
W08	PA_07
W09	PA_06
W10	PA_04
W11	DMC0_DQ05
W12	DMC0_DQ04
W13	DMC0_DQ03
W14	DMC0_DQ02
W15	$\overline{\text{SYS\_FAULT}}$
W16	DMC0_ODT
W17	DMC0_A08
W18	SYS_BMODE1
W19	GND
W20	DMC0_A07
Y01	GND
Y02	$\overline{\text{DMC0\_UDQS}}$
Y03	DMC0_UDQS
Y04	DMC0_DQ10
Y05	DMC0_DQ08
Y06	DMC0_UDM
Y07	DMC0_LDM
Y08	DMC0_CK
Y09	$\overline{\text{DMC0\_CK}}$
Y10	DMC0_DQ07
Y11	DMC0_DQ06
Y12	DMC0_LDQS
Y13	$\overline{\text{DMC0\_LDQS}}$
Y14	DMC0_DQ01
Y15	DMC0_DQ00
Y16	DMC0_CKE
Y17	$\overline{\text{DMC0\_CS0}}$
Y18	SYS_BMODE0
Y19	SYS_BMODE2
Y20	GND

Lead No.	Pin Name
161	PB_08
162	PB_07
163	VDD_INT
164	VDD_EXT
165	PB_06
166	PB_05
167	VDD_EXT
168	PB_04
169	PB_03
170	VDD_INT
171	VDD_EXT
172	PB_02
173	PB_01
174	PB_00
175	VDD_INT
176	GND
177[1]	GND

[1] Pin177 is the GND supply (see Figure 91) for the processor; this pad must connect to GND.

ORDERING GUIDE

Model[1, 2]	Processor Instruction Rate (Max)	ARM Instruction Rate (Max)[3]	Temperature Range[4]	ARM Cores[3]	SHARC+ Cores	External Memory Ports	Package Description	Package Option
ADSP-21571KSWZ-4	450 MHz	N/A	0°C to +70°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571BSWZ-4	450 MHz	N/A	–40°C to +85°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571CSWZ-4	450 MHz	N/A	–40°C to +105°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571KSWZ-5	500 MHz	N/A	0°C to +70°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571BSWZ-5	500 MHz	N/A	–40°C to +85°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571CSWZ-5	500 MHz	N/A	–40°C to +100°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21573KBCZ-4	450 MHz	N/A	0°C to +70°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573BBCZ-4	450 MHz	N/A	–40°C to +85°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573CBCZ-4	450 MHz	N/A	–40°C to +100°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573KBCZ-5	500 MHz	N/A	0°C to +70°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573BBCZ-5	500 MHz	N/A	–40°C to +85°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573CBCZ-5	500 MHz	N/A	–40°C to +95°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC570KSWZ-42	450 MHz	225 MHz	0°C to +70°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570BSWZ-42	450 MHz	225 MHz	–40°C to +85°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570CSWZ-42	450 MHz	225 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570KSWZ-4	450 MHz	450 MHz	0°C to +70°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570BSWZ-4	450 MHz	450 MHz	–40°C to +85°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570CSWZ-4	450 MHz	450 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571KSWZ-3	300 MHz	300 MHz	0°C to +70°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571BSWZ-3	300 MHz	300 MHz	–40°C to +85°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571CSWZ-3	300 MHz	300 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571KSWZ-4	450 MHz	450 MHz	0°C to +70°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571BSWZ-4	450 MHz	450 MHz	–40°C to +85°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571CSWZ-4	450 MHz	450 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571KSWZ-5	500 MHz	500 MHz	0°C to +70°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571BSWZ-5	500 MHz	500 MHz	–40°C to +85°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571CSWZ-5	500 MHz	500 MHz	–40°C to +100°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC572KBCZ-42	450 MHz	225 MHz	0°C to +70°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572BBCZ-42	450 MHz	225 MHz	–40°C to +85°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572CBCZ-42	450 MHz	225 MHz	–40°C to +100°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572KBCZ-4	450 MHz	450 MHz	0°C to +70°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572BBCZ-4	450 MHz	450 MHz	–40°C to +85°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572CBCZ-4	450 MHz	450 MHz	–40°C to +100°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573KBCZ-3	300 MHz	300 MHz	0°C to +70°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573BBCZ-3	300 MHz	300 MHz	–40°C to +85°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573CBCZ-3	300 MHz	300 MHz	–40°C to +100°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573KBCZ-4	450 MHz	450 MHz	0°C to +70°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573BBCZ-4	450 MHz	450 MHz	–40°C to +85°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573CBCZ-4	450 MHz	450 MHz	–40°C to +100°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573KBCZ-5	500 MHz	500 MHz	0°C to +70°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573BBCZ-5	500 MHz	500 MHz	–40°C to +85°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573CBCZ-5	500 MHz	500 MHz	–40°C to +95°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2

[1] Z =RoHS Compliant Part.

[2] For evaluation of all models, order the ADZS-SC573-EZLITE evaluation board.

[3] N/A means not applicable.

[4] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.