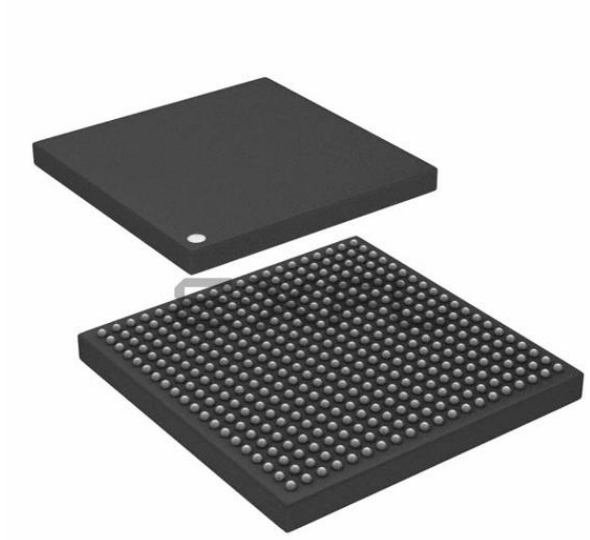

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	300MHz, 300MHz
Non-Volatile Memory	External
On-Chip RAM	2MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 100°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc573cbcz-3

Table 2. Comparison of ADSP-SC57x/ADSP-2157x Processor Features[1]

Processor Feature		ADSP-SC570	ADSP-SC571	ADSP-SC572	ADSP-SC573	ADSP-21571	ADSP-21573
ARM Cortex-A5 (MHz, Max)		450	500	450	500	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	500	450	500	500	500
SHARC+ Core2 (MHz, Max)		N/A	500	N/A	500	500	500
SHARC L1 SRAM (kB)		1 × 384	2 × 384	1 × 384	2 × 384	2 × 384	2 × 384
System Memory	L2 SRAM (Shared) (MB)	1	1	1	1	1	1
	DDR3/DDR2/LPDDR1 Controller (16-bit)	N/A	N/A	1	1	N/A	1
USB 2.0 HS + PHY (Host/Device/OTG)		N/A	N/A	1	1	N/A	N/A
EMAC Std/AVB + Timer IEEE 1588		10/100	10/100	10/100/1000	10/100/1000	N/A	N/A
SDIO/eMMC		N/A	N/A	1	1	N/A	N/A
Link Ports		1	1	2	2	1	2
GPIO Ports		Port A to D	Port A to D	Port A to F	Port A to F	Port A to D	Port A to F
GPIO + DAI Pins		64 + 20	64 + 20	92 + 20	92 + 20	64 + 20	92 + 20
Package Options		176-LQFP	176-LQFP	400-BGA	400-BGA	176-LQFP	400-BGA

[1] N/A means not applicable.

Table 3. Comparison of ADSP-SC57x/ADSP-2157x Processor Features for Automotive [1]

Processor Feature		ADSP-SC570W	ADSP-SC571W	ADSP-SC572W	ADSP-SC573W	ADSP-21571W	ADSP-21573W
ARM Cortex-A5 (MHz, Max)		450	500	450	500	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	500	450	500	500	500
SHARC+ Core2 (MHz, Max)		N/A	500	N/A	500	500	500
SHARC L1 SRAM (kB)		1 × 384	2 × 384	1 × 384	2 × 384	2 × 384	2 × 384
System Memory	L2 SRAM (Shared) (MB)	1	1	1	1	1	1
	DDR3/DDR2/LPDDR1 Controller (16-bit)	N/A	N/A	1	1	N/A	1
USB 2.0 HS + PHY (Host/Device/OTG)		N/A	N/A	1	1	N/A	N/A
EMAC Std/AVB + Timer IEEE 1588		10/100	10/100	10/100/1000	10/100/1000	N/A	N/A
SDIO/eMMC		N/A	N/A	1	1	N/A	N/A
MLB 3-Pin/6-Pin		3-pin	3-pin	6-pin/3-pin	6-pin/3-pin	3-pin	6-pin/3-pin
Link Ports		1	1	2	2	1	2
GPIO Ports		Port A to D	Port A to D	Port A to F	Port A to F	Port A to D	Port A to F
GPIO + DAI Pins		64 + 20	64 + 20	92 + 20	92 + 20	64 + 20	92 + 20
Package Options		176-LQFP	176-LQFP	400-BGA	400-BGA	176-LQFP	400-BGA

[1] N/A means not applicable.

Table 8. DMC Memory Map[1]

	Byte Address Space ARM Cortex-A5—Data Access and Instruction Fetch SHARC+—Data Access	Normal Word Address Space SHARC+ Data Access	VISA Address Space SHARC+ Instruction Fetch	ISA Address Space SHARC+ Instruction Fetch
DMC0 (1 GB)	0x80000000–0x805FFFFF	0x10000000–0x17FFFFFF	Not applicable	0x00400000–0x004FFFFF
	0x80600000–0x809FFFFF		Not applicable	Not applicable
	0x80A00000–0x80FFFFFF		0x00800000–0x00AFFFFF	Not applicable
	0x81000000–0x9FFFFFFF		Not applicable	Not applicable
	0xA0000000–0xBFFFFFFF	Not applicable	Not applicable	Not applicable

[1] The ARM Cortex-A5 can access the entire byte address space. The SHARC+ VISA/ISA address space for instruction fetch and the normal word address space for data access do not cover the entire byte address space.

System Crossbars (SCBs)

The system crossbars (SCBs) are the fundamental building blocks of a switch fabric style for on-chip system bus interconnection. The SCBs connect system bus masters to system bus slaves, providing concurrent data transfer between multiple bus masters and multiple bus slaves. A hierarchical model—built from multiple SCBs—provides a power and area efficient system interconnection.

The SCBs provide the following features:

- Highly efficient, pipelined bus transfer protocol for sustained throughput
- Full-duplex bus operation for flexibility and reduced latency
- Concurrent bus transfer support to allow multiple bus masters to access bus slaves simultaneously
- Protection model (privileged/secure) support for selective bus interconnect protection

Direct Memory Access (DMA)

The processors use direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processors can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory to memory DMA stream uses two channels: the source channel and the destination channel.

All DMA channels can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers: descriptor-based or register-based. Register-based DMA allows the processors to program DMA control registers directly to initiate a DMA transfer. On completion, the DMA control registers automatically update with original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together. Program a DMA channel to set up and start another DMA transfer automatically after the current sequence completes.

The DMA engine supports the following DMA operations:

- A single linear buffer that stops on completion
- A linear buffer with negative, positive, or zero stride length
- A circular autorefreshing buffer that interrupts when each buffer becomes full
- A similar circular buffer that interrupts on fractional buffers, such as at the halfway point
- The 1D DMA uses a set of identical ping pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address
- The 1D DMA uses a linked list of four-word descriptor sets containing a link pointer, an address, a length, and a configuration
- The 2D DMA uses an array of one-word descriptor sets, specifying only the base DMA address
- The 2D DMA uses a linked list of multiword descriptor sets, specifying all configurable parameters

Memory Direct Memory Access (MDMA)

The processor supports various memory direct memory access (MDMA) operations, including,

- Enhanced bandwidth MDMA channels with CRC protection (32-bit bus width, run on SYSCLK)
- Enhanced bandwidth MDMA channel (32-bit bus width, runs on SYSCLK)
- Maximum bandwidth MDMA channel (64-bit bus width, runs on SYCLK)

Extended Memory DMA

Extended memory DMA supports various operating modes, such as delay line (which allows processor reads and writes to external delay line buffers and to the external memory), with limited core interaction and scatter/gather DMA (writes to and from noncontiguous memory blocks).

Cyclic Redundant Code (CRC) Protection

The cyclic redundant codes (CRC) protection modules allow system software to calculate the signature of code, data, or both in memory, the content of memory-mapped registers, or

periodic communication message objects. Dedicated hardware circuitry compares the signature with precalculated values and triggers appropriate fault events.

For example, every 100 ms the system software initiates the signature calculation of the entire memory contents and compares these contents with expected, precalculated values. If a mismatch occurs, a fault condition is generated through the processor core or the trigger routing unit.

The CRC is a hardware module based on a CRC32 engine that computes the CRC value of the 32-bit data-words presented to it. The source channel of the memory to memory DMA (in memory scan mode) provides data. The data can be optionally forwarded to the destination channel (memory transfer mode). The main features of the CRC peripheral are as follows:

- Memory scan mode
- Memory transfer mode
- Data verify mode
- Data fill mode
- User-programmable CRC32 polynomial
- Bit and byte mirroring option (endianness)
- Fault and error interrupt mechanisms
- 1D and 2D fill block to initialize an array with constants
- 32-bit CRC signature of a block of a memory or an MMR block

Event Handling

The processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing a higher priority event takes precedence over servicing a lower priority event.

The processors provide support for four different types of events:

- An emulation event causes the processors to enter emulation mode, allowing command and control of the processors through the JTAG interface.
- A reset event resets the processors.
- An exceptions event occurs synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions triggered on the one side by the SHARC+ core, such as data alignment (SIMD or long word) or compute violations (fixed or floating point), and illegal instructions cause core exceptions. Conditions triggered on the other side by the SEC, such as error correcting codes (ECC), parity, watchdog, or system clock, cause system exceptions.
- An interrupts event occurs asynchronously to program flow. They are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

System Event Controller (SEC)

Both SHARC+ cores feature a system event controller. The SEC features include the following:

- Comprehensive system event source management, including interrupt enable, fault enable, priority, core mapping, and source grouping
- A distributed programming model where each system event source control and all status fields are independent of each other
- Determinism where all system events have the same propagation delay and provide unique identification of a specific system event source
- A slave control port that provides access to all SEC registers for configuration, status, and interrupt and fault services
- Global locking that supports a register level protection model to prevent writes to locked registers
- Fault management including fault action configuration, time out, external indication, and system reset

Trigger Routing Unit (TRU)

The trigger routing unit (TRU) provides system level sequence control without core intervention. The TRU maps trigger masters (generators of triggers) to trigger slaves (receivers of triggers). Slave endpoints can be configured to respond to triggers in various ways. Common applications enabled by the TRU include,

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

SECURITY FEATURES

The following sections describe the security features of the ADSP-SC57x/ADSP-2157x processors.

ARM TrustZone

The ADSP-SC57x processors provide TrustZone technology that is integrated into the ARM Cortex-A5 processors. The TrustZone technology enables a secure state that is extended throughout the system fabric.

Cryptographic Hardware Accelerators

The ADSP-SC57x/ADSP-2157x processors support standards-based hardware accelerated encryption, decryption, authentication, and true random number generation.

Support for the hardware accelerated cryptographic ciphers includes the following:

- AES in ECB, CBC, ICM, and CTR modes with 128-bit, 192-bit, and 256-bit keys
- DES in ECB and CBC mode with 56-bit key
- 3DES in ECB and CBC mode with 3x 56-bit key
- ARC4 in stateful, stateless mode, up to 128-bit key

Support for the hardware accelerated hash functions includes the following:

- SHA-1
- SHA-2 with 224-bit and 256-bit digests
- HMAC transforms for SHA-1 and SHA-2
- MD5

Public key accelerator (PKA) is available to offload computation intensive public key cryptography operations.

Both a hardware-based nondeterministic random number generator and pseudorandom number generator are available.

Secure boot is also available with 224-bit elliptic curve digital signatures ensuring integrity and authenticity of the boot stream. Optionally, ensuring confidentiality through AES-128 encryption is available.

Employ secure debug to allow only trusted users to access the system with debug tools.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

System Protection Unit (SPU)

The system protection unit (SPU) guards against accidental or unwanted access to an MMR space of the peripheral by providing a write protection mechanism. The user can choose and configure the protected peripherals as well as configure which of the four system MMR masters (two SHARC+ cores, memory DMA, and CoreSight debug) the peripherals are guarded against.

The SPU is also part of the security infrastructure. Along with providing write protection functionality, the SPU is employed to define which resources in the system are secure or nonsecure as well as block access to secure resources from nonsecure masters.

System Memory Protection Unit (SMPU)

The system memory protection unit (SMPU) provides memory protection against read and/or write transactions to defined regions of memory. There are SMPU units in the ADSP-SC57x/ADSP-2157x processors for each memory space, except for SHARC L1 and SPI direct memory slave.

The SMPU is also part of the security infrastructure. It allows the user to protect against arbitrary read and/or write transactions and allows regions of memory to be defined as secure and prevent nonsecure masters from accessing those memory regions.

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

SAFETY FEATURES

The ADSP-SC57x/ADSP-2157x processors are designed to support functional safety applications. While the level of safety is mainly dominated by the system concept, the following primitives are provided by the processors to build a robust safety concept.

Multiparity Bit Protected SHARC+ Core L1 Memories

In the SHARC+ core L1 memory space, whether SRAM or cache, multiple parity bits protect each word to detect the single event upsets that occur in all RAMs. Parity also protects the cache tags and BTB.

Parity Protected ARM L1 Cache

In the ARM Cortex-A5 L1 cache space, each word is protected by multiple parity bits to detect the single event upsets that occur in all RAMs. Parity also protects the cache tags.

Error Correcting Codes (ECC) Protected L2 Memories

Error correcting codes (ECC) correct single event upsets. A single error correct/double error detect (SEC/DED) code protects the L2 memory. By default, ECC is enabled, but it can be disabled on a per bank basis. Single-bit errors correct transparently. If enabled, dual-bit errors can issue a system event or fault. ECC protection is fully transparent to the user, even if L2 memory is read or written by 8-bit or 16-bit entities.

Parity-Protected Peripheral Memories

Parity protection is added to all peripheral memories:

- ASRC
- IIR
- FIR
- USB
- CAN
- CRYPTO
- EMAC
- SDIO
- MLB
- TRACE

ADSP-SC57x/ADSP-2157x DETAILED SIGNAL DESCRIPTIONS

Table 11 provides a detailed description of each pin.

Table 11. ADSP-SC57x/ADSP-2157x Detailed Signal Descriptions

Signal Name	Direction	Description
ACM_A[n]	Output	**ADC Control Signals.** Function varies by mode.
ACM_T[n]	Input	**External Trigger n.** Input for external trigger events.
C1_FLG[n]	Output	**SHARC Core 1 Flag Pin.**
C2_FLG[n]	Output	**SHARC Core 2 Flag Pin.**
CAN_RX	Input	**Receive.** Typically an external CAN transceiver RX output.
CAN_TX	Output	**Transmit.** Typically an external CAN transceiver TX input.
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation, this input acts either as a count down signal or a gate signal. Count down—this input causes the GP counter to decrement. Gate—stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation, this input acts either as a count up signal or a direction signal. Count up—this input causes the GP counter to increment. Direction—selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DAI_PIN[nn]	InOut	**Pin n.** The digital applications interface (DAI0) connects various peripherals to any of the DAI0_PINxx pins. Programs make these connections using the signal routing unit (SRU).
DMC_A[nn]	Output	**Address n.** Address bus.
DMC_BA[n]	Output	**Bank Address n.** Defines which internal bank an activate, read, write or precharge command is applied to on the dynamic memory. Bank Address n also defines which mode registers (MR, EMR, EMR2, and/or EMR3) load during the load mode register command.
$\overline{\text{DMC\_CAS}}$	Output	**Column Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.
DMC_CK	Output	**Clock.** Outputs DCLK to external dynamic memory.
$\overline{\text{DMC\_CK}}$	Output	**Clock (Complement).** Complement of DMC_CK.
DMC_CKE	Output	**Clock Enable.** Active high clock enables. Connects to the CKE input of the dynamic memory.
$\overline{\text{DMC\_CS[n]}}$	Output	**Chip Select n.** Commands are recognized by the memory only when this signal is asserted.
DMC_DQ[nn]	InOut	**Data n.** Bidirectional data bus.
DMC_LDM	Output	**Data Mask for Lower Byte.** Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_LDQS	InOut	**Data Strobe for Lower Byte.** DMC_DQ07:DMC_DQ00 data strobe. Output with write data. Input with read data. Can be single-ended or differential depending on register settings.
$\overline{\text{DMC\_LDQS}}$	InOut	**Data Strobe for Lower Byte (Complement).** Complement of DMC_LDQS. Not used in single-ended mode.
DMC_ODT	Output	**On Die Termination.** Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled or disabled regardless of read or write commands.
$\overline{\text{DMC\_RAS}}$	Output	**Row Address Strobe.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.
$\overline{\text{DMC\_RESET}}$	Output	**Reset (DDR3 Only).**
DMC_RZQ	InOut	**External Calibration Resistor Connection.**
DMC_UDM	Output	**Data Mask for Upper Byte.** Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.
DMC_UDQS	InOut	**Data Strobe for Upper Byte.** DMC_DQ15:DMC_DQ08 data strobe. Output with write data. Input with read data. Can be single-ended or differential depending on register settings.

GPIO MULTIPLEXING FOR 400-BALL CSP_BGA PACKAGE

Table 13 through Table 18 identify the pin functions that are multiplexed on the GPIO pins of the 400-ball CSP_BGA package.

Table 13. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PA_00					
PA_01					
PA_02					
PA_03					
PA_04					
PA_05					
PA_06					
PA_07					
PA_08					
PA_09	ETH0_PTPPPS0	LP1_D6	$\overline{\text{SPI0\_SEL4}}$		
PA_10	ETH0_MDIO	$\overline{\text{UART2\_RTS}}$	$\overline{\text{SPI2\_SEL6}}$		
PA_11	ETH0_MDC	$\overline{\text{UART2\_CTS}}$			
PA_12	ETH0_RXD1				
PA_13	ETH0_RXD0				
PA_14	ETH0_RXD2	ACM0_A3	$\overline{\text{SPI1\_SEL4}}$		
PA_15	ETH0_RXD3	ACM0_T0	$\overline{\text{SPI2\_SEL5}}$		

Table 14. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PB_00	ETH0_RXCLK_REFCLK	C2_FLG0			
PB_01	ETH0_CRS	ACM0_A4	LP1_ACK	TM0_TMR3	
PB_02	ETH0_RXCTL_RXDV		$\overline{\text{SPI1\_SEL5}}$		
PB_03	ETH0_RXERR	MLB0_CLKOUT	LP1_CLK	TM0_TMR4	
PB_04	ETH0_TXCLK	MLB0_DAT			
PB_05	ETH0_TXD3	MLB0_SIG			
PB_06	ETH0_TXD2	MLB0_CLK			
PB_07	ETH0_TXD0		$\overline{\text{SPI2\_SEL7}}$		
PB_08	ETH0_TXD1				
PB_09	ETH0_TXCTL_TXEN				
PB_10	SPI2_MISO				
PB_11	SPI2_MOSI				
PB_12	SPI2_D2				
PB_13	SPI2_D3				
PB_14	SPI2_CLK				
PB_15	$\overline{\text{SPI2\_SEL1}}$				$\overline{\text{SPI2\_SS}}$

Table 15. Signal Multiplexing for Port C

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PC_00	SPI2_SEL3	SPI2_RDY			
PC_01	SPI0_CLK	PPI0_D08			TM0_ACLK2
PC_02	SPI0_MISO	PPI0_D09			
PC_03	SPI0_MOSI	PPI0_D10			TM0_CLK
PC_04	SPI0_SEL1	PPI0_D11			SPI0_SS
PC_05	SPI0_SEL2	PPI0_D06	SPI0_RDY		
PC_06	SPI0_SEL3	ETH0_COL	PPI0_FS3		
PC_07	SPI1_CLK	PPI0_D13			
PC_08	SPI1_MISO	PPI0_D14			
PC_09	SPI1_MOSI				
PC_10	SPI1_SEL1				SPI1_SS
PC_11	SPI1_SEL2	PPI0_CLK	SPI1_RDY		TM0_ACLK4
PC_12	CAN0_RX	MSI0_CD	UART2_TX		TM0_ACI2
PC_13	CAN0_TX	MSI0_INT	UART2_RX		TM0_ACI4
PC_14	CAN1_RX	PPI0_FS1	ACM0_A1	C2_FLG1	TM0_ACI3
PC_15	CAN1_TX	PPI0_FS2	ACM0_A2	TM0_TMR5	

Table 16. Signal Multiplexing for Port D

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PD_00					
PD_01					
PD_02					
PD_03					
PD_04					
PD_05	SPI0_SEL7		UART0_RTS		
PD_06	SPI1_SEL7	C1_FLG3	UART0_CTS		
PD_07	SPI1_SEL6	CNT0_ZM	TM0_TMR7		
PD_08	ETH0_PTPPPS1	CNT0_DG	SPI2_SEL4		
PD_09	LP1_D7	PPI0_D07	HADC0_EOC_DOUT		TM0_ACLK3
PD_10	LP1_D0	PPI0_D00	TRACE0_D04		
PD_11	LP1_D1	PPI0_D01	TRACE0_D05		
PD_12	LP1_D2	PPI0_D02	TRACE0_D06		
PD_13	LP1_D3	PPI0_D03	TRACE0_D07		
PD_14	LP1_D4	PPI0_D04	ETH0_PTPAUXIN0		
PD_15	LP1_D5	PPI0_D05	ETH0_PTPAUXIN1		

Table 17. Signal Multiplexing for Port E

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function Input Tap
PE_00	ETH0_PTPPPS2	PPI0_D12	UART1_RTS		
PE_01	ETH0_PTPPPS3	PPI0_D15	C1_FLG1		
PE_02	LP0_CLK				

SPECIFICATIONS

For information about product specifications, contact your Analog Devices representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	CCLK ≤ 450 MHz	1.05	1.10	1.15	V
		CCLK ≤ 500 MHz	1.10	1.15	1.20	V
V_{DD_EXT}	External (I/O) Supply Voltage		3.13	3.3	3.47	V
V_{DD_HADC}	Analog Power Supply Voltage		3.13	3.3	3.47	V
V_{DD_DMC}[1]	DDR2/LPDDR Controller Supply Voltage		1.7	1.8	1.9	V
	DDR3 Controller Supply Voltage		1.425	1.5	1.575	V
V_{DD_USB}[2]	USB Supply Voltage		3.13	3.3	3.47	V
V_{DDR_VREF}	DDR2 Reference Voltage Applies to the DMC0_VREF pin		0.49 × V_{DD_DMC}	0.50 × V_{DD_DMC}	0.51 × V_{DD_DMC}	V
V_{HADC_REF}[3]	HADC Reference Voltage		2.5	3.30	V_{DD_HADC}	V
V_{HADC0_VINx}	HADC Input Voltage		0		V_{HADC_REF} + 0.2	V
V_{IH}[4]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.0			V
V_{IHTWI}[5, 6]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	0.7 × $V_{VBUSTWI}$		$V_{VBUSTWI}$	V
V_{IL}[4]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.8	V
V_{ILTWI}[5, 6]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.3 × $V_{VBUSTWI}$	V
V_{IL_DDR2}[7]	Low Level Input Voltage	V_{DD_DMC} = 1.7 V			V_{REF} – 0.25	V
V_{IL_DDR3}[7]	Low Level Input Voltage	V_{DD_DMC} = 1.425 V			V_{REF} – 0.175	V
V_{IH_DDR2}[7]	High Level Input Voltage	V_{DD_DMC} = 1.9 V	V_{REF} + 0.25			V
V_{IH_DDR3}[7]	High Level Input Voltage	V_{DD_DMC} = 1.575 V	V_{REF} + 0.175			V
V_{IL_LPDDR}[8]	Low Level Input Voltage	V_{DD_DMC} = 1.7 V			0.2 × V_{DD_DMC}	V
V_{IH_LPDDR}[8]	High Level Input Voltage	V_{DD_DMC} = 1.9 V	0.8 × V_{DD_DMC}			V
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 450 MHz	0		95	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = –40°C to +100°C CCLK ≤ 450 MHz	–40		+125	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 450 MHz	0		90	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = –40°C to +105°C CCLK ≤ 450 MHz	–40		+125	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 500 MHz	0		100	°C
T_J	Junction Temperature 400-Ball CSP_BGA	$T_{AMBIENT}$ = –40°C to +95°C CCLK ≤ 500 MHz	–40		+125	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = 0°C to +70°C CCLK ≤ 500 MHz	0		95	°C
T_J	Junction Temperature 176-Lead LQFP-EP	$T_{AMBIENT}$ = –40°C to +100°C CCLK ≤ 500 MHz	–40		+125	°C

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Power-Up Reset Timing

Table 41 and Figure 8 show the relationship between power supply startup and processor reset timing, related to the clock generation unit (CGU) and reset control unit (RCU).

In Figure 8, $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, and V_{DD_HADC}.

Table 41. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{SYS\_HWRST}$ Deasserted after $V_{DD\_SUPPLIES}$ (V_{DD_INT}, V_{DD_EXT}, V_{DD_DMC}, V_{DD_USB}, V_{DD_HADC}) and SYS_CLKINx are Stable and within Specification	$11 \times t_{CKIN}$		ns

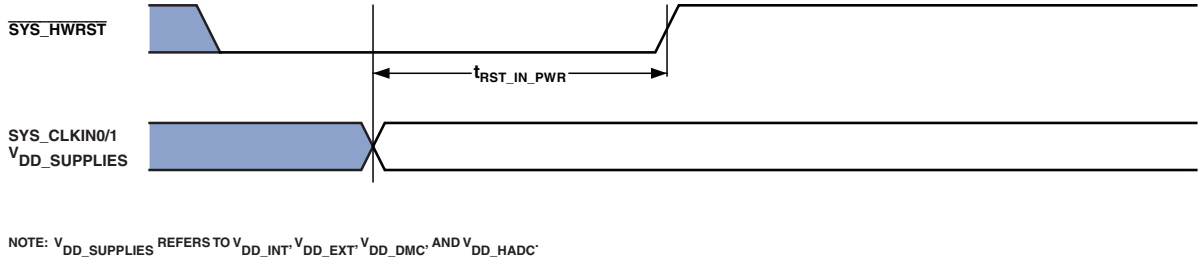


Figure 8. Power-Up Reset Timing

DDR2 SDRAM Write Cycle Timing

Table 45 and Figure 12 show DDR2 SDRAM write cycle timing, related to the DMC.

Table 45. DDR2 SDRAM Write Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		400 MHz[1]		Unit
		Min	Max	
Switching Characteristics				
t_{DQSS}	DMC0_DQS Latching Rising Transitions to Associated Clock Edges[2]	–0.15	+0.15	t_{CK}
t_{DS}	Last Data Valid to DMC0_DQS Delay	0.1		ns
t_{DH}	DMC0_DQS to First Data Invalid Delay	0.15		ns
t_{DSS}	DMC0_DQS Falling Edge to Clock Setup Time	0.2		t_{CK}
t_{DSH}	DMC0_DQS Falling Edge Hold Time From DMC0_CK	0.2		t_{CK}
t_{DQSH}	DMC0_DQS Input High Pulse Width	0.35		t_{CK}
t_{DQSL}	DMC0_DQS Input Low Pulse Width	0.35		t_{CK}
t_{WPRE}	Write Preamble	0.35		t_{CK}
t_{WPST}	Write Postamble	0.4		t_{CK}
t_{IPW}	Address and Control Output Pulse Width	0.6		t_{CK}
t_{DIPW}	DMC0_DQ and DMC0_DM Output Pulse Width	0.35		t_{CK}

[1] To ensure proper operation of the DDR2, all the DDR2 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[2] Write command to first DMC0_DQS delay = WL × t_{CK} + t_{DQSS}.

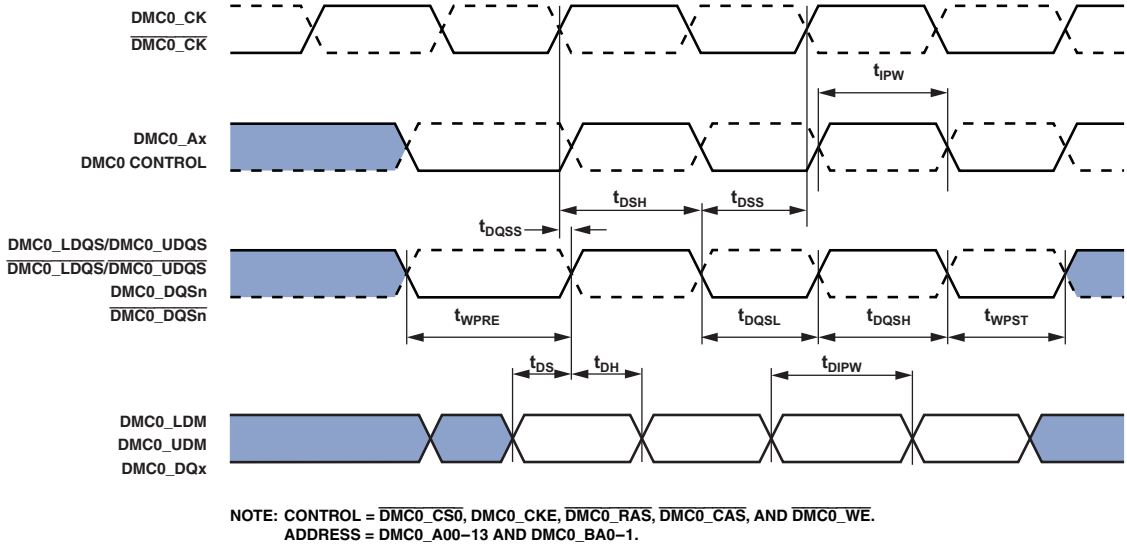


Figure 12. DDR2 SDRAM Controller Output AC Timing

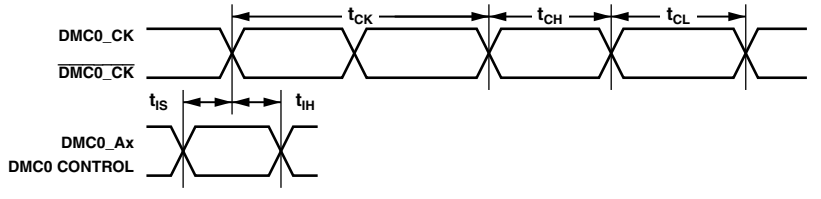
Mobile DDR (LPDDR) SDRAM Clock and Control Cycle Timing

Table 46 and Figure 13 show mobile DDR SDRAM clock and control cycle timing, related to the DMC.

Table 46. Mobile DDR SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.8 V

Parameter		200 MHz[1]		Unit
		Min	Max	
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	5		ns
t_{CH}	Minimum Clock Pulse Width	0.45	0.55	t_{CK}
t_{CL}	Maximum Clock Pulse Width	0.45	0.55	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	1		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	1		ns

[1] To ensure proper operation of LPDDR, all the LPDDR requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).



NOTE: CONTROL = DMC0_CS0, DMC0_CKE, DMC0_RAS, DMC0_CAS, AND DMC0_WE.
ADDRESS = DMC0_A0–A15 AND DMC0_BA0–BA2.

Figure 13. Mobile DDR SDRAM Clock and Control Cycle Timing

Link Ports (LPs)

In LP receive mode, the LP clock is supplied externally and is called $f_{LCLKREXT}$, therefore the period can be represented by

$$t_{LCLKREXT} = \frac{1}{f_{LCLKREXT}}$$

In LP transmit mode, the programmed LP clock ($f_{LCLKTPROG}$) frequency in megahertz is set by the following equation where VALUE is a field in the LP_DIV register that can be set from 1 to 255:

$$f_{LCLKTPROG} = \frac{f_{SCLK0}}{(VALUE \times 2)}$$

In the case where VALUE = 0, $f_{LCLKTPROG} = f_{SCLK0}$. For all settings of VALUE, the following equation is true:

$$t_{LCLKTPROG} = \frac{1}{f_{LCLKTPROG}}$$

Calculation of the link receiver data setup and hold relative to the link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LPx_Dx and LPx_CLK. Setup skew is the maximum delay that can be introduced in LPx_Dx relative to LPx_CLK (setup skew = $t_{LCLKTWH}$ minimum − t_{DLDCH} − t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LPx_CLK relative to LPx_Dx (hold skew = $t_{LCLKTWL}$ minimum − t_{HLDCH} − t_{HLDCL}).

Table 54. LPs—Receive[1]

Parameter		Min	Max	Unit
Timing Requirements				
$f_{LCLKREXT}$	LPx_CLK Frequency		112.5	MHz
t_{SLDCL}	Data Setup Before LPx_CLK Low	0.9		ns
t_{HLDCL}	Data Hold After LPx_CLK Low	1.4		ns
t_{LCLKEW}	LPx_CLK Period[2]	$t_{LCLKREXT}$ − 0.8		ns
$t_{LCLKRWL}$	LPx_CLK Width Low[2]	0.5 × $t_{LCLKREXT}$		ns
$t_{LCLKRWH}$	LPx_CLK Width High[2]	0.5 × $t_{LCLKREXT}$		ns
Switching Characteristic				
t_{DLALC}	LPx_ACK Low Delay After LPx_CLK Low[3]	1.5 × t_{SCLK0} + 4	2.5 × t_{SCLK0} + 12	ns

[1] Specifications apply to LP0 and LP1.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external LPx_CLK. For the external LPx_CLK ideal maximum frequency, see the $f_{LCLKTEXT}$ specification in Table 27.
[3] LPx_ACK goes low with t_{DLALC} relative to rise of LPx_CLK after first byte, but does not go low if the link buffer of the receiver is not about to fill.

SPI Port—Slave Timing

SPI0, SPI1, and SPI2

Table 65, Table 66, and Figure 37 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPIx_MOSI signal is also an output.
- In quad-mode data transmit, the SPIx_MOSI, SPIx_D2, and SPIx_D3 signals are also outputs.
- In dual-mode data receive, the SPIx_MISO signal is also an input.
- In quad-mode data receive, the SPIx_MISO, SPIx_D2, and SPIx_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

- Quad mode is supported by SPI2 only.
- CPHA is a configuration bit in the SPI_CTL register.

Table 65. SPI0, SPI1 Port—Slave Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	SPIx_CLK High Period[2]	$0.5 \times t_{SPICLKEXT} - 1.5$		ns
t_{SPICLS}	SPIx_CLK Low Period[2]	$0.5 \times t_{SPICLKEXT} - 1.5$		ns
t_{SPICLK}	SPIx_CLK Period[2]	$t_{SPICLKEXT} - 1.5$		ns
t_{HDS}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	$t_{SPICLKEXT} - 1.5$		ns
t_{SDSCI}	$\overline{\text{SPIx\_SS}}$ Assertion to First SPIx_CLK Edge	11.7		ns
t_{SSPID}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPIx_CLK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIx\_SS}}$ Assertion to Data Out Active	0	14.12	ns
t_{DSDHI}	$\overline{\text{SPIx\_SS}}$ Deassertion to Data High Impedance	0	12.6	ns
t_{DDSPID}	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		14.16	ns
t_{HDSPID}	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	1.5		ns

[1] All specifications apply to SPI0 and SPI1.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx_CLK. For the external SPIx_CLK ideal maximum frequency, see the $f_{SPICLKTEXT}$ specification in Table 27.

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference.

Controller Area Network (CAN) Interface

The CAN interface timing is described in the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference.

Universal Serial Bus (USB)

Table 78 describes the universal serial bus (USB) clock timing. Refer to the *USB 2.0 Specification* for timing and dc specifications for USB pins (including output characteristics for driver types E, F, and G listed in the ADSP-SC57x/ADSP-2157x Designer Quick Reference).

Table 78. USB Clock Timing[1]

Parameter		Min	Max	Unit
Timing Requirements				
f_{USBS}	USB_CLKIN Frequency	24	24	MHz
fs_{USB}	USB_CLKIN Clock Frequency Stability	–50	+50	ppm

[1] This specification is supported by USB0.

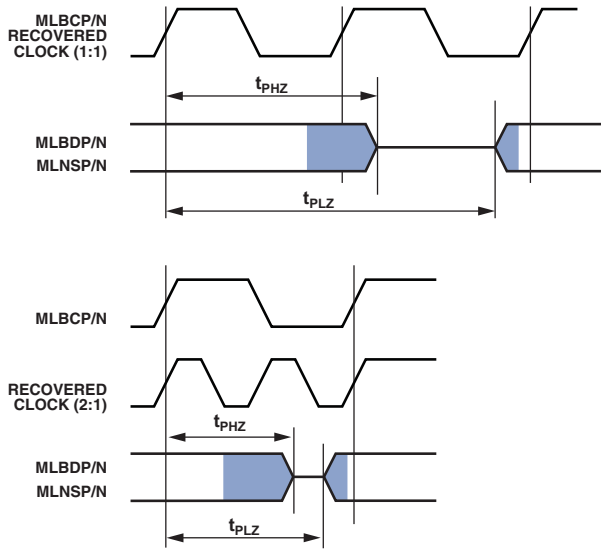


Figure 64. MLB 6-Pin Disable and Enable Turnaround Times

OUTPUT DRIVE CURRENTS

Figure 68 through Figure 80 show typical current-voltage characteristics for the output drivers of the ADSP-SC57x and ADSP-2157x processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

Output drive currents for MLB pins are compliant with MOST150 LVDS specifications. Output drive currents for USB pins are compliant with the USB 2.0 specifications.

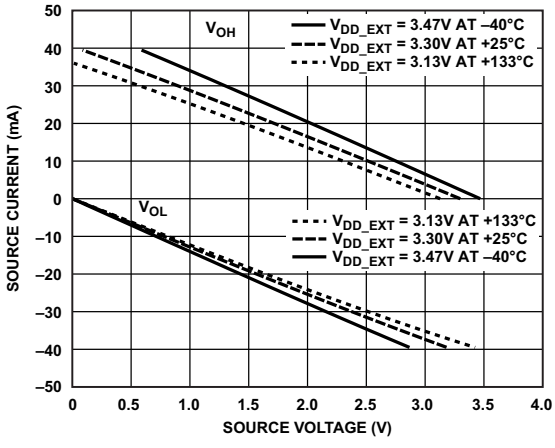


Figure 68. Driver Type A Current (3.3 V V_{DD_EXT})

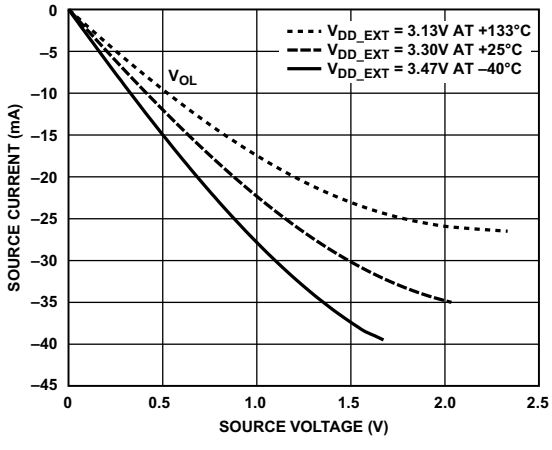


Figure 69. Driver Type D Current (3.3 V V_{DD_EXT})

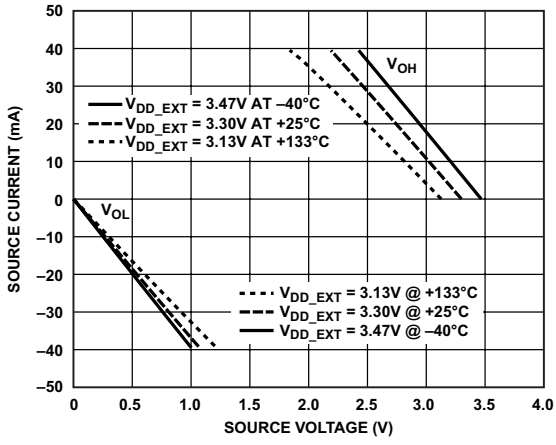


Figure 70. Driver Type H Current (3.3 V V_{DD_EXT})

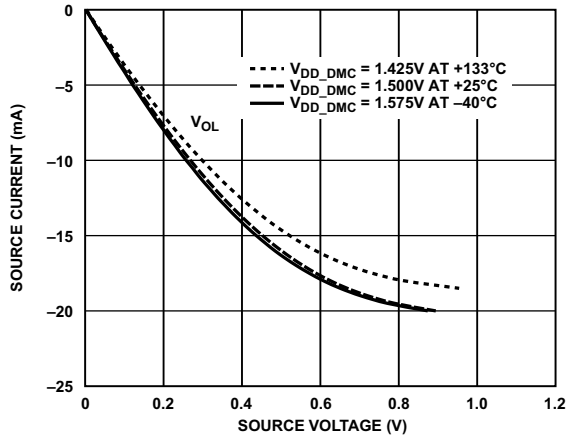


Figure 71. Driver Type B and Driver Type C (DDR3 Drive Strength 40 Ω)

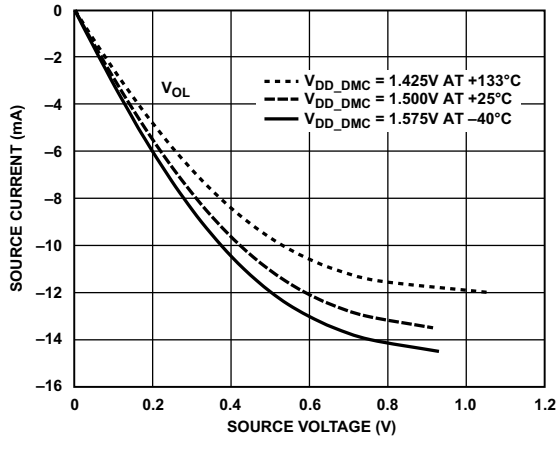


Figure 72. Driver Type B and Driver Type C (DDR3 Drive Strength 60 Ω)

CONFIGURATION OF THE 176-LEAD LQFP LEAD CONFIGURATION

Figure 90 shows the top view of the 176-lead LQFP lead configuration and Figure 91 shows the bottom view of the 176-lead LQFP lead configuration.

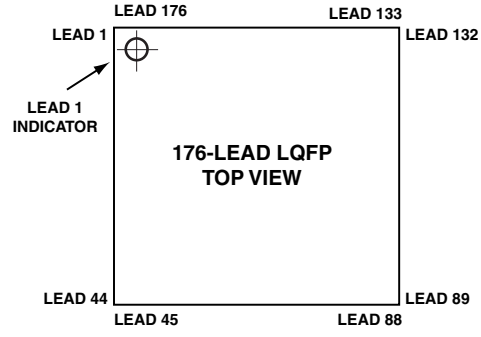


Figure 90. 176-Lead LQFP Lead Configuration (Top View)

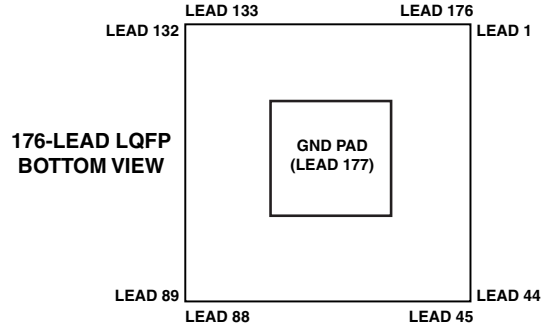


Figure 91. 176-Lead LQFP Lead Configuration (Bottom View)

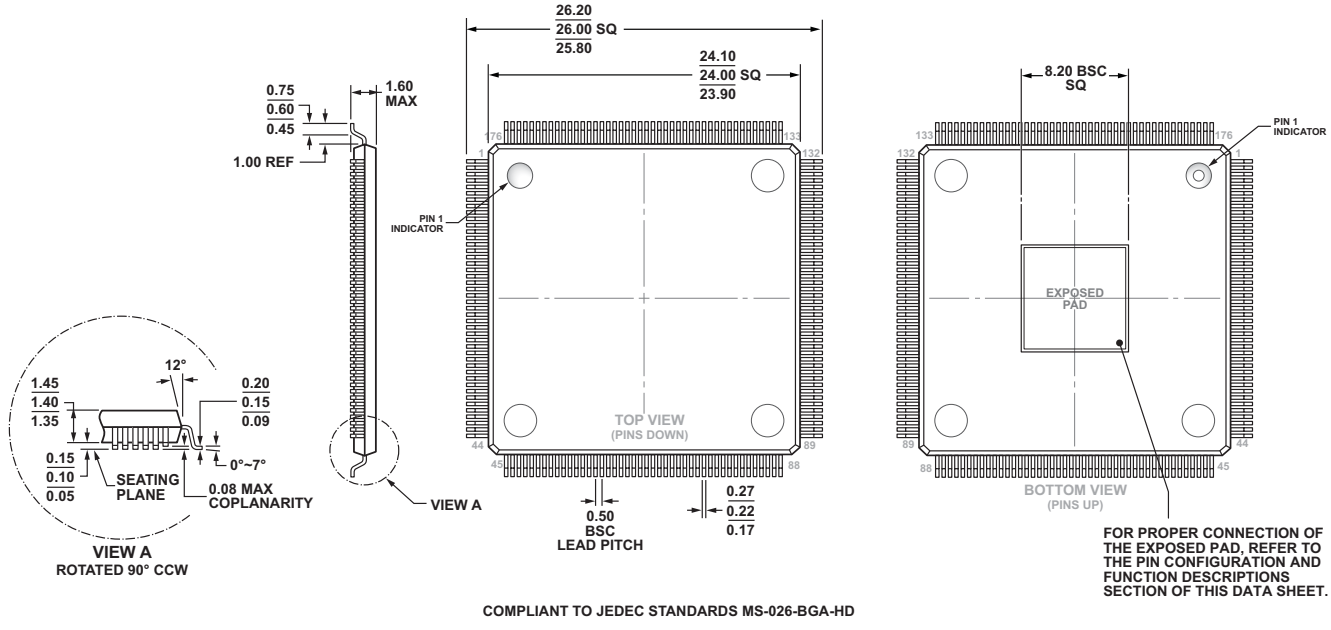


Figure 93. 176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-176-5)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 98 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 98. CSP_BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
BC-400-2	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter

AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 99 are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 99. Automotive Products

Model [1, 2, 3]	Processor Instruction Rate (Max)	ARM Instruction Rate (Max)[4]	Temperature Range[5]	ARM Cores[4]	SHARC+ Cores	External Memory Ports	Package Description	Package Option
AD21571WCSWZ4xx	450 MHz	N/A	–40°C to +105°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
AD21571WCSWZ5xx	500 MHz	N/A	–40°C to +105°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
AD21573WCBCZ4xx	450 MHz	N/A	–40°C to +105°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
AD21573WCBCZ5xx	500 MHz	N/A	–40°C to +105°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC570WCSWZ42xx	450 MHz	225 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSC570WCSWZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ3xx	300 MHz	300 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ5xx	500 MHz	500 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC572WCBCZ42xx	450 MHz	225 MHz	–40°C to +105°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC572WCBCZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ3xx	300 MHz	300 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ5xx	500 MHz	500 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2

[1] Z = RoHS Compliant Part.
[2] xx denotes the current die revision.
[3] For evaluation of all models, order the ADZS-SC573-EZLITE evaluation board.
[4] N/A means not applicable.
[5] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.

ORDERING GUIDE

Model[1, 2]	Processor Instruction Rate (Max)	ARM Instruction Rate (Max)[3]	Temperature Range[4]	ARM Cores[3]	SHARC+ Cores	External Memory Ports	Package Description	Package Option
ADSP-21571KSWZ-4	450 MHz	N/A	0°C to +70°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571BSWZ-4	450 MHz	N/A	–40°C to +85°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571CSWZ-4	450 MHz	N/A	–40°C to +105°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571KSWZ-5	500 MHz	N/A	0°C to +70°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571BSWZ-5	500 MHz	N/A	–40°C to +85°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21571CSWZ-5	500 MHz	N/A	–40°C to +100°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-21573KBCZ-4	450 MHz	N/A	0°C to +70°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573BBCZ-4	450 MHz	N/A	–40°C to +85°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573CBCZ-4	450 MHz	N/A	–40°C to +100°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573KBCZ-5	500 MHz	N/A	0°C to +70°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573BBCZ-5	500 MHz	N/A	–40°C to +85°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-21573CBCZ-5	500 MHz	N/A	–40°C to +95°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC570KSWZ-42	450 MHz	225 MHz	0°C to +70°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570BSWZ-42	450 MHz	225 MHz	–40°C to +85°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570CSWZ-42	450 MHz	225 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570KSWZ-4	450 MHz	450 MHz	0°C to +70°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570BSWZ-4	450 MHz	450 MHz	–40°C to +85°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC570CSWZ-4	450 MHz	450 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571KSWZ-3	300 MHz	300 MHz	0°C to +70°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571BSWZ-3	300 MHz	300 MHz	–40°C to +85°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571CSWZ-3	300 MHz	300 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571KSWZ-4	450 MHz	450 MHz	0°C to +70°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571BSWZ-4	450 MHz	450 MHz	–40°C to +85°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571CSWZ-4	450 MHz	450 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571KSWZ-5	500 MHz	500 MHz	0°C to +70°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571BSWZ-5	500 MHz	500 MHz	–40°C to +85°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC571CSWZ-5	500 MHz	500 MHz	–40°C to +100°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSP-SC572KBCZ-42	450 MHz	225 MHz	0°C to +70°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572BBCZ-42	450 MHz	225 MHz	–40°C to +85°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572CBCZ-42	450 MHz	225 MHz	–40°C to +100°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572KBCZ-4	450 MHz	450 MHz	0°C to +70°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572BBCZ-4	450 MHz	450 MHz	–40°C to +85°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC572CBCZ-4	450 MHz	450 MHz	–40°C to +100°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573KBCZ-3	300 MHz	300 MHz	0°C to +70°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573BBCZ-3	300 MHz	300 MHz	–40°C to +85°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573CBCZ-3	300 MHz	300 MHz	–40°C to +100°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573KBCZ-4	450 MHz	450 MHz	0°C to +70°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573BBCZ-4	450 MHz	450 MHz	–40°C to +85°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573CBCZ-4	450 MHz	450 MHz	–40°C to +100°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573KBCZ-5	500 MHz	500 MHz	0°C to +70°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573BBCZ-5	500 MHz	500 MHz	–40°C to +85°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSP-SC573CBCZ-5	500 MHz	500 MHz	–40°C to +95°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2

[1] Z =RoHS Compliant Part.

[2] For evaluation of all models, order the ADZS-SC573-EZLITE evaluation board.

[3] N/A means not applicable.

[4] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.