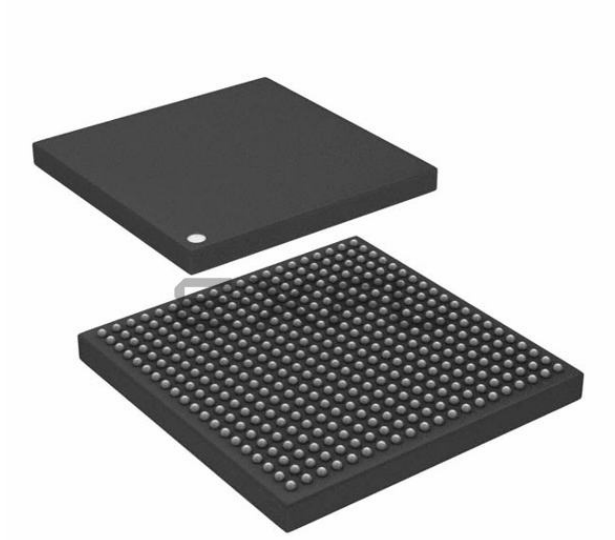

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Fixed/Floating Point |
| Interface | CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG |
| Clock Rate | 300MHz, 300MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 2MB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.10V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 400-LFBGA, CSPBGA |
| Supplier Device Package | 400-CSPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-sc573kbcz-3 |

### *Generic Interrupt Controller (GIC), PL390 (ADSP-SC57x Only)*

The generic interrupt controller (GIC) is a centralized resource for supporting and managing interrupts. The GIC splits into the distributor block (GICPORT0) and the central processing unit (CPU) interface block (GICPORT1).

#### Generic Interrupt Controller Port0 (GICPORT0)

The GICPORT0 distributor block performs interrupt prioritization and distribution to the GICPORT1 CPU interface blocks that connect to the processors in the system. It centralizes all interrupt sources, determines the priority of each interrupt, and forwards the interrupt with the highest priority to the interface, for priority masking and preemption handling.

#### Generic Interrupt Controller Port1 (GICPORT1)

The GICPORT1 CPU interface block performs priority masking and preemption handling for a connected processor in the system. GICPORT1 supports 8 software generated interrupts (SGIs) and 212 shared peripheral interrupts (SPIs).

### *L2 Cache Controller, PL310 (ADSP-SC57x Only)*

The Level 2 (L2) cache controller, PL310 (see Figure 2), works efficiently with the ARM Cortex-A5 processors that implement system fabric. The cache controller directly interfaces on the data and instruction interface. The internal pipelining of the cache controller is optimized to enable the processors to operate at the same clock frequency. The cache controller supports the following:

- Two read/write 64-bit slave ports, one connected to the ARM Cortex-A5 instruction and data interfaces, and one connecting the ARM Cortex-A5 and SHARC+ cores for data coherency.
- Two read/write 64-bit master ports for interfacing with the system fabric.

## SHARC PROCESSOR

Figure 3 shows the SHARC processor integrates a SHARC+ SIMD core, L1 memory crossbar, I/D cache controller, L1 memory blocks, and the master/slave ports. Figure 4 shows the SHARC+ SIMD core block diagram.

The SHARC processor supports a modified Harvard architecture in combination with a hierarchical memory structure. L1 memories typically operate at the full processor speed with little or no latency.

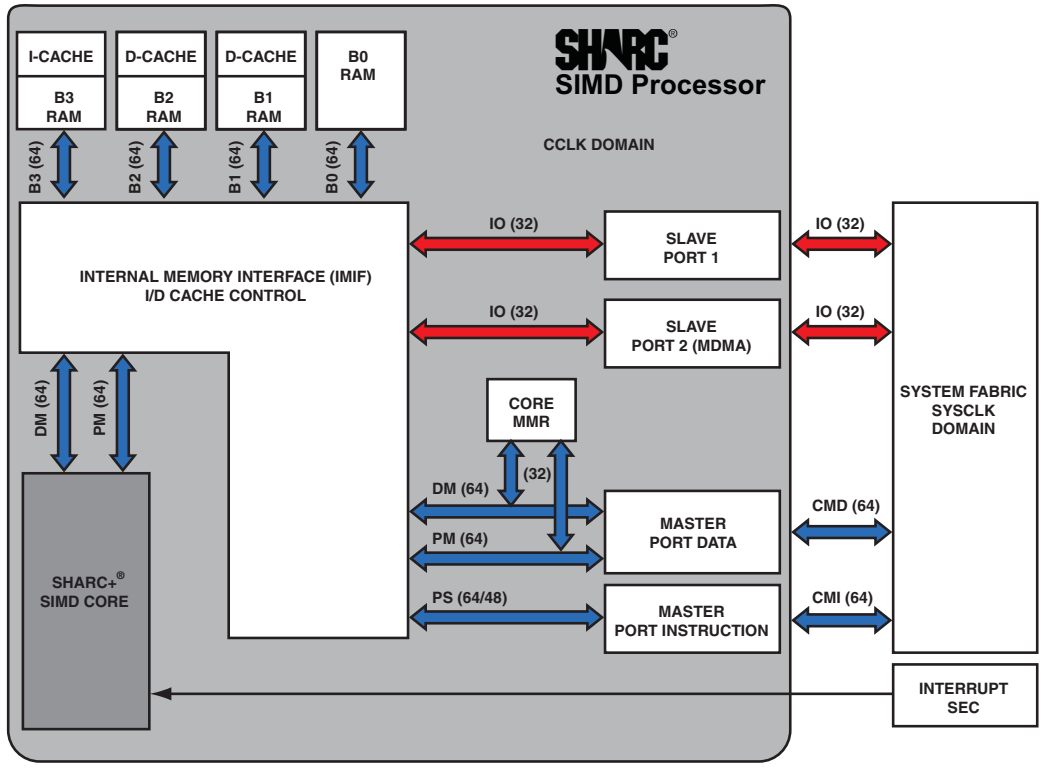



*Figure 3. SHARC Processor Block Diagram*

### Cyclic Redundant Code (CRC) Protected Memories

While parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the cyclic redundant code (CRC) engines can protect against systematic errors (pointer errors) and static content (instruction code) of L1, L2, and even Level 3 (L3) memories (DDR2, LPDDR). The processors feature two CRC engines that are embedded in the memory to memory DMA controllers.

CRC checksums can be calculated or compared automatically during memory transfers, or one or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

### Signal Watchdogs

The eight general-purpose (GP) timers feature modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range.

The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help detect undesired toggling or lack of toggling of system level signals.

### System Event Controller (SEC)

Besides system events, the system event controller (SEC) further supports fault management including fault action configuration as timeout, internal indication by system interrupt, or external indication through the $\overline{\text{SYS\_FAULT}}$ pin and system reset.

### Memory Error Controller (MEC)

The memory error controller (MEC) manages memory parity/ECC errors and warnings from the cores and peripherals and sends out interrupts and triggers.

## PROCESSOR PERIPHERALS

The following sections describe the peripherals of the ADSP-SC57x/ADSP-2157x processors.

### Dynamic Memory Controller (DMC)

The 16-bit dynamic memory controller (DMC) interfaces to

- LPDDR1 (JESD209A) maximum frequency 200 MHz, DDRCLK (64 Mb to 2 Gb)
- DDR2 (JESD79-2E) maximum frequency 400 MHz, DDRCLK (256 Mb to 4 Gb)
- DDR3 (JESD79-3E) maximum frequency 450 MHz, DDRCLK (512 Mb to 8 Gb)
- DDR3L (1.5 V compatible only) maximum frequency 450 MHz, DDRCLK (512 Mb to 8 Gb)

See Table 8 for the DMC memory map.

### Digital Audio Interface (DAI)

The processors support one mirrored digital audio interface (DAI) unit. The DAI can connect various peripherals to any of the DAI pins (DAI_PIN20–DAI_PIN01).

The application code makes these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to interconnect under software control. This functionality allows easy use of the DAI associated peripherals for a wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes the peripherals described in the following sections (SPORTs, ASRC, S/PDIF, and PCG). DAI Pin Buffers 20 and 19 can change the polarity of the input signals. Most signals of the peripherals belonging to different DAIs cannot be interconnected, with few exceptions.

The DAI_PINx pin buffers can also be used as GPIO pins. DAI input signals allow the triggering of interrupts on the rising edge, falling edge, or both.

See the Digital Audio Interface (DAI) chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for complete information on the use of the DAIs and SRUs.

### Serial Port (SPORT)

The processors feature four synchronous full serial ports (SPORTs). These ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. These devices include Analog Devices AD19xx and ADAU19xx family of audio codecs, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Two data lines, a clock, and frame sync make up the serial ports. The data lines can be programmed to either transmit or receive data and each data line has a dedicated DMA channel.

An individual full SPORT module consists of two independently configurable SPORT halves with identical functionality. Two bidirectional data lines—primary (0) and secondary (1)—are available per SPORT half and are configurable as either transmitters or receivers. Therefore, each SPORT half permits two unidirectional streams into or out of the same SPORT. This bidirectional functionality provides greater flexibility for serial communications. For full-duplex configuration, one half SPORT provides two transmit signals, while the other half SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in the following six modes:

- Standard DSP serial mode
- Multichannel time division multiplexing (TDM) mode
- $I^2S$ mode
- Packed $I^2S$ mode
- Left justified mode
- Right justified mode

### Asynchronous Sample Rate Converter (ASRC)

The asynchronous sample rate converter (ASRC) contains four ASRC blocks. It is the same core in the AD1896 192 kHz stereo asynchronous sample rate converter. The ASRC provides up to 140 dB signal-to-noise ratio (SNR). The ASRC block performs

synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The ASRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can clean up audio data from jittery clock sources such as the S/PDIF receiver.

### *S/PDIF-Compatible Digital Audio Receiver/Transmitter*

The Sony/Philips Digital Interface Format (S/PDIF) is a standard audio data transfer format that allows the transfer of digital audio signals from one device to another without converting them to an analog signal. There is one S/PDIF transmit/receive block on the processor. The digital audio interface carries three types of information: audio data, nonaudio data (compressed data), and timing information.

The S/PDIF interface supports one stereo channel or compressed audio streams. The S/PDIF transmitter and receiver are AES3 compliant and support the sample rate from 24 KHz to 192 KHz. The S/PDIF receiver supports professional jitter standards.

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, $I^2S$, or right justified with word widths of 16, 18, 20, or 24 bits. The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from various sources, such as the SPORTs, external pins, and the precision clock generators (PCGs), and are controlled by the SRU control registers.

### *Precision Clock Generators (PCG)*

The precision clock generators (PCG) consist of two units located in the DAI block. The PCG can generate a pair of signals (clock and frame sync) derived from a clock input signal (CLKIN, SCLK0, or DAI pin buffer). Both units are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

### *Enhanced Parallel Peripheral Interface (EPPI)*

The processors provide an enhanced parallel peripheral interface (EPPI) that supports data widths up to 16 bits for the BGA package and 12 bits for the LQFP package. The EPPI supports direct connection to thin film transistor (TFT) LCD panels, parallel ADCs and DACs, video encoders and decoders, image sensor modules, and other general-purpose peripherals.

The features supported in the EPPI module include the following:

- Programmable data length of 8 bits, 10 bits, 12 bits, 14 bits, and 16 bits per clock.
- Various framed, nonframed, and general-purpose operating modes. Frame syncs can be generated internally or can be supplied by an external device.
- ITU-656 status word error detection and correction for ITU-656 receive modes and ITU-656 preamble and status word decoding.
- Optional packing and unpacking of data to/from 32 bits from/to 8 bits and 16 bits. If packing/unpacking is enabled, configure endianness to change the order of packing/unpacking of bytes or words.
- RGB888 can be converted to RGB666 or RGB565 for transmit modes.
- Various deinterleaving/interleaving modes for receiving or transmitting 4:2:2 YCrCb data.
- Configurable LCD data enable output available on Frame Sync 3.

### *Universal Asynchronous Receiver/Transmitter (UART) Ports*

The processors provide three full-duplex universal asynchronous receiver/transmitter (UART) ports, fully compatible with PC standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits as well as no parity, even parity, or odd parity.

Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multidrop bus (MDB) systems. A frame is terminated by a configurable number of stop bits.

The UART ports support automatic hardware flow control through the clear to send (CTS) input and request to send (RTS) output with programmable assertion first in, first out (FIFO) levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable interframe space.

### *Serial Peripheral Interface (SPI) Ports*

The processors have three industry-standard SPI-compatible ports that allow the processors to communicate with multiple SPI-compatible devices.

The baseline SPI peripheral is a synchronous, 4-wire interface consisting of two data pins, one device select pin, and a gated clock pin. The two data pins allow full-duplex operation to other SPI-compatible devices. An extra two (optional) data pins are provided to support quad-SPI operation. Enhanced modes of operation, such as flow control, fast mode, and dual-I/O mode (DIOM), are also supported. DMA mode allows for transferring several words with minimal central processing unit (CPU) interaction.

With a range of configurable options, the SPI ports provide a glueless hardware interface with other SPI-compatible devices in master mode, slave mode, and multimaster environments. The SPI peripheral includes programmable baud rates, clock phase, and clock polarity. The peripheral can operate in a multimaster environment by interfacing with several other devices,

**Table 11. ADSP-SC57x/ADSP-2157x Detailed Signal Descriptions (Continued)**

| Signal Name | Direction | Description |
|---|---|---|
| $\overline{\text{DMC\_UDQS}}$ | InOut | **Data Strobe for Upper Byte (Complement).** Complement of DMC_UDQS. Not used in single-ended mode. |
| DMC_VREF | Input | **Voltage Reference.** Connects to half of the VDD_DMC voltage. Applies to the DMC0_VREF pin. |
| $\overline{\text{DMC\_WE}}$ | Output | **Write Enable.** Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the $\overline{\text{WE}}$ input of dynamic memory. |
| ETH_COL | Input | **MII Collision Detect.** Collision detect input signal valid only in MII. |
| ETH_CRS | Input | **MII Carrier Sense.** Asserted by the PHY when either the transmit or receive medium is not idle. Deasserted when both are idle. This signal is not used in RMII/RGMII modes. |
| ETH_MDC | Output | **Management Channel Clock.** Clocks the MDC input of the PHY for RMII/RGMII. |
| ETH_MDIO | InOut | **Management Channel Serial Data.** Bidirectional data bus for PHY control for RMII/RGMII. |
| ETH_PTPAUXIN[n] | Input | **PTP Auxiliary Trigger Input.** Assert this signal to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO. |
| ETH_PTPCLKIN[n] | Input | **PTP Clock Input.** Optional external PTP clock input. |
| ETH_PTPPPS[n] | Output | **PTP Pulse Per Second Output.** When the advanced time stamp feature enables, this signal is asserted based on the PPS mode selected. Otherwise, this signal is asserted every time the seconds counter is incremented. |
| ETH_RXCLK_REFCLK | InOut | **RXCLK (10/100/1000) or REFCLK (10/100).** |
| ETH_RXCTL_RXDV | InOut | **RXCTL (10/100/1000) or RXDV (10/100).** In RGMII mode, RX_CTL multiplexes receive data valid and receiver error. In RMII mode, RXDV is carrier sense and receive data valid (CRS_DV), multiplexed on alternating clock cycles. In MII mode, RXDV is receive data valid (RX_DV), asserted by the PHY when the data on ETH_RXD[n] is valid. |
| ETH_RXD[n] | Input | **Receive Data n.** Receive data bus. |
| ETH_RXERR | Input | **Receive Error.** |
| ETH_TXCLK | Input | **Reference Clock.** Externally supplied Ethernet clock |
| ETH_TXCTL_TXEN | InOut | **TXCTL (10/100/1000) or TXEN (10/100).** |
| ETH_TXD[n] | Output | **Transmit Data n.** Transmit data bus. |
| HADC_EOC_DOUT | Output | **End of Conversion/Serial Data Out.** Transitions high for one cycle of the HADC internal clock at the end of every conversion. Alternatively, HADC serial data out can be seen by setting the appropriate bit in HADC_CTL. |
| HADC_VIN[n] | Input | **Analog Input at Channel n.** Analog voltage inputs for digital conversion. |
| HADC_VREFN | Input | **Ground Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications. |
| HADC_VREFP | Input | **External Reference for ADC.** Connect to an external voltage reference that meets data sheet specifications. |
| JTG_TCK | Input | **JTAG Clock.** JTAG test access port clock. |
| JTG_TDI | Input | **JTAG Serial Data In.** JTAG test access port data input. |
| JTG_TDO | Output | **JTAG Serial Data Out.** JTAG test access port data output. |
| JTG_TMS | Input | **JTAG Mode Select.** JTAG test access port mode select. |
| $\overline{\text{JTG\_TRST}}$ | Input | **JTAG Reset.** JTAG test access port reset. |
| LP_ACK | InOut | **Acknowledge.** Provides handshaking. When the link port is configured as a receiver, ACK is an output. When the link port is configured as a transmitter, ACK is an input. |
| LP_CLK | InOut | **Clock.** When the link port is configured as a receiver, CLK is an input. When the link port is configured as a transmitter, CLK is an output. |
| LP_D[n] | InOut | **Data n.** Data bus. Input when receiving, output when transmitting. |
| MLB_CLK | InOut | **Single Ended Clock.** |
| MLB_CLKN | InOut | **Differential Clock (–).** |
| MLB_CLKOUT | InOut | **Single Ended Clock Out.** |
| MLB_CLKP | InOut | **Differential Clock (+).** |
| MLB_DAT | InOut | **Single Ended Data.** |

**Table 12. ADSP-SC57x/ADSP-2157x 400-Ball CSP_BGA Signal Descriptions (Continued)**

| Signal Name | Description | Port | Pin Name |
|---|---|---|---|
| SPI2_SEL2 | SPI2 Slave Select Output 2 | F | PF_10 |
| SPI2_SEL3 | SPI2 Slave Select Output 3 | C | PC_00 |
| SPI2_SEL4 | SPI2 Slave Select Output 4 | D | PD_08 |
| SPI2_SEL5 | SPI2 Slave Select Output 5 | A | PA_15 |
| SPI2_SEL6 | SPI2 Slave Select Output n | A | PA_10 |
| SPI2_SEL7 | SPI2 Slave Select Output n | B | PB_07 |
| SPI2_SS | SPI2 Slave Select Input | B | PB_15 |
| SYS_BMODE0 | Boot Mode Control n | Not Muxed | SYS_BMODE0 |
| SYS_BMODE1 | Boot Mode Control n | Not Muxed | SYS_BMODE1 |
| SYS_BMODE2 | Boot Mode Control n | Not Muxed | SYS_BMODE2 |
| SYS_CLKIN0 | Clock/Crystal Input | Not Muxed | SYS_CLKIN0 |
| SYS_CLKIN1 | Clock/Crystal Input | Not Muxed | SYS_CLKIN1 |
| SYS_CLKOUT | Processor Clock Output | Not Muxed | SYS_CLKOUT |
| SYS_FAULT | Active-High Fault Output | Not Muxed | SYS_FAULT |
| SYS_FAULT | Active-Low Fault Output | Not Muxed | SYS_FAULT |
| SYS_HWRST | Processor Hardware Reset Control | Not Muxed | SYS_HWRST |
| SYS_RESOUT | Reset Output | Not Muxed | SYS_RESOUT |
| SYS_XTAL0 | Crystal Output | Not Muxed | SYS_XTAL0 |
| SYS_XTAL1 | Crystal Output | Not Muxed | SYS_XTAL1 |
| TM0_ACI0 | TIMER0 Alternate Capture Input 0 | F | PF_09 |
| TM0_ACI1 | TIMER0 Alternate Capture Input 1 | F | PF_11 |
| TM0_ACI2 | TIMER0 Alternate Capture Input 2 | C | PC_12 |
| TM0_ACI3 | TIMER0 Alternate Capture Input 3 | C | PC_14 |
| TM0_ACI4 | TIMER0 Alternate Capture Input 4 | C | PC_13 |
| TM0_ACI5 | TIMER0 Alternate Capture Input 5 | Not Applicable | DAI0_PIN04[1] |
| TM0_ACI6 | TIMER0 Alternate Capture Input 6 | Not Applicable | DAI0_PIN19[1] |
| TM0_ACI7 | TIMER0 Alternate Capture Input 7 | Not Applicable | CNT0_TO |
| TM0_ACLK0 | TIMER0 Alternate Clock 0 | Not Applicable | SYS_CLKIN1 |
| TM0_ACLK1 | TIMER0 Alternate Clock 1 | F | PF_06 |
| TM0_ACLK2 | TIMER0 Alternate Clock 2 | C | PC_01 |
| TM0_ACLK3 | TIMER0 Alternate Clock 3 | D | PD_09 |
| TM0_ACLK4 | TIMER0 Alternate Clock 4 | E | PE_02 |
| TM0_ACLK5 | TIMER0 Alternate Clock 5 | Not Applicable | DAI0_PIN03[1] |
| TM0_ACLK6 | TIMER0 Alternate Clock 6 | Not Applicable | DAI0_PIN20[1] |
| TM0_ACLK7 | TIMER0 Alternate Clock 7 | Not Applicable | SYS_CLKIN0 |
| TM0_CLK | TIMER0 Clock | C | PC_03 |
| TM0_TMR0 | TIMER0 Timer 0 | E | PE_12 |
| TM0_TMR1 | TIMER0 Timer 1 | F | PF_05 |
| TM0_TMR2 | TIMER0 Timer 2 | F | PF_07 |
| TM0_TMR3 | TIMER0 Timer 3 | B | PB_01 |
| TM0_TMR4 | TIMER0 Timer 4 | B | PB_03 |
| TM0_TMR5 | TIMER0 Timer 5 | C | PC_15 |
| TM0_TMR6 | TIMER0 Timer 6 | E | PE_14 |
| TM0_TMR7 | TIMER0 Timer 7 | D | PD_07 |
| TRACE0_CLK | TRACE0 Trace Clock | F | PF_06 |
| TRACE0_D00 | TRACE0 Trace Data 0 | F | PF_00 |
| TRACE0_D01 | TRACE0 Trace Data 1 | F | PF_01 |
| TRACE0_D02 | TRACE0 Trace Data 2 | F | PF_02 |

**Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)**

| Signal Name | Type | Driver Type | Internal Termination | Reset Drive | Power Domain | Description and Notes |
|---|---|---|---|---|---|---|
| $\overline{\text{DMC0\_CAS}}$ | Output | B | none | L | VDD_DMC | Desc: DMC0 Column Address Strobe<br>Notes: No notes |
| DMC0_CK | Output | C | none | L | VDD_DMC | Desc: DMC0 Clock<br>Notes: No notes |
| DMC0_CKE | Output | B | none | L | VDD_DMC | Desc: DMC0 Clock enable<br>Notes: No notes |
| $\overline{\text{DMC0\_CK}}$ | Output | C | none | L | VDD_DMC | Desc: DMC0 Clock (complement)<br>Notes: No notes |
| $\overline{\text{DMC0\_CS0}}$ | Output | B | none | L | VDD_DMC | Desc: DMC0 Chip Select 0<br>Notes: No notes |
| DMC0_DQ00 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 0<br>Notes: No notes |
| DMC0_DQ01 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 1<br>Notes: No notes |
| DMC0_DQ02 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 2<br>Notes: No notes |
| DMC0_DQ03 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 3<br>Notes: No notes |
| DMC0_DQ04 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 4<br>Notes: No notes |
| DMC0_DQ05 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 5<br>Notes: No notes |
| DMC0_DQ06 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 6<br>Notes: No notes |
| DMC0_DQ07 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 7<br>Notes: No notes |
| DMC0_DQ08 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 8<br>Notes: No notes |
| DMC0_DQ09 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 9<br>Notes: No notes |
| DMC0_DQ10 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 10<br>Notes: No notes |
| DMC0_DQ11 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 11<br>Notes: No notes |
| DMC0_DQ12 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 12<br>Notes: No notes |
| DMC0_DQ13 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 13<br>Notes: No notes |
| DMC0_DQ14 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 14<br>Notes: No notes |
| DMC0_DQ15 | InOut | B | none | none | VDD_DMC | Desc: DMC0 Data 15<br>Notes: No notes |
| DMC0_LDM | Output | B | none | L | VDD_DMC | Desc: DMC0 Data Mask for Lower Byte<br>Notes: No notes |
| DMC0_LDQS | InOut | C | none | none | VDD_DMC | Desc: DMC0 Data Strobe for Lower Byte<br>Notes: External weak pull-down required in LPDDR mode |

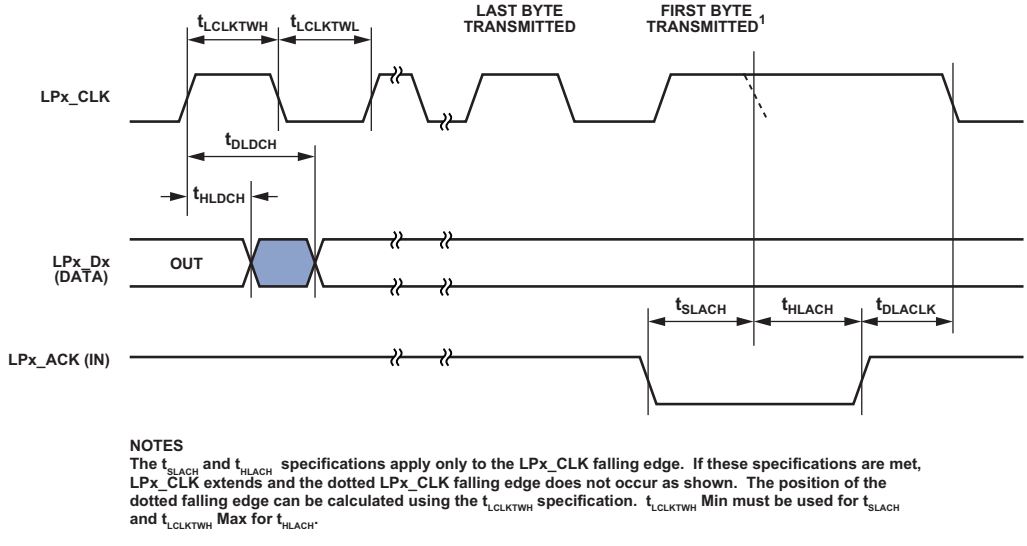
| Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_IDLE}$ | $V_{DD\_INT}$ Current in Idle | $f_{CCLK}$ = 500 MHz<br>$ASF_{SHARC1}$ = 0.32<br>$ASF_{SHARC2}$ = 0.32<br>$ASF_{A5}$ = 0.25<br>$f_{SYSCLK}$ = 250 MHz<br>$f_{SCLK0/1}$ = 125 MHz<br>(Other clocks are disabled)<br>No Peripheral or DMA activity<br>$T_J$ = 25°C<br>$V_{DD\_INT}$ = 1.15 V | | 477 | | mA |
| $I_{DD\_TYP}$ | $V_{DD\_INT}$ Current | $f_{CCLK}$ = 450 MHz<br>$ASF_{SHARC1}$ = 1.0<br>$ASF_{SHARC2}$ = 1.0<br>$ASF_{A5}$ = 0.67<br>$f_{SYSCLK}$ = 225 MHz<br>$f_{SCLK0/1}$ = 112.5 MHz<br>(Other clocks are disabled)<br>DMA data rate = 600 MB/s<br>$T_J$ = 25°C<br>$V_{DD\_INT}$ = 1.1 V | | 890 | | mA |
| $I_{DD\_TYP}$ | $V_{DD\_INT}$ Current | $f_{CCLK}$ = 500 MHz<br>$ASF_{SHARC1}$ = 1.0<br>$ASF_{SHARC2}$ = 1.0<br>$ASF_{A5}$ = 0.67<br>$f_{SYSCLK}$ = 250 MHz<br>$f_{SCLK0/1}$ = 125 MHz<br>(Other clocks are disabled)<br>DMA data rate = 600 MB/s<br>$T_J$ = 25°C<br>$V_{DD\_INT}$ = 1.15 V | | 1031 | | mA |
| $I_{DD\_INT}$[11] | $V_{DD\_INT}$ Current | $f_{CCLK}$ > 0 MHz<br>$f_{SCLK0/1} \geq 0$ MHz | | | See $I_{DD\_INT\_TOT}$ equation in the Total Internal Power Dissipation section. | mA |

[1] Applies to all output and bidirectional pins except TWI, DMC, USB, and MLB.
[2] See the Output Drive Currents section for typical drive current capabilities.
[3] Applies to all DMC output and bidirectional signals in DDR2 mode.
[4] Applies to all DMC output and bidirectional signals in DDR3 mode.
[5] Applies to all DMC output and bidirectional signals in LPDDR mode.
[6] Applies to input pins: SYS_BMODE0-2, SYS_CLKIN0, SYS_CLKIN1, $\overline{\text{SYS\_HWRST}}$, JTG_TDI, JTG_TMS, and USB0_CLKIN.
[7] Applies to input pins with internal pull-ups: JTG_TDI, JTG_TMS, and JTG_TCK.
[8] Applies to signals: JTAG_TRST, USB0_VBUS.
[9] Applies to signals: PA0-15, PB0-15, PC0-15, PD0-15, PE0-15, PF0-11, DAI0_PINx, DMC0_DQx, DMC0_LDQS, DMC0_UDQS, $\overline{\text{DMC0\_LDQS}}$, $\overline{\text{DMC0\_UDQS}}$, SYS_FAULT, $\overline{\text{SYS\_FAULT}}$, JTG_TDO, USB0_ID, USB0_DM, USB0_DP, and USB0_VBC.
[10] Applies to all signal pins.
[11] See "Estimating Power for ADSP-SC57x/2157x SHARC+ Processors" (EE-397) for further information.

**Table 55. LPs—Transmit[1]**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SLACH}$ | LPx_ACK Setup Before LPx_CLK Low | $2 \times t_{SCLK0} + 13.5$ | | ns |
| $t_{HLACH}$ | LPx_ACK Hold After LPx_CLK Low | –5.5 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DLDCH}$ | Data Delay After LPx_CLK High | | 2.23 | ns |
| $t_{HLDCH}$ | Data Hold After LPx_CLK High | –2.3 | | ns |
| $t_{LCLKTWL}$[2] | LPx_CLK Width Low | $0.4 \times t_{LCLKTPROG}$ | $0.6 \times t_{LCLKTPROG}$ | ns |
| $t_{LCLKTWH}$[2] | LPx_CLK Width High | $0.4 \times t_{LCLKTPROG}$ | $0.6 \times t_{LCLKTPROG}$ | ns |
| $t_{LCLKTW}$[2] | LPx_CLK Period | $N \times t_{LCLKTPROG} - 0.6$ | | ns |
| $t_{DLACLK}$ | LPx_CLK Low Delay After LPx_ACK High | $t_{SCLK0} + 4$ | $2 \times t_{SCLK0} + 1 \times t_{LPCLK} + 10$ | ns |

[1] Specifications apply to LP0 and LP1.
[2] See Table 27 for details on the minimum period that can be programmed for $t_{LCLKTPROG}$.




NOTES
The $t_{SLACH}$ and $t_{HLACH}$ specifications apply only to the LPx_CLK falling edge. If these specifications are met, LPx_CLK extends and the dotted LPx_CLK falling edge does not occur as shown. The position of the dotted falling edge can be calculated using the $t_{LCLKTWH}$ specification. $t_{LCLKTWH}$ Min must be used for $t_{SLACH}$ and $t_{LCLKTWH}$ Max for $t_{HLACH}$.

*Figure 29. LPs—Transmit*

The SPTx_TDV output signal becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPTx_TDV is asserted for communication with external devices.

**Table 59. SPORTs—Transmit Data Valid (TDV)[1]**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{DRDVEN}$ | Data Valid Enable Delay from Drive Edge of External Clock[2] | 2 | | ns |
| $t_{DFDVEN}$ | Data Valid Disable Delay from Drive Edge of External Clock[2] | | 14 | ns |
| $t_{DRDVIN}$ | Data Valid Enable Delay from Drive Edge of Internal Clock[2] | –2.5 | | ns |
| $t_{DFDVIN}$ | Data Valid Disable Delay from Drive Edge of Internal Clock[2] | | 3.5 | ns |

[1] Specifications apply to all four SPORTs.
[2] Referenced to drive edge.

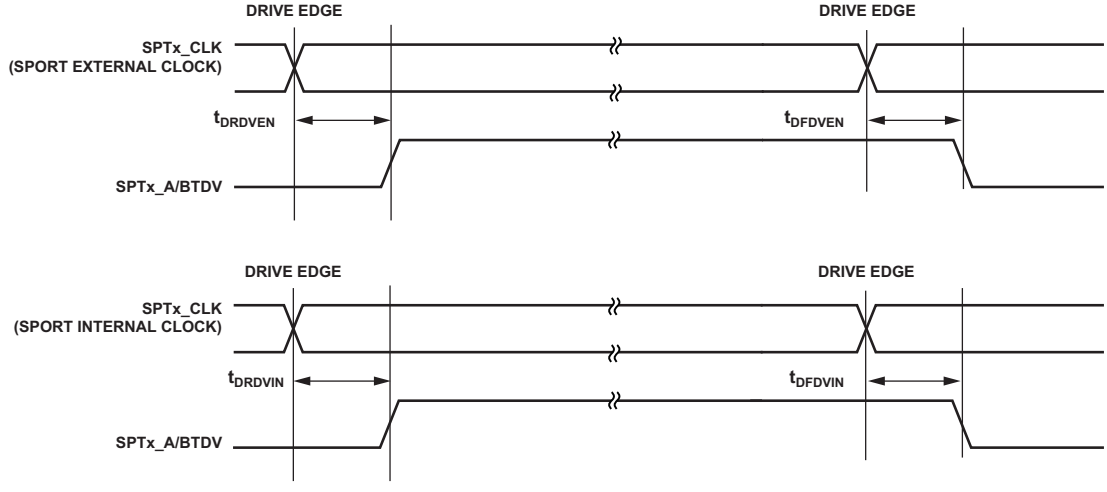



*Figure 32. SPORTs—Transmit Data Valid Internal and External Clock*

**Table 66. SPI2 Port—Slave Timing**[1]

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SPICHS}$ | SPIx_CLK High Period[2] | $0.5 \times t_{SPICLKEXT} - 1.5$ | | ns |
| $t_{SPICLS}$ | SPIx_CLK Low Period[2] | $0.5 \times t_{SPICLKEXT} - 1.5$ | | ns |
| $t_{SPICLK}$ | SPIx_CLK Period[2] | $t_{SPICLKEXT} - 1.5$ | | ns |
| $t_{HDS}$ | Last SPIx_CLK Edge to $\overline{SPIx\_SS}$ Not Asserted | 5 | | ns |
| $t_{SPITDS}$ | Sequential Transfer Delay | $t_{SPICLKEXT} - 1.5$ | | ns |
| $t_{SDSCI}$ | $\overline{SPIx\_SS}$ Assertion to First SPIx_CLK Edge | 10.5 | | ns |
| $t_{SSPID}$ | Data Input Valid to SPIx_CLK Edge (Data Input Setup) | 2 | | ns |
| $t_{HSPID}$ | SPIx_CLK Sampling Edge to Data Input Invalid | 1.6 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DSOE}$ | $\overline{SPIx\_SS}$ Assertion to Data Out Active | 0 | 14 | ns |
| $t_{DSDHI}$ | $\overline{SPIx\_SS}$ Deassertion to Data High Impedance | 0 | 11.5 | ns |
| $t_{DDSPID}$ | SPIx_CLK Edge to Data Out Valid (Data Out Delay) | | 14 | ns |
| $t_{HDSPID}$ | SPIx_CLK Edge to Data Out Invalid (Data Out Hold) | 1.5 | | ns |

[1] All specifications apply to SPI2 only.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx_CLK. For the external SPIx_CLK ideal maximum frequency, see the $f_{SPICLKTEXT}$ specification in Table 27.

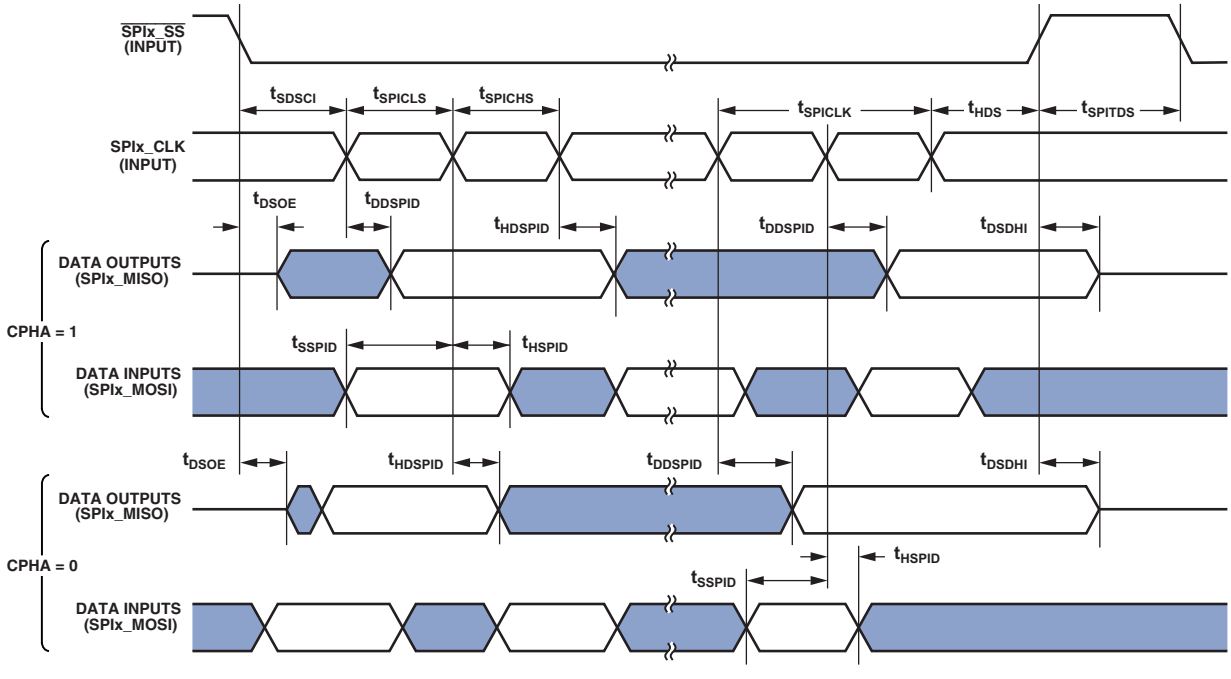



*Figure 37. SPI Port—Slave Timing*

### *SPI Port—SPIx_RDY Master Timing*

SPIx_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx_CTL register, while LEADX, LAGX, and STOP are configuration bits in the SPIx_DLY register.

**Table 70. SPI Port—SPIx_RDY Master Timing[1]**

| Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| *Timing Requirement* | | | | | |
| $t_{SRDYSCKM}$ | Setup Time for SPIx_RDY Deassertion Before Last Valid Data SPIx_CLK Edge | | $(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$ | | ns |
| *Switching Characteristic* | | | | | |
| $t_{DRDYSCKM}$[3] | Assertion of SPIx_RDY to First SPIx_CLK Edge of Next Transfer | BAUD = 0, CPHA = 0 | $4.5 \times t_{SCLK1}$ | $5.5 \times t_{SCLK1} + 10$ | ns |
| | | BAUD = 0, CPHA = 1 | $4 \times t_{SCLK1}$ | $5 \times t_{SCLK1} + 10$ | ns |
| | | BAUD > 0, CPHA = 0 | $(1 + 1.5 \times BAUD^{2}) \times t_{SCLK1}$ | $(2 + 2.5 \times BAUD^{2}) \times t_{SCLK1} + 10$ | ns |
| | | BAUD > 0, CPHA = 1 | $(1 + 1 \times BAUD^{2}) \times t_{SCLK1}$ | $(2 + 2 \times BAUD^{2}) \times t_{SCLK1} + 10$ | ns |

[1] All specifications apply to all three SPIs.
[2] BAUD value is set using the SPIx_CLK.BAUD bits. BAUD value = SPIx_CLK.BAUD bits + 1.
[3] Specification assumes the LEADX, LAGX, and STOP bits in the SPI_DLY register are zero.

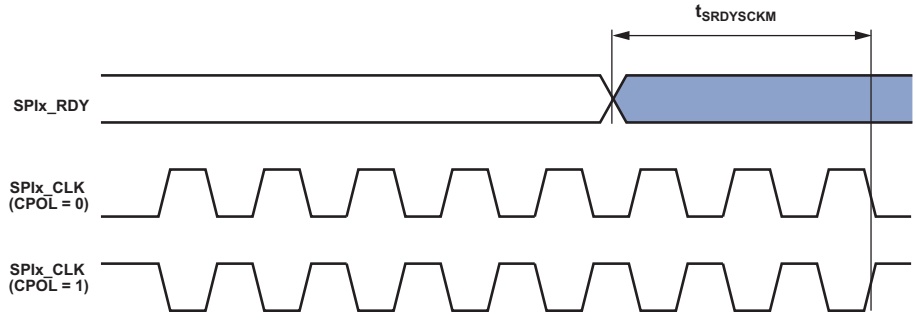



*Figure 41. SPIx_RDY Setup Before SPIx_CLK*

### *ADC Controller Module (ACM) Timing*

Table 77 and Figure 48 describe ACM operations.

When internally generated, the programmed ACM clock ($f_{ACLKPROG}$) frequency in megahertz is set by the following equation where CKDIV is a field in the ACM_TC0 register and ranges from 1 to 255:

$$f_{ACLKPROG} = \frac{f_{SCLK1}}{CKDIV + 1}$$

$$t_{ACLKPROG} = \frac{1}{f_{ACLKPROG}}$$

Setup cycles (SC) in Table 77 is also a field in the ACM_TC0 register and ranges from 0 to 4095. Hold Cycles (HC) is a field in the ACM_TC1 register that ranges from 0 to 15.

**Table 77. ACM Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SDR}$ | SPORT DRxPRI/DRxSEC Setup Before ACMx_CLK | 3.4 | | ns |
| $t_{HDR}$ | SPORT DRxPRI/DRxSEC Hold After ACMx_CLK | 1.5 | | ns |
| *Switching Characteristics* | | | | |
| $t_{SCTLCS}$ | ACM Controls (ACMx_A[4:0]) Setup Before Assertion of $\overline{CS}$ | (SC + 1) × $t_{SCLK1}$ – 4.88 | | ns |
| $t_{HCTLCS}$ | ACM Control (ACMx_A[4:0]) Hold After Deassertion of $\overline{CS}$ | HC × $t_{ACLKPROG}$ – 1 | | ns |
| $t_{ACLKW}$ | ACM Clock Pulse Width[1] | (0.5 × $t_{ACLKPROG}$) – 1.6 | | ns |
| $t_{ACLK}$ | ACM Clock Period[1] | $t_{ACLKPROG}$ – 1.5 | | ns |
| $t_{HCSACLK}$ | $\overline{CS}$ Hold to ACMx_CLK Edge | –2.5 | | ns |
| $t_{SCSACLK}$ | $\overline{CS}$ Setup to ACMx_CLK Edge | $t_{ACLKPROG}$ – 3.5 | | ns |

[1] See Table 27 for details on the minimum period that can be programmed for $t_{ACLKPROG}$.

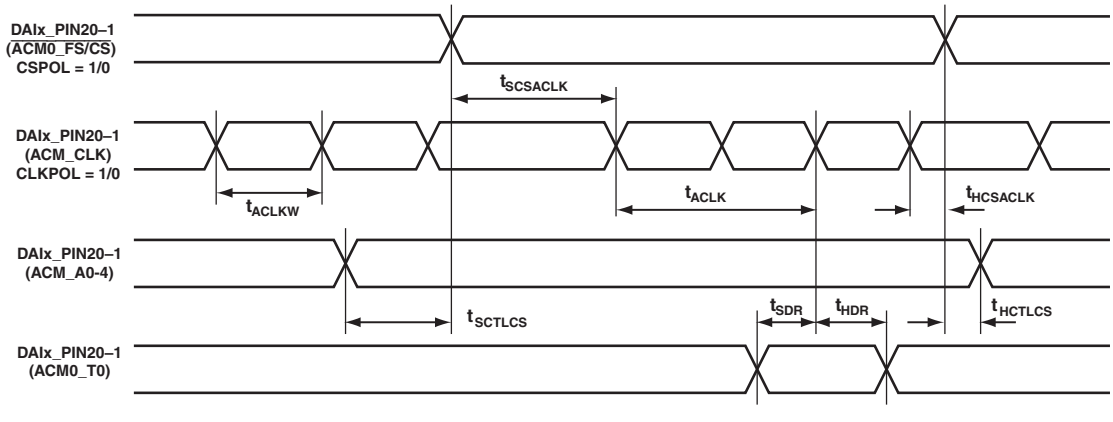



*Figure 48. ACM Timing*

### *10/100 EMAC Timing*

Table 79 through Table 83 and Figure 49 through Figure 53 describe the MII and RMII EMAC operations.

**Table 79. 10/100 EMAC Timing: MII Receive Signal**

| Parameter[1] | | $V_{DDEXT}$ 3.3 V Nominal | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| *Timing Requirements* | | | | |
| $t_{ERXCLKF}$ | ETH0_RXCLK_REFCLK Frequency ($f_{SCLK}$ = SCLK Frequency) | None | 25 + 1% | MHz |
| $t_{ERXCLKW}$ | ETH0_RXCLK_REFCLK Width ($t_{ERxCLK}$ = ETH0_RXCLK_REFCLK Period) | $t_{ERxCLK}$ × 35% | $t_{ERxCLK}$ × 65% | ns |
| $t_{ERXCLKIS}$ | Rx Input Valid to ETH0_RXCLK_REFCLK Rising Edge (Data In Setup) | 1.75 | | ns |
| $t_{ERXCLKIH}$ | ETH0_RXCLK_REFCLK Rising Edge to Rx Input Invalid (Data In Hold) | 1.5 | | ns |

[1] MII inputs synchronous to ETH0_RXCLK_REFCLK are ETH0_RXD3-0, ETH0_RXCTL_RXDV, and ETH0_RXERR.

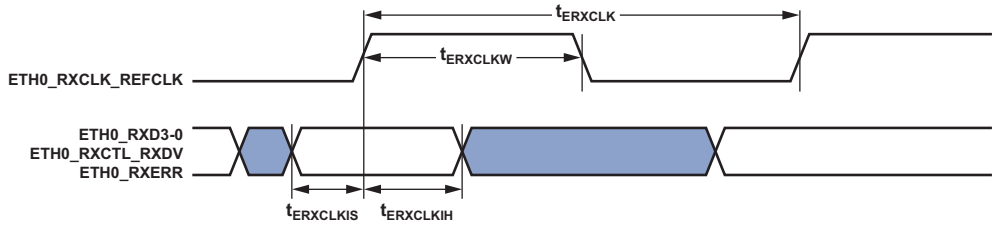



*Figure 49. 10/100 EMAC Timing: MII Receive Signal*

**Table 80. 10/100 EMAC Timing: MII Transmit Signal**

| Parameter[1] | | $V_{DDEXT}$ 3.3 V Nominal | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| *Timing Requirements* | | | | |
| $t_{ETXCLKF}$ | ETH0_TXCLK Frequency ($f_{SCLK}$ = SCLK Frequency) | None | 25 + 1% | MHz |
| $t_{ETXCLKW}$ | ETH0_TXCLK Width ($t_{ETxCLK}$ = ETH0_TXCLK Period) | $t_{ETxCLK}$ × 35% | $t_{ETxCLK}$ × 65% | ns |
| *Switching Characteristics* | | | | |
| $t_{ETXCLKOV}$ | ETH0_TXCLK Rising Edge to Tx Output Valid (Data Out Valid) | | 11.4 | ns |
| $t_{ETXCLKOH}$ | ETH0_TXCLK Rising Edge to Tx Output Invalid (Data Out Hold) | 2 | | ns |

[1] MII outputs synchronous to ETH0_TXCLK are ETH0_TXD3-0.

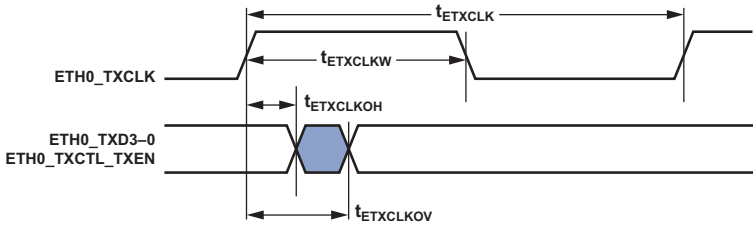



*Figure 50. 10/100 EMAC Timing: MII Transmit Signal*

### *Sony/Philips Digital Interface (S/PDIF) Transmitter*

Serial data input to the S/PDIF transmitter can be formatted as left justified, I$^2$S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

#### S/PDIF Transmitter Serial Input Waveforms

Figure 55 and Table 85 show the right justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right justified to the next frame sync transition.

**Table 85. S/PDIF Transmitter Right Justified Mode**

| Parameter | | Conditions | Nominal | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{RJD}$ | Frame Sync to MSB Delay in Right Justified Mode | 16-bit word mode | 16 | SCLK |
| | | 18-bit word mode | 14 | SCLK |
| | | 20-bit word mode | 12 | SCLK |
| | | 24-bit word mode | 8 | SCLK |

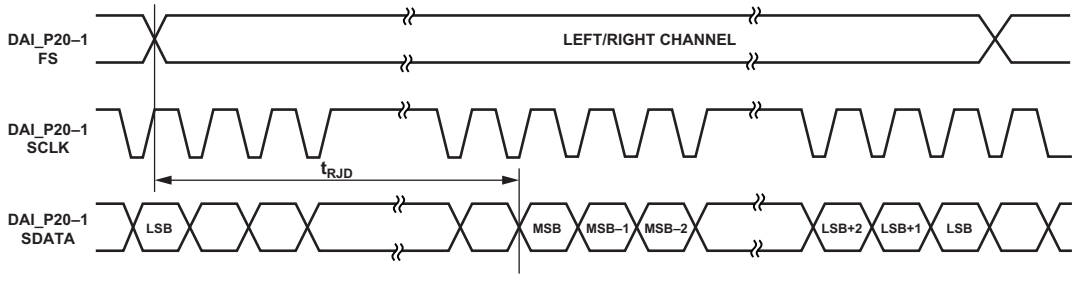



*Figure 55. Right Justified Mode*

Figure 56 and Table 86 show the default I²S justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left justified to the frame sync transition but with a delay.

**Table 86. S/PDIF Transmitter I²S Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{I2SD}$ | Frame Sync to MSB Delay in I²S Mode | 1 | SCLK |

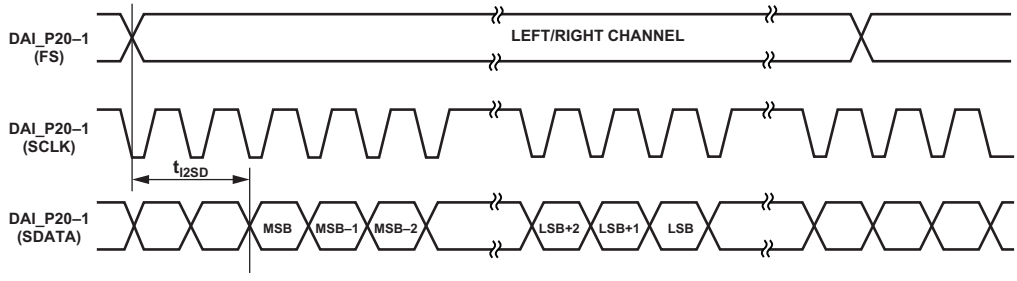



*Figure 56. I²S Justified Mode*

Figure 57 and Table 87 show the left justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left justified to the frame sync transition with no delay.

**Table 87. S/PDIF Transmitter Left Justified Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{LJD}$ | Frame Sync to MSB Delay in Left Justified Mode | 0 | SCLK |

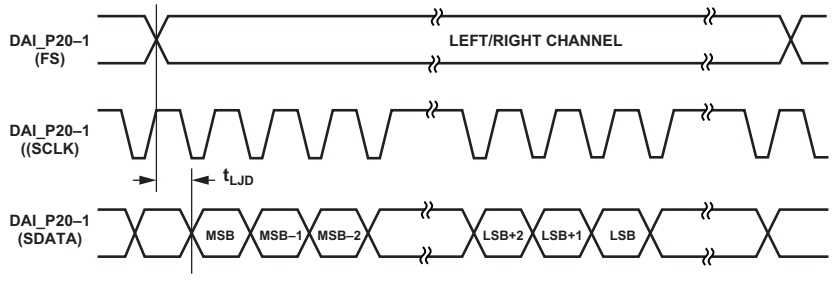



*Figure 57. Left Justified Mode*

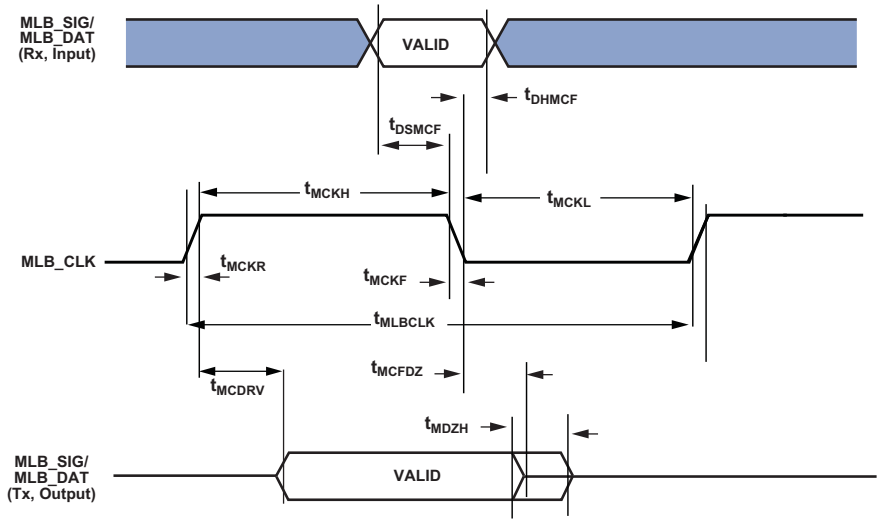



*Figure 60. MLB Timing (3-Pin Interface)*

The ac timing specifications of the 6-pin MLB interface is detailed in Table 92. Refer to the *Media Local Bus Specification version 4.2* for more details.

**Table 92. 6-Pin MLB Interface Specifications**

| Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{MT}$ | Differential Transition Time at the Input Pin (See Figure 61) | 20% to 80% $V_{IN}+/V_{IN}-$<br>80% to 20% $V_{IN}+/V_{IN}-$ | | | 1 | ns |
| $f_{MCKE}$ | MLBCP/N External Clock Operating Frequency (See Figure 62)[1] | 2048 × FS at 44.0 kHz | 90.112 | | | MHz |
| | | 2048 × FS at 50.0 kHz | | | 102.4 | MHz |
| $f_{MCKR}$ | Recovered Clock Operating Frequency (Internal, Not Observable at Pins, Only for Timing References) (See Figure 62) | 2048 × FS at 44.0 kHz | 90.112 | | | MHz |
| | | 2048 × FS at 50.0 kHz | | | 102.4 | MHz |
| $t_{DELAY}$ | Transmitter MLBSP/N (MLBDP/N) Output Valid From Transition of MLBCP/N (Low to High) (See Figure 63) | $f_{MCKR}$ = 2048 × FS | 0.6 | | 5 | ns |
| $t_{PHZ}$ | Disable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 64) | $f_{MCKR}$ = 2048 × FS | 0.6 | | 7 | ns |
| $t_{PLZ}$ | Enable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 64) | $f_{MCKR}$ = 2048 × FS | 0.6 | | 11.2 | ns |
| $t_{SU}$ | MLBSP/N (MLBDP/N) Valid to Transition of MLBCP/N (Low to High) (See Figure 63) | $f_{MCKR}$ = 2048 × FS | 1 | | | ns |
| $t_{HD}$ | MLBSP/N (MLBDP/N) Hold From Transition of MLBCP/N (Low to High) (See Figure 63)[2] | | 0.6 | | | ns |

[1] $f_{MCKE}$ (maximum) and $f_{MCKR}$ (maximum) include maximum cycle to cycle system jitter ($t_{JITTER}$) of 600 ps for a bit error rate of 10E-9.
[2] Receivers must latch MLBSP/N (MLBDP/N) data within $t_{HD}$ (minimum) of the rising edge of MLBCP/N.

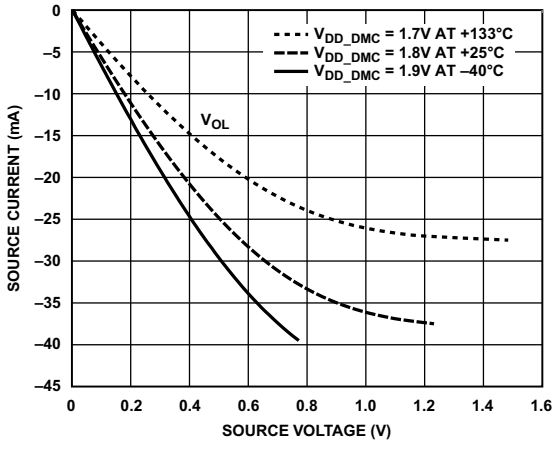



*Figure 79. Driver Type B and Device Driver C (LPDDR)*

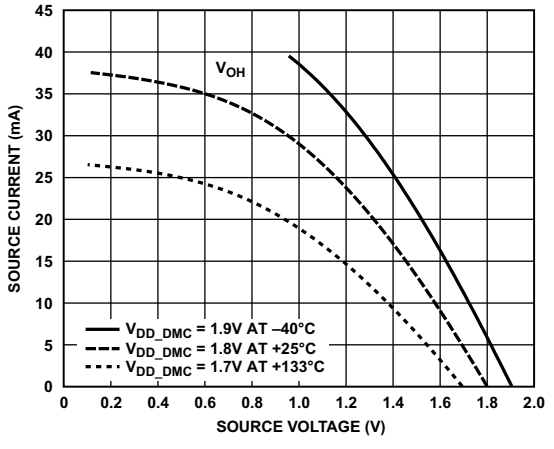



*Figure 80. Driver Type B and Device Driver C (LPDDR)*

## TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 81 shows the measurement point for ac measurements (except output enable/disable). The measurement point, $V_{MEAS}$, is $V_{DD\_EXT}/2$ for $V_{DD\_EXT}$ (nominal) = 3.3 V.

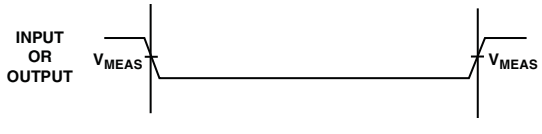



*Figure 81. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)*

### Output Enable Time Measurement

Output pins are considered enabled when they make a transition from a high impedance state to the point when they start driving.

The output enable time, $t_{ENA,}$ is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving, as shown on the right side of Figure 82. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

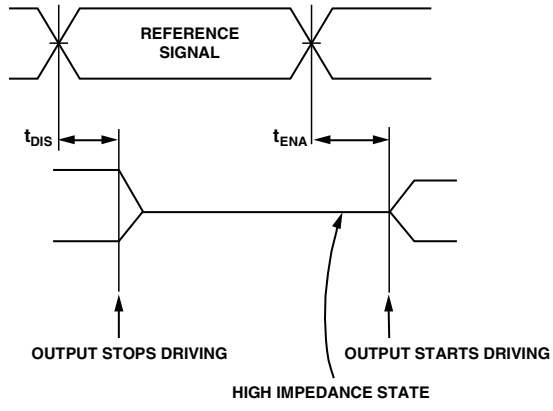



*Figure 82. Output Enable/Disable*

### Output Disable Time Measurement

Output pins are considered disabled when they stop driving, enter a high impedance state, and start to decay from the output high or low voltage. The output disable time, $t_{DIS}$, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving, as shown on the left side of Figure 82).

### Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 83). $V_{LOAD}$ is equal to $V_{DD\_EXT}/2$. Figure 84 through Figure 88 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in Figure 84 through Figure 88 cannot be linear outside the ranges shown.

# ADSP-SC57x/ADSP-2157x 400-BALL BGA BALL ASSIGNMENTS

The ADSP-SC57x/ADSP-2157x 400-Ball BGA Ball Assignments (Numerical by Ball Number) table lists the 400-ball BGA package by ball number.

The ADSP-SC57x/ADSP-2157x 400-Ball BGA Ball Assignments (Alphabetical by Pin Name) table lists the 400-ball BGA package by pin name.

## ADSP-SC57x/ADSP-2157x 400-BALL BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

| Ball No. | Pin Name | Ball No. | Pin Name | Ball No. | Pin Name | Ball No. | Pin Name |
|---|---|---|---|---|---|---|---|
| A01 | GND | C02 | PC_13 | E03 | PE_03 | G04 | VDD_EXT |
| A02 | PA_10 | C03 | GND | E04 | PE_02 | G05 | VDD_INT |
| A03 | PA_09 | C04 | PA_12 | E05 | GND | G06 | GND |
| A04 | PA_11 | C05 | PA_14 | E06 | PB_00 | G07 | GND |
| A05 | PE_07 | C06 | PB_03 | E07 | VDD_EXT | G08 | GND |
| A06 | MLB0_CLKN | C07 | PB_02 | E08 | VDD_EXT | G09 | GND |
| A07 | MLB0_CLKP | C08 | PE_10 | E09 | VDD_EXT | G10 | GND |
| A08 | MLB0_SIGN | C09 | PB_06 | E10 | VDD_EXT | G11 | GND |
| A09 | GND | C10 | PB_05 | E11 | VDD_EXT | G12 | GND |
| A10 | SYS_XTAL0 | C11 | $\overline{\text{SYS\_HWRST}}$ | E12 | VDD_EXT | G13 | GND |
| A11 | SYS_CLKIN0 | C12 | USB0_ID | E13 | VDD_USB | G14 | GND |
| A12 | GND | C13 | USB0_CLKIN | E14 | JTG_TCK | G15 | GND |
| A13 | SYS_XTAL1 | C14 | PB_12 | E15 | PE_15 | G16 | VDD_INT |
| A14 | SYS_CLKIN1 | C15 | PB_13 | E16 | GND | G17 | PB_15 |
| A15 | GND | C16 | JTG_TDI | E17 | VDD_EXT | G18 | DAI0_PIN08 |
| A16 | USB0_DP | C17 | PE_14 | E18 | PF_04 | G19 | DAI0_PIN10 |
| A17 | USB0_DM | C18 | GND | E19 | DAI0_PIN07 | G20 | DAI0_PIN09 |
| A18 | PF_03 | C19 | PF_08 | E20 | DAI0_PIN03 | H01 | PE_01 |
| A19 | PF_05 | C20 | PF_11 | F01 | PC_02 | H02 | PC_09 |
| A20 | GND | D01 | PC_06 | F02 | PC_03 | H03 | PC_15 |
| B01 | PC_12 | D02 | PC_08 | F03 | PC_04 | H04 | VDD_EXT |
| B02 | GND | D03 | PE_04 | F04 | PE_06 | H05 | VDD_INT |
| B03 | PA_13 | D04 | GND | F05 | VDD_INT | H06 | GND |
| B04 | PA_15 | D05 | PE_08 | F06 | GND | H07 | GND |
| B05 | PB_01 | D06 | PE_11 | F07 | VDD_INT | H08 | GND |
| B06 | PB_04 | D07 | PE_09 | F08 | VDD_INT | H09 | GND |
| B07 | MLB0_DATN | D08 | PB_08 | F09 | VDD_INT | H10 | GND |
| B08 | MLB0_DATP | D09 | PB_07 | F10 | VDD_INT | H11 | GND |
| B09 | MLB0_SIGP | D10 | PB_09 | F11 | VDD_INT | H12 | GND |
| B10 | $\overline{\text{JTG\_TRST}}$ | D11 | SYS_CLKOUT | F12 | VDD_INT | H13 | GND |
| B11 | USB0_VBUS | D12 | PB_11 | F13 | VDD_INT | H14 | GND |
| B12 | USB0_XTAL | D13 | USB0_VBC | F14 | VDD_INT | H15 | GND |
| B13 | PB_10 | D14 | PB_14 | F15 | GND | H16 | VDD_INT |
| B14 | JTG_TDO | D15 | PE_13 | F16 | VDD_INT | H17 | VDD_EXT |
| B15 | JTG_TMS | D16 | PE_12 | F17 | PF_02 | H18 | DAI0_PIN05 |
| B16 | PF_00 | D17 | GND | F18 | PF_09 | H19 | DAI0_PIN14 |
| B17 | PF_01 | D18 | PF_10 | F19 | DAI0_PIN02 | H20 | DAI0_PIN11 |
| B18 | PF_06 | D19 | DAI0_PIN01 | F20 | DAI0_PIN06 | J01 | PE_00 |
| B19 | GND | D20 | DAI0_PIN04 | G01 | PC_00 | J02 | PC_07 |
| B20 | PF_07 | E01 | PC_05 | G02 | PC_14 | J03 | PC_10 |
| C01 | PC_11 | E02 | PE_05 | G03 | PC_01 | J04 | VDD_EXT |

| Ball No. | Pin Name |
|---|---|
| V17 | DMC0_BA1 |
| V18 | GND |
| V19 | DMC0_A04 |
| V20 | DMC0_A05 |
| W01 | TWI2_SCL |
| W02 | GND |
| W03 | DMC0_DQ12 |
| W04 | DMC0_DQ11 |
| W05 | DMC0_DQ09 |
| W06 | PD_02 |
| W07 | PD_00 |
| W08 | PA_07 |
| W09 | PA_06 |
| W10 | PA_04 |
| W11 | DMC0_DQ05 |
| W12 | DMC0_DQ04 |
| W13 | DMC0_DQ03 |
| W14 | DMC0_DQ02 |
| W15 | $\overline{\text{SYS\_FAULT}}$ |
| W16 | DMC0_ODT |
| W17 | DMC0_A08 |
| W18 | SYS_BMODE1 |
| W19 | GND |
| W20 | DMC0_A07 |
| Y01 | GND |
| Y02 | $\overline{\text{DMC0\_UDQS}}$ |
| Y03 | DMC0_UDQS |
| Y04 | DMC0_DQ10 |
| Y05 | DMC0_DQ08 |
| Y06 | DMC0_UDM |
| Y07 | DMC0_LDM |
| Y08 | DMC0_CK |
| Y09 | $\overline{\text{DMC0\_CK}}$ |
| Y10 | DMC0_DQ07 |
| Y11 | DMC0_DQ06 |
| Y12 | DMC0_LDQS |
| Y13 | $\overline{\text{DMC0\_LDQS}}$ |
| Y14 | DMC0_DQ01 |
| Y15 | DMC0_DQ00 |
| Y16 | DMC0_CKE |
| Y17 | $\overline{\text{DMC0\_CS0}}$ |
| Y18 | SYS_BMODE0 |
| Y19 | SYS_BMODE2 |
| Y20 | GND |

## ORDERING GUIDE

| Model[1, 2] | Processor Instruction Rate (Max) | ARM Instruction Rate (Max)[3] | Temperature Range[4] | ARM Cores[3] | SHARC+ Cores | External Memory Ports | Package Description | Package Option |
|---|---|---|---|---|---|---|---|---|
| ADSP-21571KSWZ-4 | 450 MHz | N/A | 0°C to +70°C | N/A | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-21571BSWZ-4 | 450 MHz | N/A | –40°C to +85°C | N/A | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-21571CSWZ-4 | 450 MHz | N/A | –40°C to +105°C | N/A | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-21571KSWZ-5 | 500 MHz | N/A | 0°C to +70°C | N/A | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-21571BSWZ-5 | 500 MHz | N/A | –40°C to +85°C | N/A | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-21571CSWZ-5 | 500 MHz | N/A | –40°C to +100°C | N/A | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-21573KBCZ-4 | 450 MHz | N/A | 0°C to +70°C | N/A | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-21573BBCZ-4 | 450 MHz | N/A | –40°C to +85°C | N/A | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-21573CBCZ-4 | 450 MHz | N/A | –40°C to +100°C | N/A | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-21573KBCZ-5 | 500 MHz | N/A | 0°C to +70°C | N/A | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-21573BBCZ-5 | 500 MHz | N/A | –40°C to +85°C | N/A | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-21573CBCZ-5 | 500 MHz | N/A | –40°C to +95°C | N/A | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC570KSWZ-42 | 450 MHz | 225 MHz | 0°C to +70°C | 1 | 1 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC570BSWZ-42 | 450 MHz | 225 MHz | –40°C to +85°C | 1 | 1 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC570CSWZ-42 | 450 MHz | 225 MHz | –40°C to +105°C | 1 | 1 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC570KSWZ-4 | 450 MHz | 450 MHz | 0°C to +70°C | 1 | 1 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC570BSWZ-4 | 450 MHz | 450 MHz | –40°C to +85°C | 1 | 1 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC570CSWZ-4 | 450 MHz | 450 MHz | –40°C to +105°C | 1 | 1 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571KSWZ-3 | 300 MHz | 300 MHz | 0°C to +70°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571BSWZ-3 | 300 MHz | 300 MHz | –40°C to +85°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571CSWZ-3 | 300 MHz | 300 MHz | –40°C to +105°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571KSWZ-4 | 450 MHz | 450 MHz | 0°C to +70°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571BSWZ-4 | 450 MHz | 450 MHz | –40°C to +85°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571CSWZ-4 | 450 MHz | 450 MHz | –40°C to +105°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571KSWZ-5 | 500 MHz | 500 MHz | 0°C to +70°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571BSWZ-5 | 500 MHz | 500 MHz | –40°C to +85°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC571CSWZ-5 | 500 MHz | 500 MHz | –40°C to +100°C | 1 | 2 | 0 | 176-Lead LQFP_EP | SW-176-5 |
| ADSP-SC572KBCZ-42 | 450 MHz | 225 MHz | 0°C to +70°C | 1 | 1 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC572BBCZ-42 | 450 MHz | 225 MHz | –40°C to +85°C | 1 | 1 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC572CBCZ-42 | 450 MHz | 225 MHz | –40°C to +100°C | 1 | 1 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC572KBCZ-4 | 450 MHz | 450 MHz | 0°C to +70°C | 1 | 1 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC572BBCZ-4 | 450 MHz | 450 MHz | –40°C to +85°C | 1 | 1 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC572CBCZ-4 | 450 MHz | 450 MHz | –40°C to +100°C | 1 | 1 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573KBCZ-3 | 300 MHz | 300 MHz | 0°C to +70°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573BBCZ-3 | 300 MHz | 300 MHz | –40°C to +85°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573CBCZ-3 | 300 MHz | 300 MHz | –40°C to +100°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573KBCZ-4 | 450 MHz | 450 MHz | 0°C to +70°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573BBCZ-4 | 450 MHz | 450 MHz | –40°C to +85°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573CBCZ-4 | 450 MHz | 450 MHz | –40°C to +100°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573KBCZ-5 | 500 MHz | 500 MHz | 0°C to +70°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573BBCZ-5 | 500 MHz | 500 MHz | –40°C to +85°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |
| ADSP-SC573CBCZ-5 | 500 MHz | 500 MHz | –40°C to +95°C | 1 | 2 | 1 | Pad 400-Ball CSP_BGA | BC-400-2 |

[1] Z =RoHS Compliant Part.

[2] For evaluation of all models, order the ADZS-SC573-EZLITE evaluation board.

[3] N/A means not applicable.

[4] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature ($T_J$) specification which is the only temperature specification.