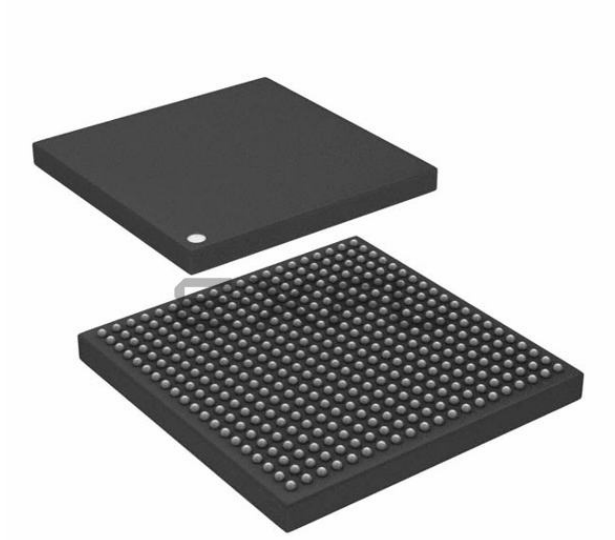

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	CAN, EBI/EMI, Ethernet, DAI, I²C, MMC/SD/SDIO, SPI, SPORT, UART/USART, USB OTG
Clock Rate	450MHz, 450MHz
Non-Volatile Memory	External
On-Chip RAM	2MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-sc573kbcz-4

Table 2. Comparison of ADSP-SC57x/ADSP-2157x Processor Features[1]

Processor Feature		ADSP-SC570	ADSP-SC571	ADSP-SC572	ADSP-SC573	ADSP-21571	ADSP-21573
ARM Cortex-A5 (MHz, Max)		450	500	450	500	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	500	450	500	500	500
SHARC+ Core2 (MHz, Max)		N/A	500	N/A	500	500	500
SHARC L1 SRAM (kB)		1 × 384	2 × 384	1 × 384	2 × 384	2 × 384	2 × 384
System Memory	L2 SRAM (Shared) (MB)	1	1	1	1	1	1
	DDR3/DDR2/LPDDR1 Controller (16-bit)	N/A	N/A	1	1	N/A	1
USB 2.0 HS + PHY (Host/Device/OTG)		N/A	N/A	1	1	N/A	N/A
EMAC Std/AVB + Timer IEEE 1588		10/100	10/100	10/100/1000	10/100/1000	N/A	N/A
SDIO/eMMC		N/A	N/A	1	1	N/A	N/A
Link Ports		1	1	2	2	1	2
GPIO Ports		Port A to D	Port A to D	Port A to F	Port A to F	Port A to D	Port A to F
GPIO + DAI Pins		64 + 20	64 + 20	92 + 20	92 + 20	64 + 20	92 + 20
Package Options		176-LQFP	176-LQFP	400-BGA	400-BGA	176-LQFP	400-BGA

[1] N/A means not applicable.

Table 3. Comparison of ADSP-SC57x/ADSP-2157x Processor Features for Automotive [1]

Processor Feature		ADSP-SC570W	ADSP-SC571W	ADSP-SC572W	ADSP-SC573W	ADSP-21571W	ADSP-21573W
ARM Cortex-A5 (MHz, Max)		450	500	450	500	N/A	N/A
ARM Core L1 Cache (I, D kB)		32, 32	32, 32	32, 32	32, 32	N/A	N/A
ARM Core L2 Cache (kB)		256	256	256	256	N/A	N/A
SHARC+ Core1 (MHz, Max)		450	500	450	500	500	500
SHARC+ Core2 (MHz, Max)		N/A	500	N/A	500	500	500
SHARC L1 SRAM (kB)		1 × 384	2 × 384	1 × 384	2 × 384	2 × 384	2 × 384
System Memory	L2 SRAM (Shared) (MB)	1	1	1	1	1	1
	DDR3/DDR2/LPDDR1 Controller (16-bit)	N/A	N/A	1	1	N/A	1
USB 2.0 HS + PHY (Host/Device/OTG)		N/A	N/A	1	1	N/A	N/A
EMAC Std/AVB + Timer IEEE 1588		10/100	10/100	10/100/1000	10/100/1000	N/A	N/A
SDIO/eMMC		N/A	N/A	1	1	N/A	N/A
MLB 3-Pin/6-Pin		3-pin	3-pin	6-pin/3-pin	6-pin/3-pin	3-pin	6-pin/3-pin
Link Ports		1	1	2	2	1	2
GPIO Ports		Port A to D	Port A to D	Port A to F	Port A to F	Port A to D	Port A to F
GPIO + DAI Pins		64 + 20	64 + 20	92 + 20	92 + 20	64 + 20	92 + 20
Package Options		176-LQFP	176-LQFP	400-BGA	400-BGA	176-LQFP	400-BGA

[1] N/A means not applicable.

Single-Instruction, Multiple Data (SIMD) Computational Engine

The SHARC+ core contains two computational processing elements that operate as a single-instruction, multiple data (SIMD) engine.

The processing elements are referred to as PEx and PEy data registers and each contain an arithmetic logic unit (ALU), multiplier, shifter, and register file. PEx is always active and PEy is enabled by setting the PEYEN mode bit in the mode control register (MODE1).

SIMD mode allows the processors to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture efficiently executes math intensive DSP algorithms. In addition to all the features of previous generation SHARC cores, the SHARC+ core also provides a new and simpler way to execute an instruction only on the PEy data register.

SIMD mode also affects the way data transfers between memory and the processing elements because to sustain computational operation in the processing elements requires twice the data bandwidth. Therefore, entering SIMD mode doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values transfer with each memory or register file access.

Independent Parallel Computation Units

Within each processing element is a set of pipelined computational units. The computational units consist of a multiplier, arithmetic/logic unit (ALU), and shifter. These units are arranged in parallel, maximizing computational throughput. These computational units support IEEE 32-bit single-precision floating-point, 40-bit extended-precision floating-point, IEEE 64-bit double-precision floating-point, and 32-bit fixed-point data formats.

A multifunction instruction set supports parallel execution of the ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements per core.

All processing operations take one cycle to complete. For all floating-point operations, the processor takes two cycles to complete in case of data dependency. Double-precision floating-point data take two to six cycles to complete. The processor stalls for the appropriate number of cycles for an interlocked pipeline plus data dependency check.

Core Timer

Each SHARC+ processor core also has a timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register register files (16 primary, 16 secondary), combined with the enhanced Harvard architecture of the processor, allow unconstrained data flow between computation units and internal memory. The registers in the PEx data register file are referred to as R0–R15 and in the PEy data register file as S0–S15.

Context Switch

Many of the registers of the processor have secondary registers that can activate during interrupt servicing for a fast context switch. The data, DAG, and multiplier result registers have secondary registers. The primary registers are active at reset, while control bits in MODE1 activate the secondary registers.

Universal Registers

General-purpose tasks use the universal registers. The four USTAT registers allow easy bit manipulations (set, clear, toggle, test, XOR) for all control and status peripheral registers.

The data bus exchange register (PX) permits data to pass between the 64-bit PM data bus and the 64-bit DM data bus or between the 40-bit register file and the PM or DM data bus. These registers contain hardware to handle the data width difference.

Data Address Generators (DAG) With Zero-Overhead Hardware Circular Buffer Support

For indirect addressing and implementing circular data buffers in hardware, the ADSP-SC57x/ADSP-2157x processor uses the two data address generators (DAGs). Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and fast Fourier transforms (FFT). The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets and 16 secondary sets). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set Architecture (ISA)

The flexible instruction set architecture (ISA), a 48-bit instruction word, accommodates various parallel operations for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction. Additionally, the double-precision floating-point instruction set is an addition to the SHARC+ core.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the SHARC+ core processors support 16-bit and 32-bit opcodes for many instructions, formerly 48-bit in the ISA. This feature, called variable instruction set architecture (VISA), drops redundant or unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external memories. VISA is not an operating mode; it is only address dependent (refer to memory map ISA/VISA address spaces in Table 7). Furthermore, it allows jumps between ISA and VISA instruction fetches.

Single-Cycle Fetch of Instructional Four Operands

The ADSP-SC57x/ADSP-2157x processors feature an enhanced Harvard architecture in which the DM bus transfers data and PM bus transfers both instructions and data.

With the separate program memory bus, data memory buses, and on-chip instruction conflict cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction from the conflict cache, in a single cycle.

Core Event Controller (CEC)

The SHARC+ core generates various core interrupts (including arithmetic and circular buffer instruction flow exceptions) and SEC events (debug or monitor and software). The core event controller (CEC) is used to unmask interrupts for core processing (enabled in the IMASK register).

Instruction Conflict Cache

The processors include a 32-entry instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions that require fetches conflict with the PM bus data accesses cache. This cache allows full speed execution of core, looped operations, such as digital filter multiply accumulates, and FFT butterfly processing. The conflict cache serves for on-chip bus conflicts only.

Branch Target Buffer (BTB)/Branch Predictor (BP)

Implementation of a hardware-based branch predictor (BP) and branch target buffer (BTB) reduce branch delay. The program sequencer supports efficient branching using the BTB for conditional and unconditional instructions.

Addressing Spaces

In addition to traditionally supported long word, normal word, extended precision word, and short word addressing aliases, the processors support byte addressing for the data and instruction accesses. The enhanced ISA/VISA provides new instructions for accessing all sizes of data from byte space as well as converting word addresses to byte and byte to word addresses.

Additional Features

The enhanced ISA/VISA of the ADSP-SC57x/ADSP-2157x processors provides a memory barrier instruction for data synchronization, exclusive data access support for multicore data sharing, and exclusive data access to enable multiprocessor programming. To enhance the reliability of the application, L1 data RAMs support parity error detection logic for every byte. Additionally, the processors detect illegal opcodes. Core interrupts flag both errors. Master ports of the core also detect for failed external accesses.

SYSTEM INFRASTRUCTURE

The following sections describe the system infrastructure of the ADSP-SC57x/ADSP-2157x processors.

System L2 Memory

A system L2 SRAM memory of 8 Mb (1 MB) is available to both SHARC+ cores, the ARM Cortex-A5 core, and the system DMA channels (see Table 5). The L2 SRAM block is subdivided into eight banks to support concurrent access to the L2 memory ports. Memory accesses to the L2 memory space are multicycle accesses by both the ARM Cortex-A5 and SHARC+ cores.

The memory space is used for various situations including

- ARM Cortex-A5 to SHARC+ core data sharing and intercore communications
- Accelerator and peripheral sources and destination memory to avoid accessing data in the external memory
- A location for DMA descriptors
- Storage for additional data for either the ARM Cortex-A5 or SHARC+ cores to avoid external memory latencies and reduce external memory bandwidth
- Storage for incoming Ethernet traffic to improve performance
- Storage for data coefficient tables cached by the SHARC+ core

See System Memory Protection Unit (SMPU) section for options in limiting access by specific cores and DMA masters.

The ARM Cortex-A5 core has an L1 instruction and data cache, each of which is 32 kB in size. The core also has an L2 cache controller of 256 kB. When enabling the caches, accesses to all other memory spaces (internal and external) go through the cache.

SHARC+ Core L1 Memory in Multiprocessor Space

The ARM Cortex-A5 core can access the L1 memory of the SHARC+ core. See Table 6 for the L1 memory address in multiprocessor space. The SHARC+ core can access the L1 memory of the other SHARC+ core in the multiprocessor space.

One Time Programmable Memory (OTP)

The processors feature 7 Kb of one time programmable (OTP) memory which is memory map accessible. This memory can be programmed with custom keys and it supports secure boot and secure operation.

I/O Memory Space

Mapped I/Os include SPI2 memory address space (see Table 7).

Board Support Packages (BSPs) for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add ins called board support packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product.

Middleware Packages

Analog Devices offers middleware add ins such as real-time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the following web pages:

- www.analog.com/ucos2
- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/ucusbh
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add ins that perform popular audio and video processing algorithms. These are available for use with CrossCore Embedded Studio. For more information visit www.analog.com.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG test access port (TAP). In circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the internal features of the processor via the TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers.

The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the JTAG port of the DSP to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see "Analog Devices JTAG Emulation Technical Reference" (EE-68).

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-SC57x/ADSP-2157x architecture and functionality. For detailed information on the core architecture and instruction set, refer to the SHARC+ Core Programming Reference.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (www.analog.com\circuits) provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

176-LEAD LQFP SIGNAL DESCRIPTIONS

The processor pin definitions are shown Table 20 for the 176-lead LQFP package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a GPIO port pin.
- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a GPIO pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the Digital Audio Interface (DAI) chapter of the ADSP-SC57x/ADSP-2157x SHARC+ Processor Hardware Reference for complete information on the use of the DAIs and SRUs.

Table 20. ADSP-SC57x/ADSP-2157x 176-Lead LQFP Signal Descriptions

Signal Name	Description	Port	Pin Name
ACM0_A0	ACM0 ADC Control Signals	A	PA_08
ACM0_A1	ACM0 ADC Control Signals	C	PC_14
ACM0_A2	ACM0 ADC Control Signals	C	PC_15
ACM0_A3	ACM0 ADC Control Signals	A	PA_14
ACM0_A4	ACM0 ADC Control Signals	B	PB_01
ACM0_T0	ACM0 External Trigger n	A	PA_15
C1_FLG0	SHARC Core 1 Flag Pin	D	PD_00
C1_FLG1	SHARC Core 1 Flag Pin	D	PD_01
C1_FLG2	SHARC Core 1 Flag Pin	C	PC_09
C1_FLG3	SHARC Core 1 Flag Pin	D	PD_06
C2_FLG0	SHARC Core 2 Flag Pin	B	PB_00
C2_FLG1	SHARC Core 2 Flag Pin	C	PC_14
C2_FLG2	SHARC Core 2 Flag Pin	C	PC_15
C2_FLG3	SHARC Core 2 Flag Pin	D	PD_05
CAN0_RX	CAN0 Receive	C	PC_12
CAN0_TX	CAN0 Transmit	C	PC_13
CAN1_RX	CAN1 Receive	C	PC_14
CAN1_TX	CAN1 Transmit	C	PC_15
CNT0_DG	CNT0 Count Down and Gate	D	PD_08
CNT0_UD	CNT0 Count Up and Direction	D	PD_00
CNT0_ZM	CNT0 Count Zero Marker	D	PD_07
DAI0_PIN01	DAI0 Pin 1	Not Muxed	DAI0_PIN01
DAI0_PIN02	DAI0 Pin 2	Not Muxed	DAI0_PIN02
DAI0_PIN03	DAI0 Pin 3	Not Muxed	DAI0_PIN03
DAI0_PIN04	DAI0 Pin 4	Not Muxed	DAI0_PIN04
DAI0_PIN05	DAI0 Pin 5	Not Muxed	DAI0_PIN05
DAI0_PIN06	DAI0 Pin 6	Not Muxed	DAI0_PIN06
DAI0_PIN07	DAI0 Pin 7	Not Muxed	DAI0_PIN07
DAI0_PIN08	DAI0 Pin 8	Not Muxed	DAI0_PIN08
DAI0_PIN09	DAI0 Pin 9	Not Muxed	DAI0_PIN09
DAI0_PIN10	DAI0 Pin 10	Not Muxed	DAI0_PIN10
DAI0_PIN11	DAI0 Pin 11	Not Muxed	DAI0_PIN11
DAI0_PIN12	DAI0 Pin 12	Not Muxed	DAI0_PIN12
DAI0_PIN13	DAI0 Pin 13	Not Muxed	DAI0_PIN13
DAI0_PIN14	DAI0 Pin 14	Not Muxed	DAI0_PIN14

ADSP-SC57x/ADSP-2157x DESIGNER QUICK REFERENCE

Table 25 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The type column identifies the I/O type or supply type of the pin. The abbreviations used in this column are analog (a), supply (s), ground (g) and Input, Output, and InOut.
- The driver type column identifies the driver type used by the corresponding pin. The driver types are defined in the Output Drive Currents section of this data sheet.
- The internal termination column specifies the termination present after the processor is powered up (both during reset and after reset).
- The reset drive column specifies the active drive on the signal when the processor is in the reset state.
- The power domain column specifies the power supply domain in which the signal resides.
- The description and notes column identifies any special requirements or characteristics for a signal. These recommendations apply whether or not the hardware block associated with the signal is featured on the product. If no special requirements are listed, the signal can be left unconnected if it is not used. For multiplexed GPIO pins, this column identifies the functions available on the pin.

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
DAI0_PIN01	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 1 Notes: See note[2]
DAI0_PIN02	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 2 Notes: See note[2]
DAI0_PIN03	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 3 Notes: See note[2]
DAI0_PIN04	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 4 Notes: See note[2]
DAI0_PIN05	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 5 Notes: See note[2]
DAI0_PIN06	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 6 Notes: See note[2]
DAI0_PIN07	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 7 Notes: See note[2]
DAI0_PIN08	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 8 Notes: See note[2]
DAI0_PIN09	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 9 Notes: See note[2]
DAI0_PIN10	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 10 Notes: See note[2]
DAI0_PIN11	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 11 Notes: See note[2]
DAI0_PIN12	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 12 Notes: See note[2]
DAI0_PIN13	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 13 Notes: See note[2]
DAI0_PIN14	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 14 Notes: See note[2]
DAI0_PIN15	InOut	A	Programmable PullUp[1]	none	VDD_EXT	Desc: DAI0 Pin 15 Notes: See note[2]

Table 25. ADSP-SC57x/ADSP-2157x Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Drive	Power Domain	Description and Notes
SYS_CLKIN1	a	NA	none	none	VDD_EXT	Desc: Clock/Crystal Input Notes: Connect to GND if not used
SYS_CLKOUT	a	H	none	High-Z when $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ are both active[5]	VDD_EXT	Desc: Processor Clock Output Notes: No notes
SYS_FAULT	InOut	A	none	none	VDD_EXT	Desc: Active-High Fault Output Notes: Pull down if not used
$\overline{\text{SYS\_FAULT}}$	InOut	A	none	none	VDD_EXT	Desc: Active-Low Fault Output Notes: Pull up if not used
$\overline{\text{SYS\_HWRST}}$	Input	NA	none	none	VDD_EXT	Desc: Processor Hardware Reset Control Notes: No connection not allowed
$\overline{\text{SYS\_RESOUT}}$	Output	A	none	High-Z when $\overline{\text{SYS\_HWRST}}$ and $\overline{\text{JTG\_TRST}}$ are both active[5]	VDD_EXT	Desc: Reset Output Notes: No notes
SYS_XTAL0	a	NA	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
SYS_XTAL1	a	NA	none	none	VDD_EXT	Desc: Crystal Output Notes: No notes
TWI0_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI0 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI0_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI0 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
TWI1_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI1 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI1_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI1 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
TWI2_SCL	InOut	D	none	none	VDD_EXT	Desc: TWI2 Serial Clock Notes: Add external pull-up if used. Connect to GND if not used.
TWI2_SDA	InOut	D	none	none	VDD_EXT	Desc: TWI2 Serial Data Notes: Add external pull-up if used. Connect to GND if not used.
USB0_DM	InOut	F	none	none	VDD_USB	Desc: USB0 Data– Notes: Add external pull-down if not used[6]
USB0_DP	InOut	F	none	none	VDD_USB	Desc: USB0 Data + Notes: Add external pull-down if not used[6]
USB0_ID	InOut		none	none	VDD_USB	Desc: USB0 OTG ID Notes: Connect to GND when USB is not used[6]

Parameter		Conditions	Min	Nominal	Max	Unit
AUTOMOTIVE USE ONLY						
T_J	Junction Temperature 400-Ball CSP_BGA (Automotive Grade)	$T_{AMBIENT}$ = –40°C to +105°C CCLK ≤ 450 MHz	–40		+130[9]	°C
T_J	Junction Temperature 176-Lead LQFP-EP (Automotive Grade)	$T_{AMBIENT}$ = –40°C to +105°C CCLK ≤ 450 MHz	–40		+125[9]	°C
T_J	Junction Temperature 400-Ball CSP_BGA (Automotive Grade)	$T_{AMBIENT}$ = –40°C to +105°C CCLK ≤ 500 MHz	–40		+133[9]	°C
T_J	Junction Temperature 176-Lead LQFP-EP (Automotive Grade)	$T_{AMBIENT}$ = –40°C to +105°C CCLK ≤ 500 MHz	–40		+130[9]	°C

[1] Applies to DDR2/DDR3/LPDDR signals.
[2] If not used, V_{DD_USB} must be connected to 3.3 V.
[3] V_{HADC_VREF} must always be less than V_{DD_HADC}.
[4] Parameter value applies to all input and bidirectional pins except the TWI, DMC, USB, and MLB pins.
[5] Parameter applies to TWI signals.
[6] TWI signals are pulled up to V_{BUSTWI}. See Table 26.
[7] This parameter applies to all DMC0 signals in DDR2/DDR3 mode. V_{REF} is the voltage applied to the V_{REF_DMC} pin, nominally $V_{DD\_DMC}/2$.
[8] This parameter applies to DMC0 signals in LPDDR mode.
[9] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

Table 26. TWI_VSEL Selections and V_{DD_EXT}/V_{BUSTWI}

TWI_VSEL Selections	V_{DD_EXT} Nominal	V_{BUSTWI}			Unit
		Min	Nominal	Max	
TWI000[1]	3.30	3.13	3.30	3.47	V
TWI100	3.30	4.75	5.00	5.25	V

[1] Designs must comply with the V_{DD_EXT} and V_{BUSTWI} voltages specified for the default TWI_DT setting for correct JTAG boundary scan operation during reset.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 40 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 40. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.33 V to +1.26 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.33 V to +3.60 V
DDR2/LPDDR Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.90 V
DDR3 Controller Supply Voltage (V_{DD_DMC})	–0.33 V to +1.60 V
DDR2 Reference Voltage (V_{DDR_VREF})	–0.33 V to +1.90 V
USB PHY Supply Voltage (V_{DD_USB})	–0.33 V to +3.60 V
HADC Supply Voltage (V_{DD_HADC})	–0.33 V to +3.60 V
HADC Reference Voltage (V_{HADC_REF})	–0.33 V to +3.60 V
DDR2/LPDDR Input Voltage[1]	–0.33 V to +1.90 V
DDR3 Input Voltage[1]	–0.33 V to +1.60 V
Digital Input Voltage[1, 2]	–0.33 V to +3.60 V
TWI Input Voltage[1, 3]	–0.33 V to +5.50 V
USB0_Dx Input Voltage[1, 4]	–0.33 V to +5.25 V
USB0_VBUS Input Voltage[1, 4]	–0.33 V to +6 V
Output Voltage Swing	–0.33 V to V_{DD_EXT} +0.5 V
Analog Input Voltage[5]	–0.2 V to V_{DD_HADC} +0.2 V
I_{OH}/I_{OL} Current per Signal[2]	6 mA (maximum)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	133°C

[1] Applies only when the related power supply (V_{DD_DMC}, V_{DD_EXT}, or V_{DD_USB}) is within specification. When the power supply is below specification, the range is the voltage being applied to that power domain ± 0.2 V.

[2] Applies to 100% transient duty cycle.

[3] Applies to TWI_SCL and TWI_SDA.

[4] If the USB is not used, connect these pins according to Table 25.

[5] Applies only when V_{DD_HADC} is within specifications and ≤ 3.4 V. When V_{DD_HADC} is within specifications and > 3.4 V, the maximum rating is 3.6 V. When V_{DD_HADC} is below specifications, the range is V_{DD_HADC} ± 0.2 V.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

DDR3 SDRAM Clock and Control Cycle Timing

Table 49 and Figure 16 show mobile DDR3 SDRAM clock and control cycle timing, related to the DMC.

Table 49. DDR3 SDRAM Clock and Control Cycle Timing, V_{DD_DMC} Nominal 1.5 V

Parameter		450 MHz[1]		Unit
		Min	Max	
Switching Characteristics				
t_{CK}	Clock Cycle Time (CL = 2 Not Supported)	2.22		ns
$t_{CH(abs)}$[2]	Minimum Clock Pulse Width	0.47	0.53	t_{CK}
$t_{CL(abs)}$[2]	Maximum Clock Pulse Width	0.47	0.53	t_{CK}
t_{IS}	Control/Address Setup Relative to DMC0_CK Rise	0.2		ns
t_{IH}	Control/Address Hold Relative to DMC0_CK Rise	0.275		ns

[1] To ensure proper operation of the DDR3, all the DDR3 requirements must be strictly followed. See "Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors" (EE-387).
[2] As per JESD79-3F definition.

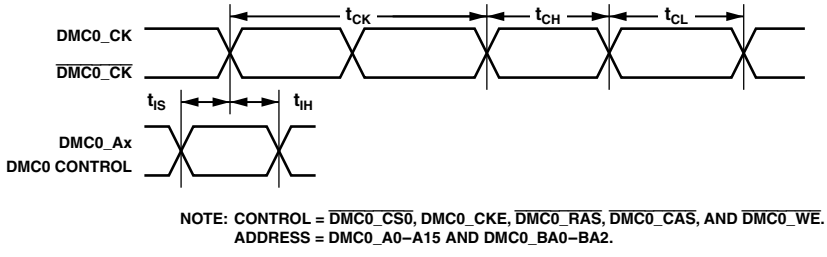

Figure 16. DDR3 SDRAM Clock and Control Cycle Timing

Table 53. Enhanced Parallel Peripheral Interface (EPPI)—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	EPPI_CLK Width[1]	0.5 × $t_{PCLKEXT}$ – 0.5		ns
t_{PCLK}	EPPI_CLK Period[1]	$t_{PCLKEXT}$ – 1		ns
t_{SFSPE}	External FS Setup Before EPPI_CLK	2		ns
t_{HFSPE}	External FS Hold After EPPI_CLK	3.7		ns
t_{SDRPE}	Receive Data Setup Before EPPI_CLK	2		ns
t_{HDRPE}	Receive Data Hold After EPPI_CLK	3.7		ns
Switching Characteristics				
t_{DFSPE}	Internal FS Delay After EPPI_CLK		15.3	ns
t_{HOFSPE}	Internal FS Hold After EPPI_CLK	2.4		ns
t_{DDTPE}	Transmit Data Delay After EPPI_CLK		15.3	ns
t_{HDTPE}	Transmit Data Hold After EPPI_CLK	2.4		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external EPPI_CLK. For the external EPPI_CLK ideal maximum frequency, see the $f_{PCLKEXT}$ specification in Table 27.

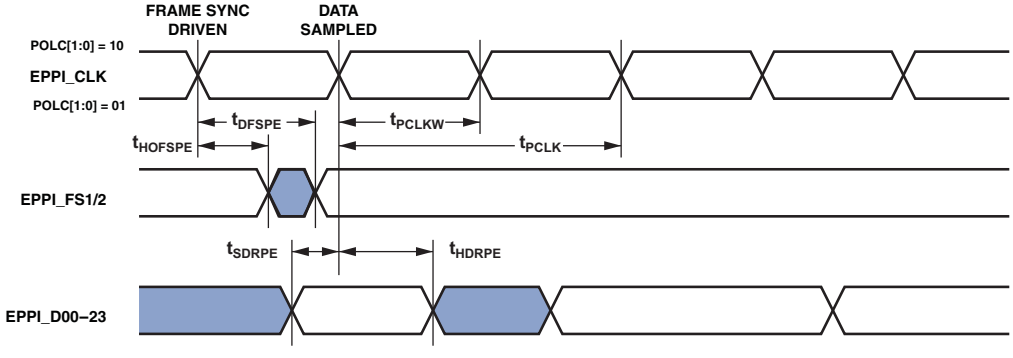

Figure 24. EPPI External Clock GP Receive Mode with Internal Frame Sync Timing

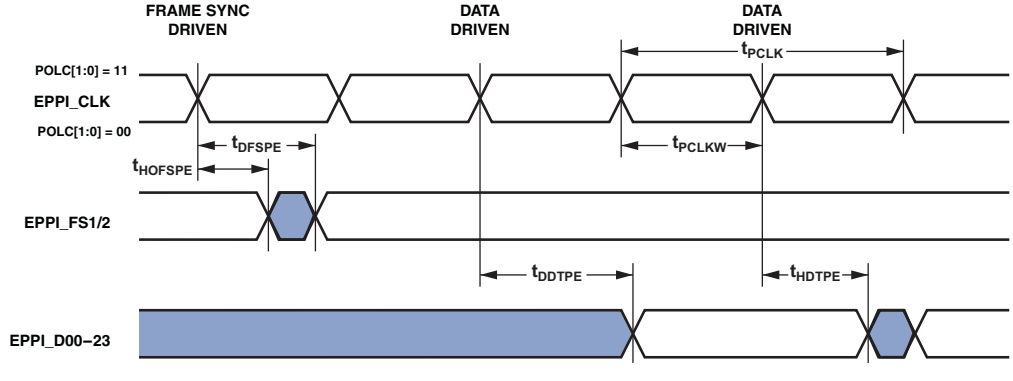

Figure 25. EPPI External Clock GP Transmit Mode with Internal Frame Sync Timing

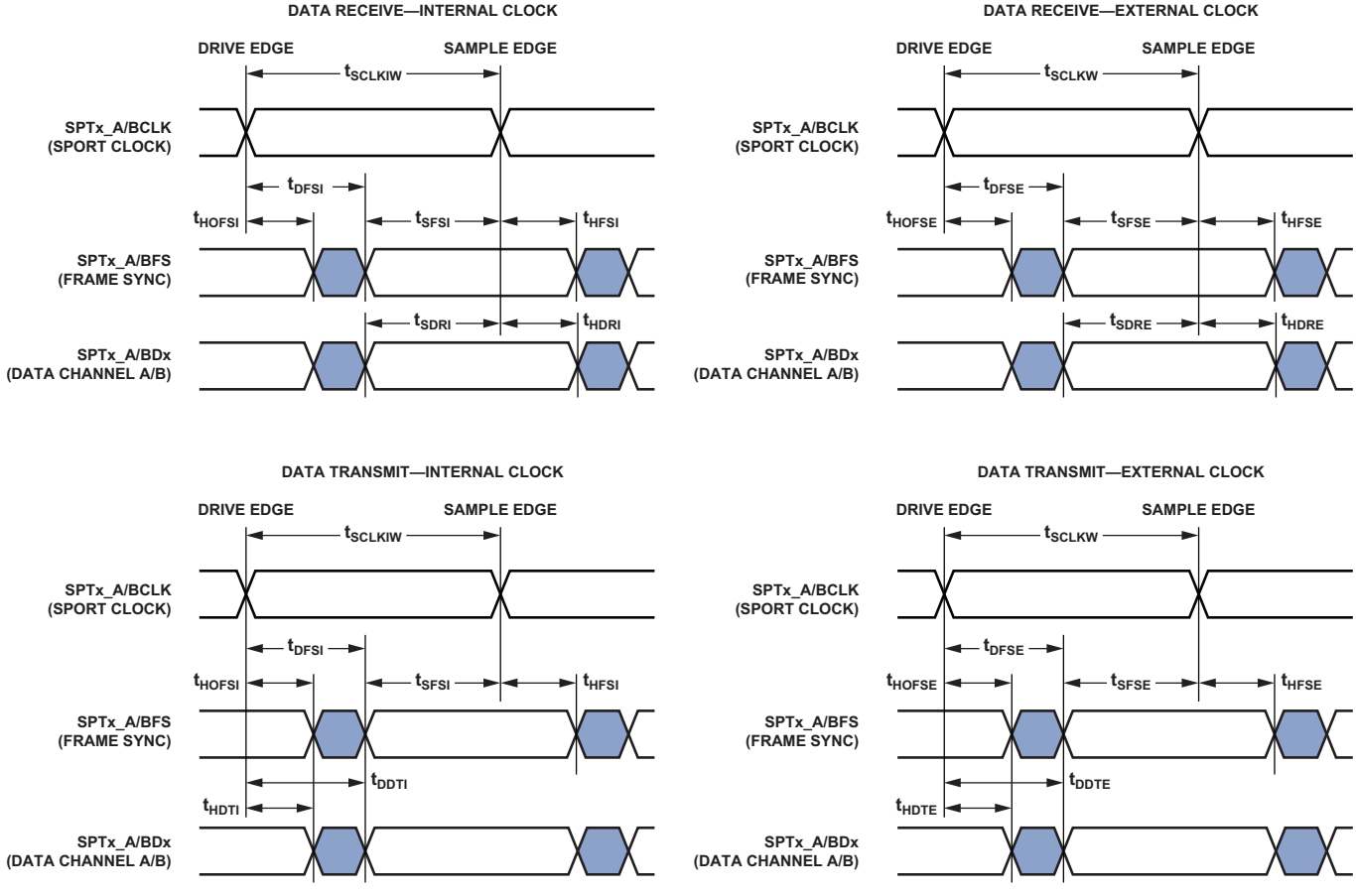

Figure 30. SPORTs

10/100 EMAC Timing

Table 79 through Table 83 and Figure 49 through Figure 53 describe the MII and RMII EMAC operations.

Table 79. 10/100 EMAC Timing: MII Receive Signal

Parameter[1]		V_{DDEXT} 3.3 V Nominal		Unit
		Min	Max	
Timing Requirements				
$t_{ERXCLKF}$	ETH0_RXCLK_REFCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1%	MHz
$t_{ERXCLKW}$	ETH0_RXCLK_REFCLK Width (t_{ERxCLK} = ETH0_RXCLK_REFCLK Period)	t_{ERxCLK} × 35%	t_{ERxCLK} × 65%	ns
$t_{ERXCLKIS}$	Rx Input Valid to ETH0_RXCLK_REFCLK Rising Edge (Data In Setup)	1.75		ns
$t_{ERXCLKIH}$	ETH0_RXCLK_REFCLK Rising Edge to Rx Input Invalid (Data In Hold)	1.5		ns

[1] MII inputs synchronous to ETH0_RXCLK_REFCLK are ETH0_RXD3-0, ETH0_RXCTL_RXDV, and ETH0_RXERR.

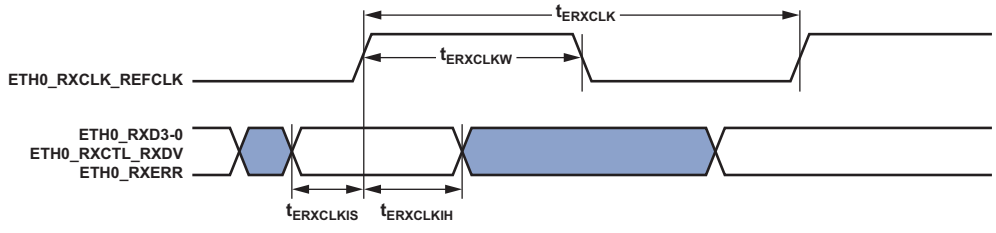

Figure 49. 10/100 EMAC Timing: MII Receive Signal

Table 80. 10/100 EMAC Timing: MII Transmit Signal

Parameter[1]		V_{DDEXT} 3.3 V Nominal		Unit
		Min	Max	
Timing Requirements				
$t_{ETXCLKF}$	ETH0_TXCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1%	MHz
$t_{ETXCLKW}$	ETH0_TXCLK Width (t_{ETxCLK} = ETH0_TXCLK Period)	t_{ETxCLK} × 35%	t_{ETxCLK} × 65%	ns
Switching Characteristics				
$t_{ETXCLKOV}$	ETH0_TXCLK Rising Edge to Tx Output Valid (Data Out Valid)		11.4	ns
$t_{ETXCLKOH}$	ETH0_TXCLK Rising Edge to Tx Output Invalid (Data Out Hold)	2		ns

[1] MII outputs synchronous to ETH0_TXCLK are ETH0_TXD3-0.

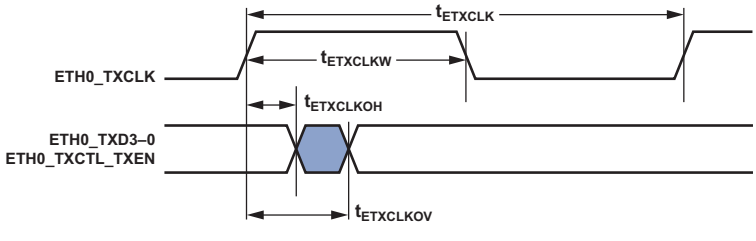

Figure 50. 10/100 EMAC Timing: MII Transmit Signal

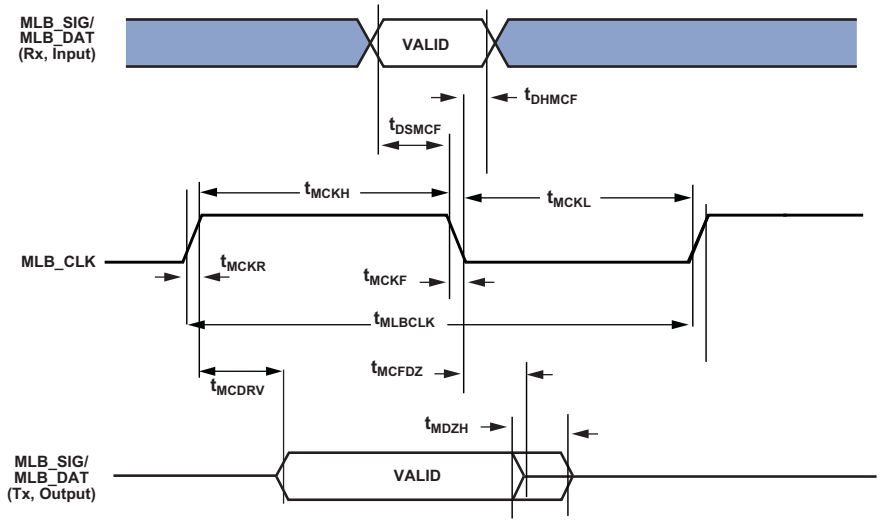

Figure 60. MLB Timing (3-Pin Interface)

The ac timing specifications of the 6-pin MLB interface is detailed in Table 92. Refer to the *Media Local Bus Specification version 4.2* for more details.

Table 92. 6-Pin MLB Interface Specifications

Parameter		Conditions	Min	Typ	Max	Unit
t_{MT}	Differential Transition Time at the Input Pin (See Figure 61)	20% to 80% $V_{IN}+/V_{IN}-$ 80% to 20% $V_{IN}+/V_{IN}-$			1	ns
f_{MCKE}	MLBCP/N External Clock Operating Frequency (See Figure 62)[1]	2048 × FS at 44.0 kHz	90.112			MHz
		2048 × FS at 50.0 kHz			102.4	MHz
f_{MCKR}	Recovered Clock Operating Frequency (Internal, Not Observable at Pins, Only for Timing References) (See Figure 62)	2048 × FS at 44.0 kHz	90.112			MHz
		2048 × FS at 50.0 kHz			102.4	MHz
t_{DELAY}	Transmitter MLBSP/N (MLBDP/N) Output Valid From Transition of MLBCP/N (Low to High) (See Figure 63)	f_{MCKR} = 2048 × FS	0.6		5	ns
t_{PHZ}	Disable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 64)	f_{MCKR} = 2048 × FS	0.6		7	ns
t_{PLZ}	Enable Turnaround Time From Transition of MLBCP/N (Low to High) (See Figure 64)	f_{MCKR} = 2048 × FS	0.6		11.2	ns
t_{SU}	MLBSP/N (MLBDP/N) Valid to Transition of MLBCP/N (Low to High) (See Figure 63)	f_{MCKR} = 2048 × FS	1			ns
t_{HD}	MLBSP/N (MLBDP/N) Hold From Transition of MLBCP/N (Low to High) (See Figure 63)[2]		0.6			ns

[1] f_{MCKE} (maximum) and f_{MCKR} (maximum) include maximum cycle to cycle system jitter (t_{JITTER}) of 600 ps for a bit error rate of 10E-9.
[2] Receivers must latch MLBSP/N (MLBDP/N) data within t_{HD} (minimum) of the rising edge of MLBCP/N.

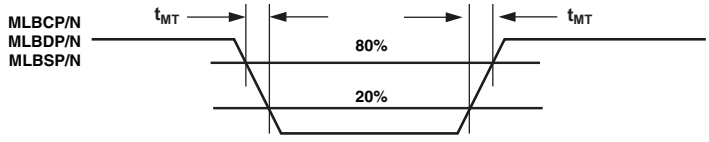

Figure 61. MLB 6-Pin Transition Time

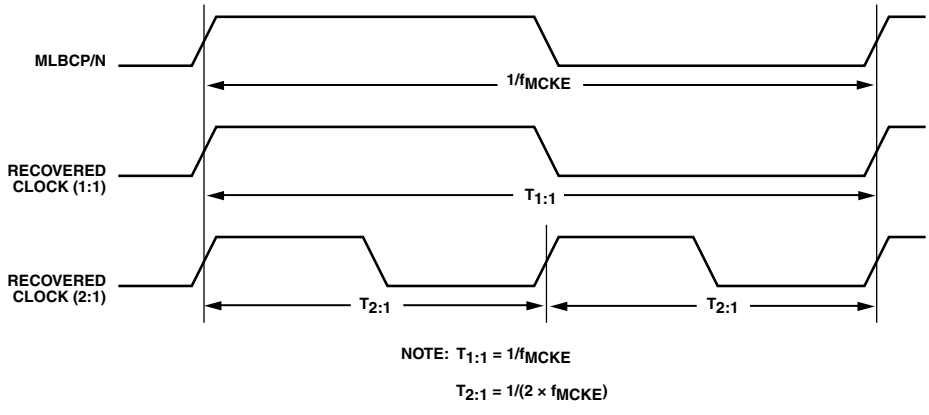

Figure 62. MLB 6-Pin Clock Definitions

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
JTG_TDI	C16	PC_05	E01	PF_04	E18	VDD_DMC	U09
JTG_TDO	B14	PC_06	D01	PF_05	A19	VDD_DMC	U10
JTG_TMS	B15	PC_07	J02	PF_06	B18	VDD_DMC	U11
$\overline{\text{JTG\_TRST}}$	B10	PC_08	D02	PF_07	B20	VDD_DMC	U12
MLB0_CLKN	A06	PC_09	H02	PF_08	C19	VDD_DMC	U13
MLB0_CLKP	A07	PC_10	J03	PF_09	F18	VDD_DMC	U14
MLB0_DATN	B07	PC_11	C01	PF_10	D18	VDD_EXT	E07
MLB0_DATP	B08	PC_12	B01	PF_11	C20	VDD_EXT	E08
MLB0_SIGN	A08	PC_13	C02	SYS_BMODE0	Y18	VDD_EXT	E09
MLB0_SIGP	B09	PC_14	G02	SYS_BMODE1	W18	VDD_EXT	E10
PA_00	V12	PC_15	H03	SYS_BMODE2	Y19	VDD_EXT	E11
PA_01	V11	PD_00	W07	SYS_CLKIN0	A11	VDD_EXT	E12
PA_02	V10	PD_01	V06	SYS_CLKIN1	A14	VDD_EXT	E17
PA_03	V09	PD_02	W06	SYS_CLKOUT	D11	VDD_EXT	G04
PA_04	W10	PD_03	V04	SYS_FAULT	V14	VDD_EXT	H04
PA_05	V08	PD_04	V05	$\overline{\text{SYS\_FAULT}}$	W15	VDD_EXT	H17
PA_06	W09	PD_05	T01	$\overline{\text{SYS\_HWRST}}$	C11	VDD_EXT	J04
PA_07	W08	PD_06	R01	$\overline{\text{SYS\_RESOUT}}$	V13	VDD_EXT	J17
PA_08	V07	PD_07	R02	SYS_XTAL0	A10	VDD_EXT	K04
PA_09	A03	PD_08	R03	SYS_XTAL1	A13	VDD_EXT	K17
PA_10	A02	PD_09	M03	TWI0_SCL	T03	VDD_EXT	L04
PA_11	A04	PD_10	L02	TWI0_SDA	T02	VDD_EXT	L17
PA_12	C04	PD_11	L01	TWI1_SCL	U05	VDD_EXT	M04
PA_13	B03	PD_12	L03	TWI1_SDA	U03	VDD_EXT	M17
PA_14	C05	PD_13	K02	TWI2_SCL	W01	VDD_EXT	N17
PA_15	B04	PD_14	K01	TWI2_SDA	V01	VDD_EXT	T04
PB_00	E06	PD_15	K03	USB0_DM	A17	VDD_EXT	U06
PB_01	B05	PE_00	J01	USB0_DP	A16	VDD_HADC	R20
PB_02	C07	PE_01	H01	USB0_ID	C12	VDD_INT	F05
PB_03	C06	PE_02	E04	USB0_VBC	D13	VDD_INT	F07
PB_04	B06	PE_03	E03	USB0_VBUS	B11	VDD_INT	F08
PB_05	C10	PE_04	D03	USB0_CLKIN	C13	VDD_INT	F09
PB_06	C09	PE_05	E02	USB0_XTAL	B12	VDD_INT	F10
PB_07	D09	PE_06	F04	VDD_DMC	N04	VDD_INT	F11
PB_08	D08	PE_07	A05	VDD_DMC	T06	VDD_INT	F12
PB_09	D10	PE_08	D05	VDD_DMC	T07	VDD_INT	F13
PB_10	B13	PE_09	D07	VDD_DMC	T08	VDD_INT	F14
PB_11	D12	PE_10	C08	VDD_DMC	T09	VDD_INT	F16
PB_12	C14	PE_11	D06	VDD_DMC	T10	VDD_INT	G05
PB_13	C15	PE_12	D16	VDD_DMC	T11	VDD_INT	G16
PB_14	D14	PE_13	D15	VDD_DMC	T12	VDD_INT	H05
PB_15	G17	PE_14	C17	VDD_DMC	T13	VDD_INT	H16
PC_00	G01	PE_15	E15	VDD_DMC	T14	VDD_INT	J05
PC_01	G03	PF_00	B16	VDD_DMC	T15	VDD_INT	J16
PC_02	F01	PF_01	B17	VDD_DMC	T17	VDD_INT	K05
PC_03	F02	PF_02	F17	VDD_DMC	U07	VDD_INT	K16
PC_04	F03	PF_03	A18	VDD_DMC	U08	VDD_INT	L05

Pin Name	Ball No.
VDD_INT	L16
VDD_INT	M05
VDD_INT	M16
VDD_INT	N05
VDD_INT	N16
VDD_INT	P05
VDD_INT	P06
VDD_INT	P08
VDD_INT	P09
VDD_INT	P10
VDD_INT	P11
VDD_INT	P12
VDD_INT	P13
VDD_INT	P15
VDD_INT	P16
VDD_INT	R04
VDD_INT	R05
VDD_INT	R07
VDD_INT	R08
VDD_INT	R09
VDD_INT	R10
VDD_INT	R11
VDD_INT	R12
VDD_INT	R13
VDD_INT	R14
VDD_INT	R16
VDD_INT	R17
VDD_USB	E13

ADSP-SC57X/ADSP-2157X 176-LEAD LQFP LEAD ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.	Pin Name	Lead No.
DAI0_PIN01	123	PA_01	79	PC_15	12	VDD_EXT	149
DAI0_PIN02	127	PA_02	77	PD_00	67	VDD_EXT	152
DAI0_PIN03	121	PA_03	76	PD_01	64	VDD_EXT	158
DAI0_PIN04	122	PA_04	75	PD_02	63	VDD_EXT	160
DAI0_PIN05	120	PA_05	74	PD_03	62	VDD_EXT	164
DAI0_PIN06	118	PA_06	70	PD_04	61	VDD_EXT	167
DAI0_PIN07	119	PA_07	69	PD_05	51	VDD_EXT	171
DAI0_PIN08	117	PA_08	68	PD_06	50	VDD_HADC	90
DAI0_PIN09	116	PA_09	13	PD_07	49	VDD_INT	01
DAI0_PIN10	113	PA_10	10	PD_08	48	VDD_INT	03
DAI0_PIN11	112	PA_11	11	PD_09	43	VDD_INT	07
DAI0_PIN12	111	PA_12	08	PD_10	42	VDD_INT	14
DAI0_PIN13	110	PA_13	06	PD_11	41	VDD_INT	16
DAI0_PIN14	108	PA_14	05	PD_12	40	VDD_INT	30
DAI0_PIN15	107	PA_15	04	PD_13	37	VDD_INT	39
DAI0_PIN16	106	PB_00	174	PD_14	36	VDD_INT	47
DAI0_PIN17	105	PB_01	173	PD_15	35	VDD_INT	52
DAI0_PIN18	102	PB_02	172	SYS_BMODE0	86	VDD_INT	59
DAI0_PIN19	101	PB_03	169	SYS_BMODE1	87	VDD_INT	66
DAI0_PIN20	100	PB_04	168	SYS_CLKIN0	154	VDD_INT	72
GND	02	PB_05	166	SYS_CLKOUT	157	VDD_INT	73
GND	15	PB_06	165	$\overline{\text{SYS\_FAULT}}$	85	VDD_INT	82
GND	44	PB_07	162	$\overline{\text{SYS\_HWRST}}$	151	VDD_INT	88
GND	45	PB_08	161	$\overline{\text{SYS\_RESOUT}}$	81	VDD_INT	98
GND	65	PB_09	159	SYS_XTAL0	155	VDD_INT	103
GND	83	PB_10	148	TWI0_SCL	54	VDD_INT	109
GND	89	PB_11	146	TWI0_SDA	53	VDD_INT	114
GND	97	PB_12	144	TWI1_SCL	56	VDD_INT	124
GND	99	PB_13	142	TWI1_SDA	55	VDD_INT	129
GND	125	PB_14	141	TWI2_SCL	58	VDD_INT	130
GND	131	PB_15	128	TWI2_SDA	57	VDD_INT	132
GND	133	PC_00	34	VDD_EXT	09	VDD_INT	134
GND	176	PC_01	33	VDD_EXT	21	VDD_INT	139
GND	177[1]	PC_02	32	VDD_EXT	31	VDD_INT	145
HADC0_VIN0	91	PC_03	29	VDD_EXT	38	VDD_INT	150
HADC0_VIN1	92	PC_04	28	VDD_EXT	46	VDD_INT	156
HADC0_VIN2	94	PC_05	27	VDD_EXT	60	VDD_INT	163
HADC0_VIN3	95	PC_06	26	VDD_EXT	71	VDD_INT	170
HADC0_VREFN	93	PC_07	25	VDD_EXT	78	VDD_INT	175
HADC0_VREFP	96	PC_08	24	VDD_EXT	84		
JTG_TCK	135	PC_09	23	VDD_EXT	104		
JTG_TDI	137	PC_10	22	VDD_EXT	115		
JTG_TDO	136	PC_11	20	VDD_EXT	126		
JTG_TMS	138	PC_12	19	VDD_EXT	140		
$\overline{\text{JTG\_TRST}}$	153	PC_13	18	VDD_EXT	143		
PA_00	80	PC_14	17	VDD_EXT	147		

[1] Pin 177 is the GND supply (see Figure 91) for the processor; this pad must connect to GND.

CONFIGURATION OF THE 176-LEAD LQFP LEAD CONFIGURATION

Figure 90 shows the top view of the 176-lead LQFP lead configuration and Figure 91 shows the bottom view of the 176-lead LQFP lead configuration.

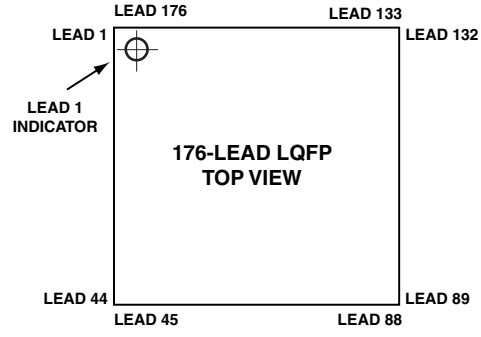

Figure 90. 176-Lead LQFP Lead Configuration (Top View)

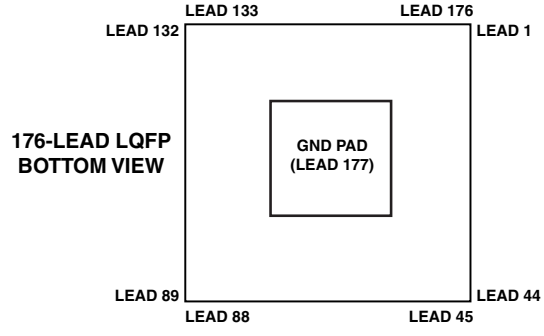

Figure 91. 176-Lead LQFP Lead Configuration (Bottom View)

AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 99 are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 99. Automotive Products

Model [1, 2, 3]	Processor Instruction Rate (Max)	ARM Instruction Rate (Max)[4]	Temperature Range[5]	ARM Cores[4]	SHARC+ Cores	External Memory Ports	Package Description	Package Option
AD21571WCSWZ4xx	450 MHz	N/A	–40°C to +105°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
AD21571WCSWZ5xx	500 MHz	N/A	–40°C to +105°C	N/A	2	0	176-Lead LQFP_EP	SW-176-5
AD21573WCBCZ4xx	450 MHz	N/A	–40°C to +105°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
AD21573WCBCZ5xx	500 MHz	N/A	–40°C to +105°C	N/A	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC570WCSWZ42xx	450 MHz	225 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSC570WCSWZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	1	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ3xx	300 MHz	300 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC571WCSWZ5xx	500 MHz	500 MHz	–40°C to +105°C	1	2	0	176-Lead LQFP_EP	SW-176-5
ADSC572WCBCZ42xx	450 MHz	225 MHz	–40°C to +105°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC572WCBCZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	1	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ3xx	300 MHz	300 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ4xx	450 MHz	450 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2
ADSC573WCBCZ5xx	500 MHz	500 MHz	–40°C to +105°C	1	2	1	Pad 400-Ball CSP_BGA	BC-400-2

[1] Z = RoHS Compliant Part.
[2] xx denotes the current die revision.
[3] For evaluation of all models, order the ADZS-SC573-EZLITE evaluation board.
[4] N/A means not applicable.
[5] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see the Operating Conditions section for the junction temperature (T_J) specification which is the only temperature specification.