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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	100
Number of Logic Elements/Cells	238
Total RAM Bits	3200
Number of I/O	61
Number of Gates	5000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs05xl-4pc84c

General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in Figure 1. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.

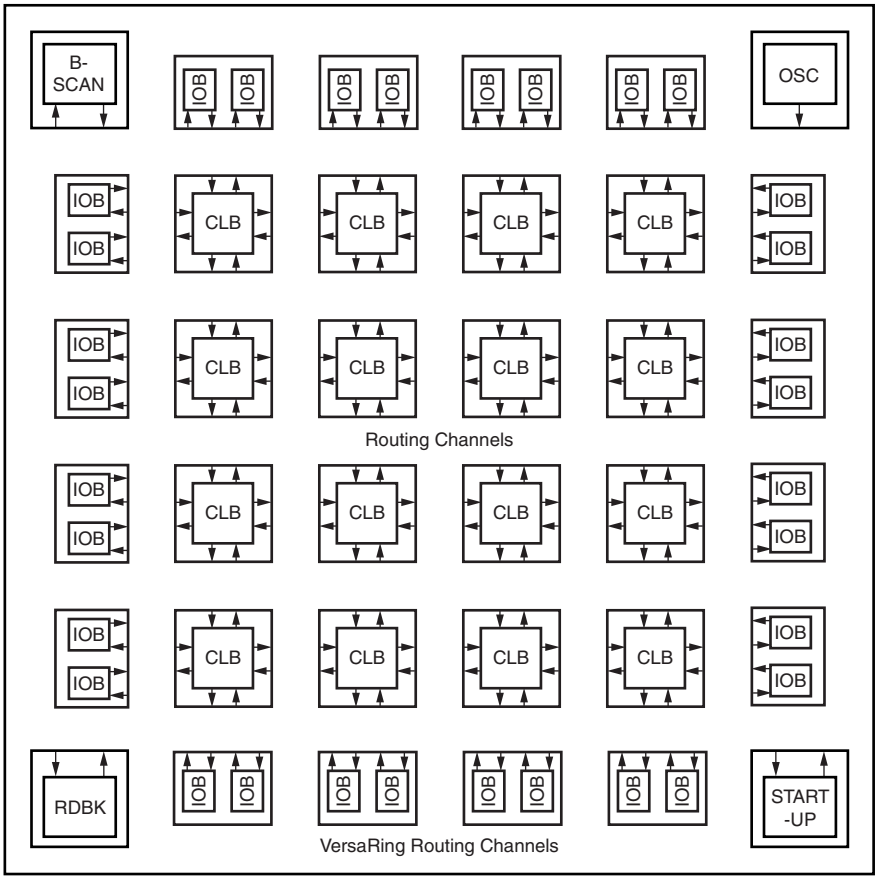


Figure 1: **Basic FPGA Block Diagram**

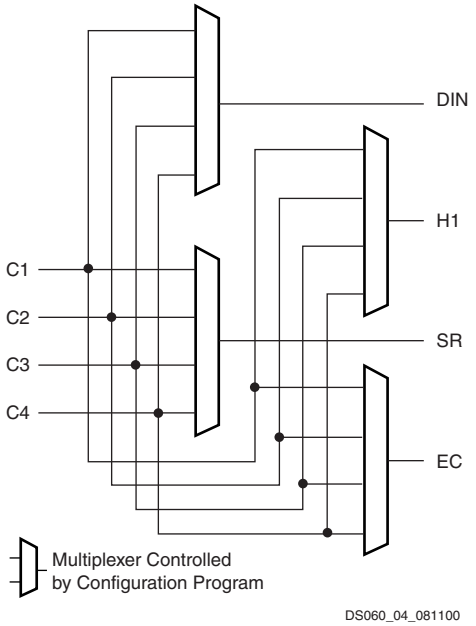


Figure 4: **CLB Control Signal Interface**

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

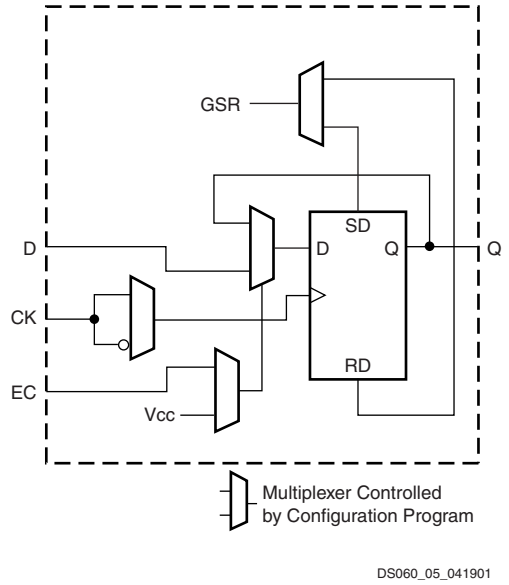


Figure 5: **IOB Flip-Flop/Latch Functional Block Diagram**

IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: **Input Register Functionality**

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	⌐	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care.
⌐	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds, using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.

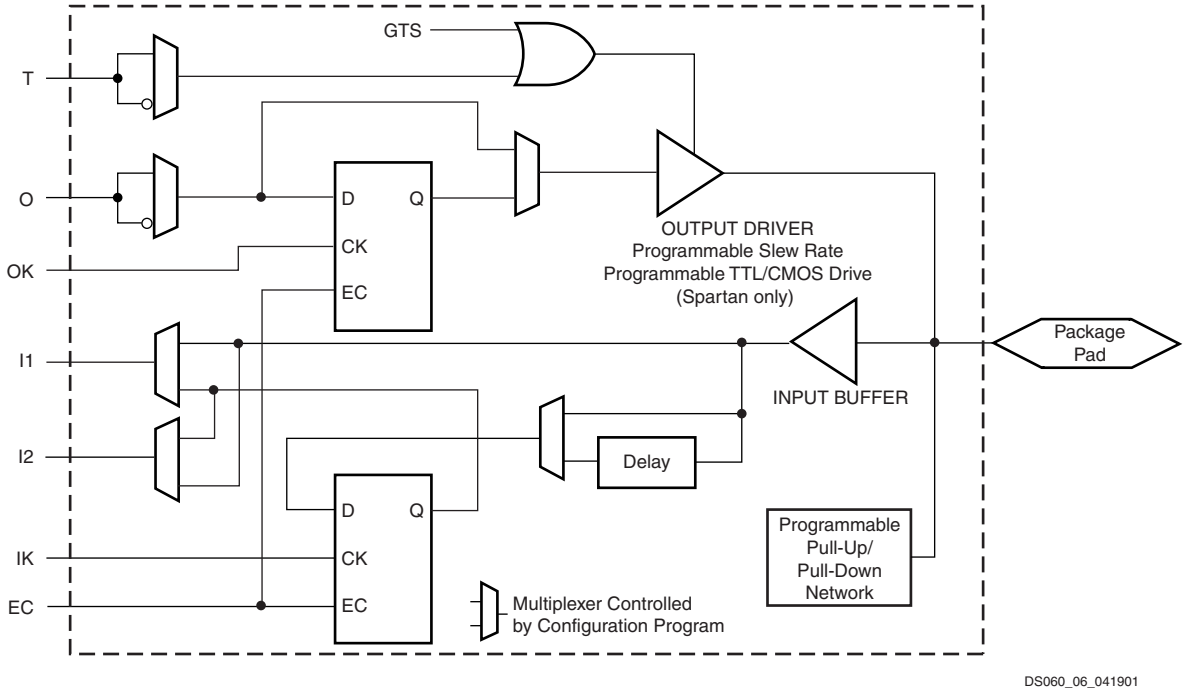


Figure 6: **Simplified Spartan/XL IOB Block Diagram**

Table 4: **Supported Sources for Spartan/XL Inputs**

Source	Spartan Inputs		Spartan-XL Inputs
	5V, TTL	5V, CMOS	3.3V CMOS
Any device, V_{CC} = 3.3V, CMOS outputs	√	Unreliable Data	√
Spartan family, V_{CC} = 5V, TTL outputs	√		√
Any device, V_{CC} = 5V, TTL outputs ($V_{OH} \leq 3.7V$)	√		√
Any device, V_{CC} = 5V, CMOS outputs	√	√	√ (default mode)

Spartan-XL Family V_{CC} Clamping

Spartan-XL FPGAs have an optional clamping diode connected from each I/O to V_{CC}. When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. V_{CC} clamping is a global option affecting all I/O pins.

Spartan-XL devices are fully 5V TTL I/O compatible if V_{CC} clamping is not enabled. With V_{CC} clamping enabled, the Spartan-XL devices will begin to clamp input voltages to one diode voltage drop above V_{CC}. If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

Spartan-XL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 5.

Table 5: **I/O Standards Supported by Spartan-XL FPGAs**

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}
LVCMOS 3V	OK	12/24 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}

Additional Fast Capture Input Latch (Spartan-XL Family Only)

The Spartan-XL family OB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active High input flip-flop. ILFLX is a transparent Low Fast Capture latch followed by a transparent High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 6.

Table 6: **Output Flip-Flop Functionality**

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	⌐	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
⌐	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

CLB signals from which they are originally derived are shown in Table 10.

Table 10: **Dual-Port RAM Signals**

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F_{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G_{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: *"Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM,"* and *"Synchronous and Asynchronous FIFO Designs."* All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan

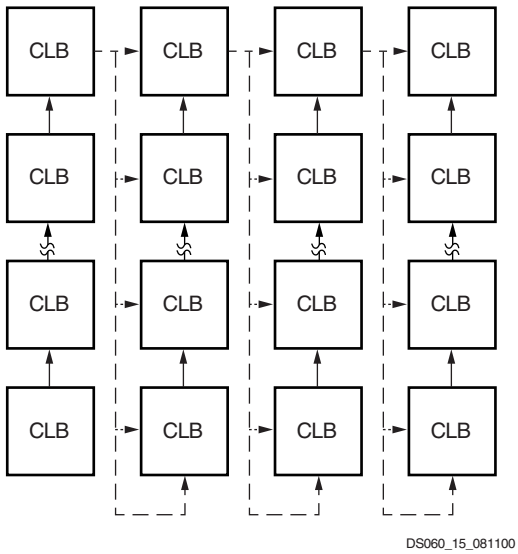


Figure 15: **Available Spartan/XL Carry Propagation Paths**

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. $\overline{\text{PROGRAM}}$, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.

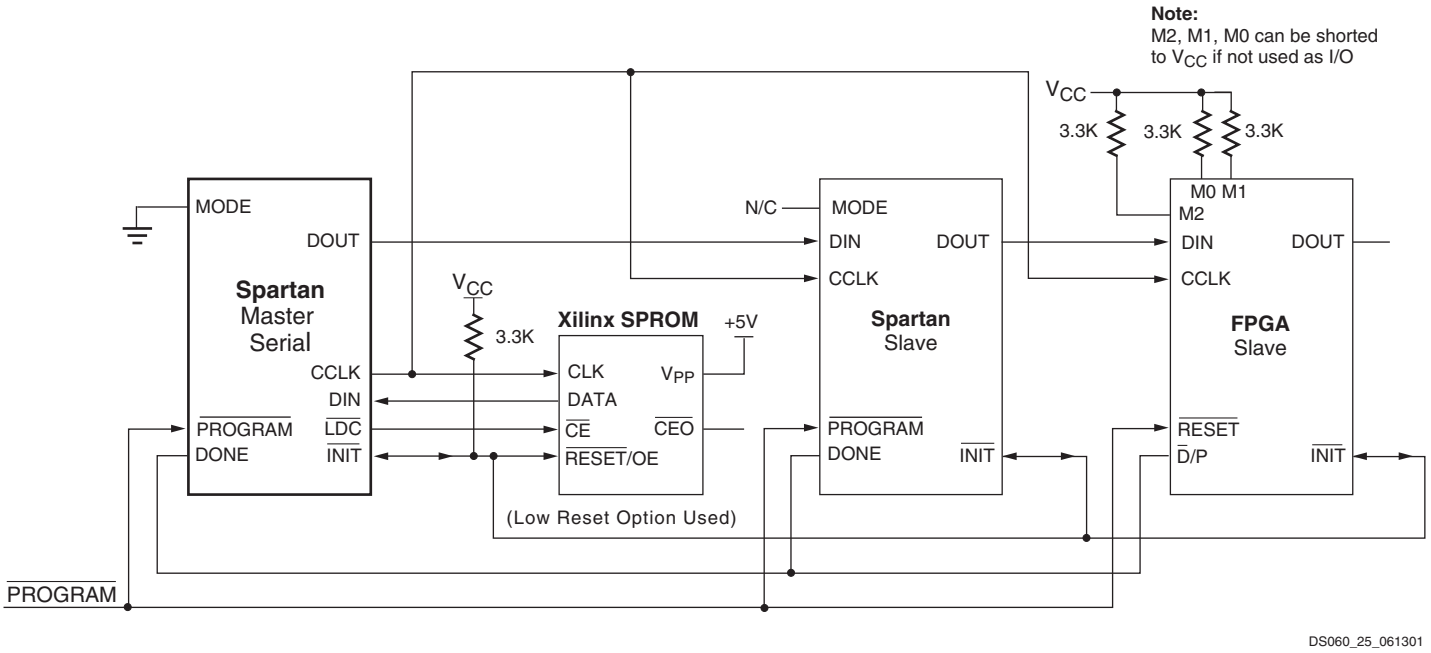


Figure 25: **Master/Slave Serial Mode Circuit Diagram**

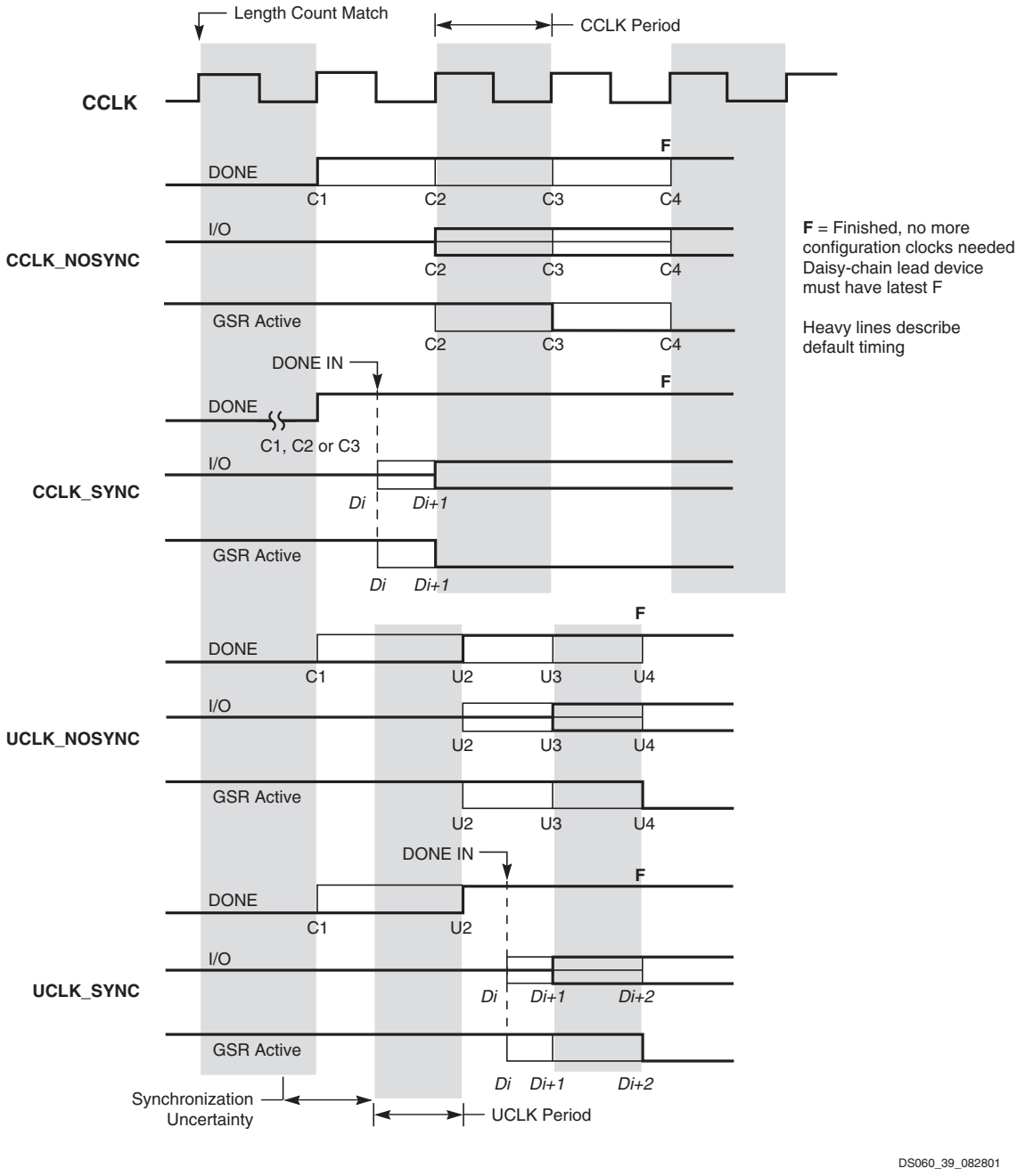


Figure 31: **Start-up Timing**

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input.
- Wait for $\overline{\text{INIT}}$ to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after $\overline{\text{INIT}}$ goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and Spartan-XL devices.

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 16 and Table 17.

Spartan Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan Family Absolute Maximum Ratings(1)

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND(2,3)		–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output(2,3)		–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot (above V_{CC}) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = –40°C to +100°C(1)	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage(2)	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage(2)	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size[1]	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T_{WCTS}		32x1	8.0	-	11.6	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T_{WPTS}		32x1	4.0	-	5.8	-	ns
T_{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T_{ASTS}		32x1	1.5	-	2.0	-	ns
T_{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{AHTS}		32x1	0.0	-	0.0	-	ns
T_{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T_{DSTS}		32x1	1.5	-	1.7	-	ns
T_{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{DHTS}		32x1	0.0	-	0.0	-	ns
T_{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T_{WSTS}		32x1	1.5	-	1.6	-	ns
T_{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{WHTS}		32x1	0.0	-	0.0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T_{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T_{RCT}		32x1	3.8	-	3.8	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T_{IHO}		32x1	-	2.0	-	2.7	ns
T_{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T_{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:
1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Min	Min	
Input Setup/Hold Times Using Primary Clock and IFF					
T_{PSUF}/T_{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T_{PSU}/T_{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T_{SSUF}/T_{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T_{SSU}/T_{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:

1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Typ.	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min (LVTTL)		2.4	-	-	V
	High-level output voltage @ I_{OH} = –500 µA, (LVCMOS)		90% V_{CC}	-	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (LVTTL)(1)		-	-	0.4	V
	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL)(2)		-	-	0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)		-	-	10% V_{CC}	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		2.5	-	-	V
I_{CCO}	Quiescent FPGA supply current(3,4)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I_{CCPD}	Power Down FPGA supply current(3,5)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I_L	Input or output leakage current		–10	-	10	µA
C_{IN}	Input capacitance (sample tested)		-	-	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V (sample tested)		0.02	-	-	mA

Notes:
1. With up to 64 pins simultaneously sinking 12 mA (default mode).
2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
4. With no output current loads, no active input resistors, and all package pins at V_{CC} or GND.
5. With $\overline{PWRDWN}$ active.

Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CC} lines for a successful power on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Max	Units
I_{CCPO}	Total V_{CC} supply current required during power-on	100	-	mA
T_{CCPO}	V_{CC} ramp time(2,3)	-	50	ms

Notes:
1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CC} ramps from 0 to 3.3V.
2. The ramp time is measured from GND to V_{CC} max on a fully loaded board.
3. V_{CC} must not dip in the negative direction during power on.

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

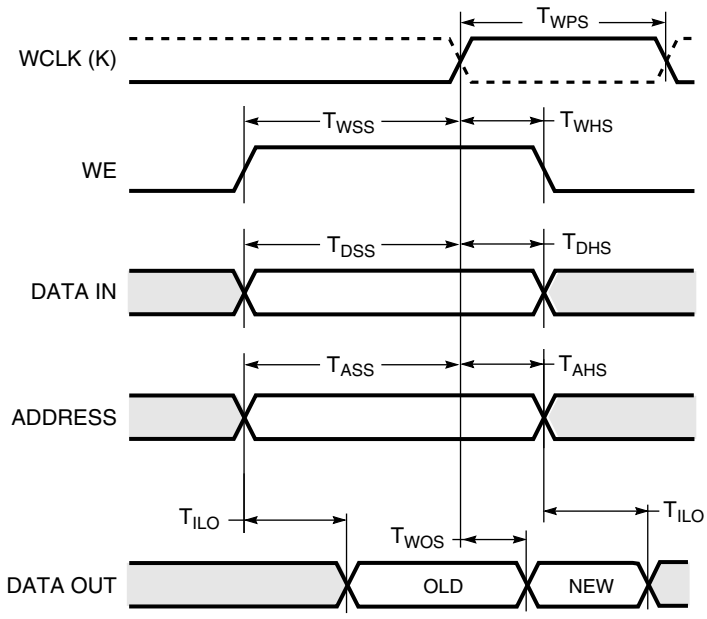
All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation(1)							
T_{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T_{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

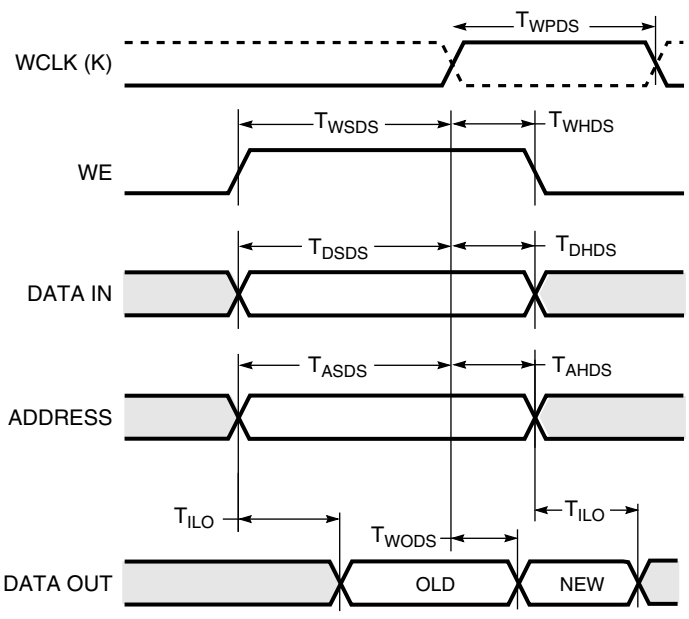
Notes:
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



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Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Setup Times							
T_{ECIK}	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T_{PICK}	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T_{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T_{PID}	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T_{Delay}	$T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T_{RRI}	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	P18	P28	P44	P52	V1	T1	272
I/O	P19	P29	P45	P53	T4	T2	275
I/O	-	P30	P46	P54	U3	T3	278
I/O	-	P31	P47	P55	V2	U1	281
I/O	P20	P32	P48	P56	W1	V1	284
I/O, SGCK2[1], GCK2[2]	P21	P33	P49	P57	V3	U2	287
Not Connected[1], M1[2]	P22	P34	P50	P58	W2	V2	290
GND	P23	P35	P51	P59	GND[4]	GND[4]	-
MODE[1], M0[2]	P24	P36	P52	P60	Y1	W1	293
VCC	P25	P37	P53	P61	VCC[4]	U3	-
Not Connected [1], $\overline{\text{PWRDWN}}$[2]	P26	P38	P54	P62	W3	V3	294 [1]
I/O, PGCK2[1], GCK3[2]	P27	P39	P55	P63	Y2	W2	295 [3]
I/O (HDC)	P28	P40	P56	P64	W4	W3	298 [3]
I/O	-	P41	P57	P65	V4	T4	301 [3]
I/O	-	P42	P58	P66	U5	U4	304 [3]
I/O	P29	P43	P59	P67	Y3	V4	307 [3]
I/O ($\overline{\text{LDC}}$)	P30	P44	P60	P68	Y4	W4	310 [3]
I/O	-	-	P61	P69	V5	T5	313 [3]
I/O	-	-	P62	P70	W5	W5	316 [3]
I/O	-	-	P63	P71	Y5	R6	319 [3]
I/O	-	-	P64	P72	V6	U6	322 [3]
I/O	-	-	P65	P73	W6	V6	325 [3]
I/O	-	-	-	P74	Y6	T6	328 [3]
GND	-	P45	P66	P75	GND[4]	GND[4]	-
I/O	-	P46	P67	P76	W7	W6	331 [3]
I/O	-	P47	P68	P77	Y7	U7	334 [3]
I/O	P31	P48	P69	P78	V8	V7	337 [3]
I/O	P32	P49	P70	P79	W8	W7	340 [3]
VCC	-	-	P71	P80	VCC[4]	T7	-
I/O	-	-	P72	P81	Y8	W8	343 [3]
I/O	-	-	P73	P82	U9	U8	346 [3]
I/O	-	-	-	P84	Y9	W9	349 [3]
I/O	-	-	-	P85	W10	V9	352 [3]
I/O	P33	P50	P74	P86	V10	U9	355 [3]
I/O	P34	P51	P75	P87	Y10	T9	358 [3]
I/O	P35	P52	P76	P88	Y11	W10	361 [3]
I/O ($\overline{\text{INIT}}$)	P36	P53	P77	P89	W11	V10	364 [3]
VCC	P37	P54	P78	P90	VCC[4]	U10	-
GND	P38	P55	P79	P91	GND[4]	GND[4]	-
I/O	P39	P56	P80	P92	V11	T10	367 [3]
I/O	P40	P57	P81	P93	U11	R10	370 [3]
I/O	P41	P58	P82	P94	Y12	W11	373 [3]
I/O	P42	P59	P83	P95	W12	V11	376 [3]
I/O	-	-	P84	P96	V12	U11	379 [3]

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	-	P85	P97	U12	T11	382 [3]
I/O	-	-	-	P99	V13	U12	385 [3]
I/O	-	-	-	P100	Y14	T12	388 [3]
VCC	-	-	P86	P101	VCC[4]	W13	-
I/O	P43	P60	P87	P102	Y15	V13	391 [3]
I/O	P44	P61	P88	P103	V14	U13	394 [3]
I/O	-	P62	P89	P104	W15	T13	397 [3]
I/O	-	P63	P90	P105	Y16	W14	400 [3]
GND	-	P64	P91	P106	GND[4]	GND[4]	-
I/O	-	-	-	P107	V15	V14	403 [3]
I/O	-	-	P92	P108	W16	U14	406 [3]
I/O	-	-	P93	P109	Y17	T14	409 [3]
I/O	-	-	P94	P110	V16	R14	412 [3]
I/O	-	-	P95	P111	W17	W15	415 [3]
I/O	-	-	P96	P112	Y18	U15	418 [3]
I/O	P45	P65	P97	P113	U16	V16	421 [3]
I/O	P46	P66	P98	P114	V17	U16	424 [3]
I/O	-	P67	P99	P115	W18	W17	427 [3]
I/O	-	P68	P100	P116	Y19	W18	430 [3]
I/O	P47	P69	P101	P117	V18	V17	433 [3]
I/O, SGCK3[1], GCK4[2]	P48	P70	P102	P118	W19	V18	436 [3]
GND	P49	P71	P103	P119	GND[4]	GND[4]	-
DONE	P50	P72	P104	P120	Y20	W19	-
VCC	P51	P73	P105	P121	VCC[4]	U17	-
$\overline{\text{PROGRAM}}$	P52	P74	P106	P122	V19	U18	-
I/O (D7[2])	P53	P75	P107	P123	U19	V19	439 [3]
I/O, PGCK3[1], GCK5[2]	P54	P76	P108	P124	U18	U19	442 [3]
I/O	-	P77	P109	P125	T17	T16	445 [3]
I/O	-	P78	P110	P126	V20	T17	448 [3]
I/O	-	-	-	P127	U20	T18	451 [3]
I/O	-	-	P111	P128	T18	T19	454 [3]
I/O (D6[2])	P55	P79	P112	P129	T19	R16	457 [3]
I/O	P56	P80	P113	P130	T20	R19	460 [3]
I/O	-	-	P114	P131	R18	P15	463 [3]
I/O	-	-	P115	P132	R19	P17	466 [3]
I/O	-	-	P116	P133	R20	P18	469 [3]
I/O	-	-	P117	P134	P18	P16	472 [3]
GND	-	P81	P118	P135	GND[4]	GND[4]	-
I/O	-	-	-	P136	P20	P19	475 [3]
I/O	-	-	-	P137	N18	N17	478 [3]
I/O	-	P82	P119	P138	N19	N18	481 [3]
I/O	-	P83	P120	P139	N20	N19	484 [3]
VCC	-	-	P121	P140	VCC[4]	N16	-
I/O (D5[2])	P57	P84	P122	P141	M17	M19	487 [3]
I/O	P58	P85	P123	P142	M18	M17	490 [3]

CS280

VCC Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-
Not Connected Pins					
A4	A12	C8	C12	C15	D1
D2	D5	D8	D17	D18	E15
H2	H3	H18	H19	L4	M1
M16	M18	R2	R4	R5	R15
R17	T8	T15	U5	V8	V12
W12	W16	-	-	-	-
Not Connected Pins (VCC in XCS40XL)					
B5	B15	E3	E18	R3	R18
V5	V15	-	-	-	-

5/21/02

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
VCC	P183	P212	VCC(4)	VCC(4)	-
I/O	P184	P213	C10	D10	86
I/O	P185	P214	D10	E10	89
I/O	P186	P215	A9	A9	92
I/O	P187	P216	B9	B9	95
I/O	P188	P217	C9	C9	98
I/O	P189	P218	D9	D9	101
I/O	P190	P220	A8	A8	104
I/O	P191	P221	B8	B8	107
I/O	-	-	C8	C8	110
I/O	-	-	A7	D8	113
VCC	P192	P222	VCC(4)	VCC(4)	-
I/O	-	P223	A6	B7	116
I/O	-	P224	C7	C7	119
I/O	P193	P225	B6	D7	122
I/O	P194	P226	A5	A6	125
GND	P195	P227	GND(4)	GND(4)	-
I/O	P196	P228	C6	B6	128
I/O	P197	P229	B5	C6	131
I/O	P198	P230	A4	D6	134
I/O	P199	P231	C5	E6	137

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	P200	P232	B4	A5	140
I/O	P201	P233	A3	C5	143
I/O	-	-	-	D5	146
I/O	-	-	-	A4	149
I/O	P202	P234	D5	B4	152
I/O	P203	P235	C4	C4	155
I/O	P204	P236	B3	A3	158
I/O	P205	P237	B2	A2	161
I/O	P206	P238	A2	B3	164
I/O, SGCK1(1), GCK8(2)	P207	P239	C3	B2	167
VCC	P208	P240	VCC(4)	VCC(4)	-
GND	P1	P1	GND(4)	GND(4)	-
I/O, PGCK1(1), GCK1(2)	P2	P2	B1	C3	170
I/O	P3	P3	C2	C2	173
I/O	P4	P4	D2	B1	176
I/O	P5	P5	D3	C1	179
I/O, TDI	P6	P6	E4	D4	182
I/O, TCK	P7	P7	C1	D3	185
I/O	-	-	-	D2	188
I/O	-	-	-	D1	191
I/O	P8	P8	D1	E2	194
I/O	P9	P9	E3	E4	197
I/O	P10	P10	E2	E1	200
I/O	P11	P11	E1	F5	203
I/O	P12	P12	F3	F3	206
I/O	-	P13	F2	F2	209
GND	P13	P14	GND(4)	GND(4)	-
I/O	P14	P15	G3	F4	212
I/O	P15	P16	G2	F1	215
I/O, TMS	P16	P17	G1	G3	218
I/O	P17	P18	H3	G2	221
VCC	P18	P19	VCC(4)	VCC(4)	-
I/O	-	P20	H2	G4	224
I/O	-	P21	H1	H1	227
I/O	-	-	J4	H3	230
I/O	-	-	J3	H2	233
I/O	P19	P23	J2	H4	236
I/O	P20	P24	J1	J1	239
I/O	P21	P25	K2	J2	242
I/O	P22	P26	K3	J3	245
I/O	P23	P27	K1	J4	248
I/O	P24	P28	L1	K1	251

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	P90	P105	Y16	W14	466 (3)
GND	P91	P106	GND(4)	GND(4)	-
I/O	-	P107	V15	V14	469 (3)
I/O	P92	P108	W16	U14	472 (3)
I/O	P93	P109	Y17	T14	475 (3)
I/O	P94	P110	V16	R14	478 (3)
I/O	P95	P111	W17	W15	481 (3)
I/O	P96	P112	Y18	U15	484 (3)
I/O	-	-	-	T15	487 (3)
I/O	-	-	-	W16	490 (3)
I/O	P97	P113	U16	V16	493 (3)
I/O	P98	P114	V17	U16	496 (3)
I/O	P99	P115	W18	W17	499 (3)
I/O	P100	P116	Y19	W18	502 (3)
I/O	P101	P117	V18	V17	505 (3)
I/O, SGCK3(1), GCK4(2)	P102	P118	W19	V18	508 (3)
GND	P103	P119	GND(4)	GND(4)	-
DONE	P104	P120	Y20	W19	-
VCC	P105	P121	VCC(4)	VCC(4)	-
$\overline{\text{PROGRAM}}$	P106	P122	V19	U18	-
I/O (D7(2))	P107	P123	U19	V19	511 (3)
I/O, PGCK3(1), GCK5(2)	P108	P124	U18	U19	514 (3)
I/O	P109	P125	T17	T16	517 (3)
I/O	P110	P126	V20	T17	520 (3)
I/O	-	P127	U20	T18	523 (3)
I/O	P111	P128	T18	T19	526 (3)
I/O	-	-	-	R15	529 (3)
I/O	-	-	-	R17	523 (3)
I/O (D6(2))	P112	P129	T19	R16	535 (3)
I/O	P113	P130	T20	R19	538 (3)
I/O	P114	P131	R18	P15	541 (3)
I/O	P115	P132	R19	P17	544 (3)
I/O	P116	P133	R20	P18	547 (3)
I/O	P117	P134	P18	P16	550 (3)
GND	P118	P135	GND(4)	GND(4)	-
I/O	-	P136	P20	P19	553 (3)
I/O	-	P137	N18	N17	556 (3)
I/O	P119	P138	N19	N18	559 (3)
I/O	P120	P139	N20	N19	562 (3)
VCC	P121	P140	VCC(4)	VCC(4)	-
I/O (D5(2))	P122	P141	M17	M19	565 (3)
I/O	P123	P142	M18	M17	568 (3)

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	-	-	-	M18	571 (3)
I/O	-	-	M19	M16	574 (3)
I/O	P124	P144	M20	L19	577 (3)
I/O	P125	P145	L19	L18	580 (3)
I/O	P126	P146	L18	L17	583 (3)
I/O	P127	P147	L20	L16	586 (3)
I/O (D4(2))	P128	P148	K20	K19	589 (3)
I/O	P129	P149	K19	K18	592 (3)
VCC	P130	P150	VCC(4)	VCC(4)	-
GND	P131	P151	GND(4)	GND(4)	-
I/O (D3(2))	P132	P152	K18	K16	595 (3)
I/O	P133	P153	K17	K15	598 (3)
I/O	P134	P154	J20	J19	601 (3)
I/O	P135	P155	J19	J18	604 (3)
I/O	P136	P156	J18	J17	607 (3)
I/O	P137	P157	J17	J16	610 (3)
I/O	-	-	H20	H19	613 (3)
I/O	-	-	-	H18	616 (3)
I/O (D2(2))	P138	P159	H19	H17	619 (3)
I/O	P139	P160	H18	H16	622 (3)
VCC	P140	P161	VCC(4)	VCC(4)	-
I/O	P141	P162	G19	G18	625 (3)
I/O	P142	P163	F20	G17	628 (3)
I/O	-	P164	G18	G16	631 (3)
I/O	-	P165	F19	F19	634 (3)
GND	P143	P166	GND(4)	GND(4)	-
I/O	-	P167	F18	F18	637 (3)
I/O	P144	P168	E19	F17	640 (3)
I/O	P145	P169	D20	F16	643 (3)
I/O	P146	P170	E18	F15	646 (3)
I/O	P147	P171	D19	E19	649 (3)
I/O	P148	P172	C20	E17	652 (3)
I/O (D1(2))	P149	P173	E17	E16	655 (3)
I/O	P150	P174	D18	D19	658 (3)
I/O	-	-	-	D18	661 (3)
I/O	-	-	-	D17	664 (3)
I/O	P151	P175	C19	C19	667 (3)
I/O	P152	P176	B20	B19	670 (3)
I/O (D0(2), DIN)	P153	P177	C18	C18	673 (3)
I/O, SGCK4(1), GCK6(2) (DOUT)	P154	P178	B19	B18	676 (3)
CCLK	P155	P179	A20	A19	-
VCC	P156	P180	VCC(4)	VCC(4)	-

Revision History

The following table shows the revision history for this document.

Date	Version	Description
11/20/98	1.3	Added Spartan-XL specs and Power Down.
01/06/99	1.4	All Spartan-XL -4 specs designated Preliminary with no changes.
03/02/00	1.5	Added CS package, updated Spartan-XL specs to Final.
09/19/01	1.6	Reformatted, updated power specs, clarified configuration information. Removed T_{SOL} soldering information from Absolute Maximum Ratings table. Changed Figure 26: Slave Serial Mode Characteristics: T_{CCH}, T_{CCL} from 45 to 40 ns. Changed Master Mode Configuration Switching Characteristics: T_{CCLK} min. from 80 to 100 ns. Added Total Dist. RAM Bits to Table 1; added **Start-Up**, page 36 characteristics.
06/27/02	1.7	Clarified Express Mode pseudo daisy chain. Added new Industrial options. Clarified XCS30XL CS280 V_{CC} pinout.
06/26/08	1.8	Noted that PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, are discontinued by **PDN2004-01**. Extended description of recommended maximum delay of reconfiguration in **Delaying Configuration After Power-Up**, page 35. Added reference to Pb-free package options and provided link to **Package Specifications**, page 81. Updated links.
03/01/13	2.0	The products listed in this data sheet are obsolete. See **XCN10016** and **XCN11010** for further information.