**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 100 |
| Number of Logic Elements/Cells | 238 |
| Total RAM Bits | 3200 |
| Number of I/O | 77 |
| Number of Gates | 5000 |
| Voltage - Supply | 3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcs05xl-4vqg100c |

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds, using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the $V_{CC}$ is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V $V_{CC}$ can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.

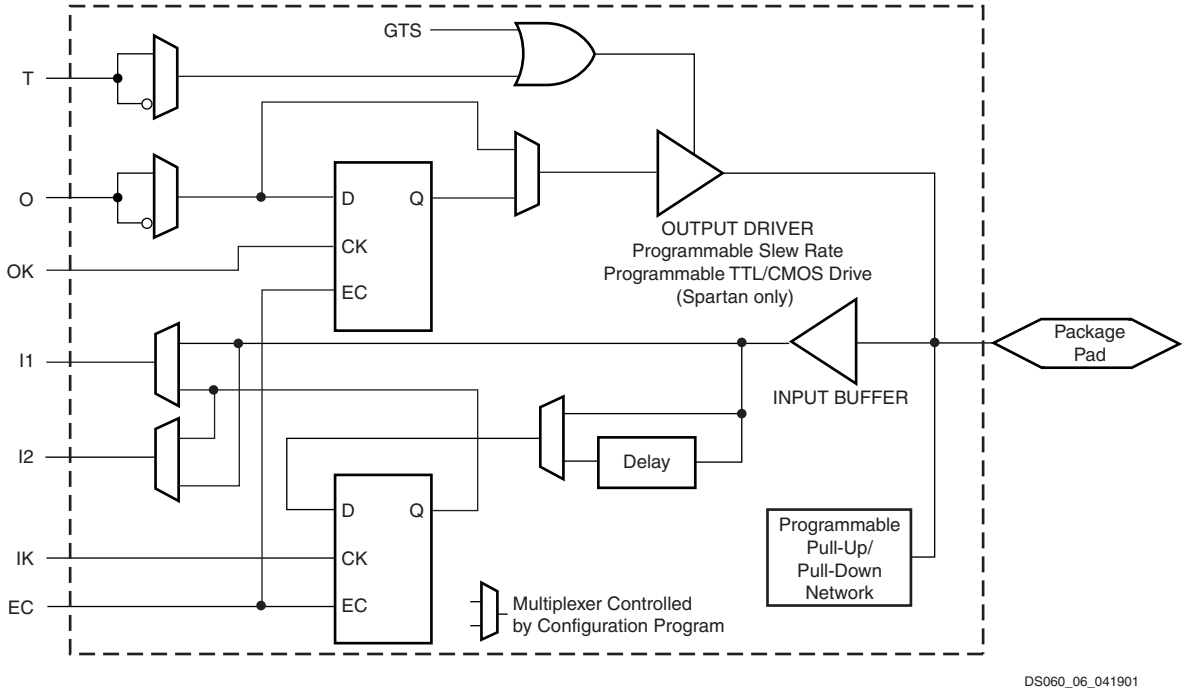



*Figure 6:* **Simplified Spartan/XL IOB Block Diagram**

- The 16 x 1 single-port configuration contains a RAM array with 16 locations, each one-bit wide. One 4-bit address decoder determines the RAM location for write and read operations. There is one input for writing data and one output for reading data, all at the selected address.
- The (16 x 1) x 2 single-port configuration combines two 16 x 1 single-port configurations (each according to the preceding description). There is one data input, one data output and one address decoder for each array. These arrays can be addressed independently.
- The 32 x 1 single-port configuration contains a RAM array with 32 locations, each one-bit wide. There is one data input, one data output, and one 5-bit address decoder.
- The dual-port mode 16 x 1 configuration contains a RAM array with 16 locations, each one-bit wide. There are two 4-bit address decoders, one for each port. One port consists of an input for writing and an output for reading, all at a selected address. The other port consists of one output for reading from an independently selected address.

The appropriate choice of RAM configuration mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Selection criteria include the following: Whereas the 32 x 1 single-port, the (16 x 1) x 2 single-port, and the 16 x 1 dual-port configurations each use one entire CLB, the 16 x 1 single-port configuration uses only one half of a CLB. Due to its simultaneous read/write capability, the dual-port RAM can transfer twice as much data as the single-port RAM, which permits only one data operation at any given time.

CLB memory configuration options are selected by using the appropriate library symbol in the design entry.

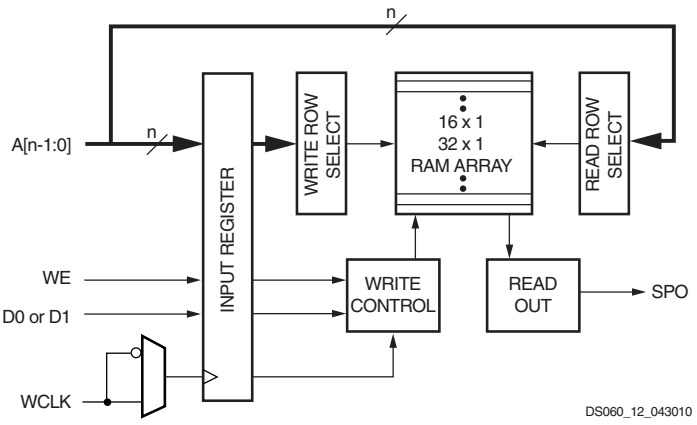
### Single-Port Mode

There are three CLB memory configurations for the single-port RAM: 16 x 1, (16 x 1) x 2, and 32 x 1, the functional organization of which is shown in Figure 12.

The single-port RAM signals and the CLB signals (Figure 2, page 4) from which they are originally derived are shown in Table 9.

*Table 9:* **Single-Port RAM Signals**

| RAM Signal | Function | CLB Signal |
|---|---|---|
| D0 or D1 | Data In | DIN or H1 |
| A[3:0] | Address | F[4:1] or G[4:1] |
| A4 (32 x 1 only) | Address | H1 |
| WE | Write Enable | SR |
| WCLK | Clock | K |
| SPO | Single Port Out (Data Out) | $F_{OUT}$ or $G_{OUT}$ |




**Notes:**
1. The (16 x 1) x 2 configuration combines two 16 x 1 single-port RAMs, each with its own independent address bus and data input. The same WE and WCLK signals are connected to both RAMs.
2. n = 4 for the 16 x 1 and (16 x 1) x 2 configurations. n = 5 for the 32 x 1 configuration.

*Figure 12:* **Logic Diagram for the Single-Port RAM**

Writing data to the single-port RAM is essentially the same as writing to a data register. It is an edge-triggered (synchronous) operation performed by applying an address to the A inputs and data to the D input during the active edge of WCLK while WE is High.

The timing relationships are shown in Figure 13. The High logic level on WE enables the input data register for writing. The active edge of WCLK latches the address, input data, and WE signals. Then, an internal write pulse is generated that loads the data into the memory cell.

CLB signals from which they are originally derived are shown in Table 10.

*Table 10:* **Dual-Port RAM Signals**

| RAM Signal | Function | CLB Signal |
|---|---|---|
| D | Data In | DIN |
| A[3:0] | Read Address for Single-Port.<br>Write Address for Single-Port and Dual-Port. | F[4:1] |
| DPRA[3:0] | Read Address for Dual-Port | G[4:1] |
| WE | Write Enable | SR |
| WCLK | Clock | K |
| SPO | Single Port Out (addressed by A[3:0]) | $F_{OUT}$ |
| DPO | Dual Port Out (addressed by DPRA[3:0]) | $G_{OUT}$ |

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

### Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

### More Information on Using RAM Inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: *"Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM,"* and *"Synchronous and Asynchronous FIFO Designs."* All three application notes apply to both the Spartan and the Spartan-XL families.

## Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan

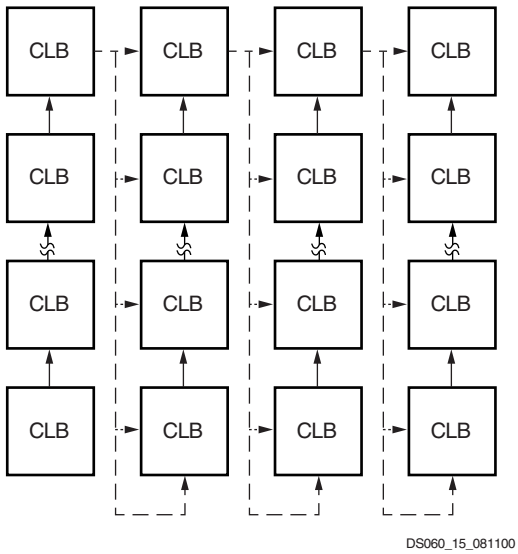



*Figure 15:* **Available Spartan/XL Carry Propagation Paths**

and Spartan-XL families, speeding up arithmetic and counting functions.

The carry chain in 5V Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in Spartan-XL devices can only run up the column, providing even higher speed.

Figure 16, page 18 shows a Spartan/XL FPGA CLB with dedicated fast carry logic. The carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 17, page 19 shows the details of the Spartan/XL FPGA carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 16.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

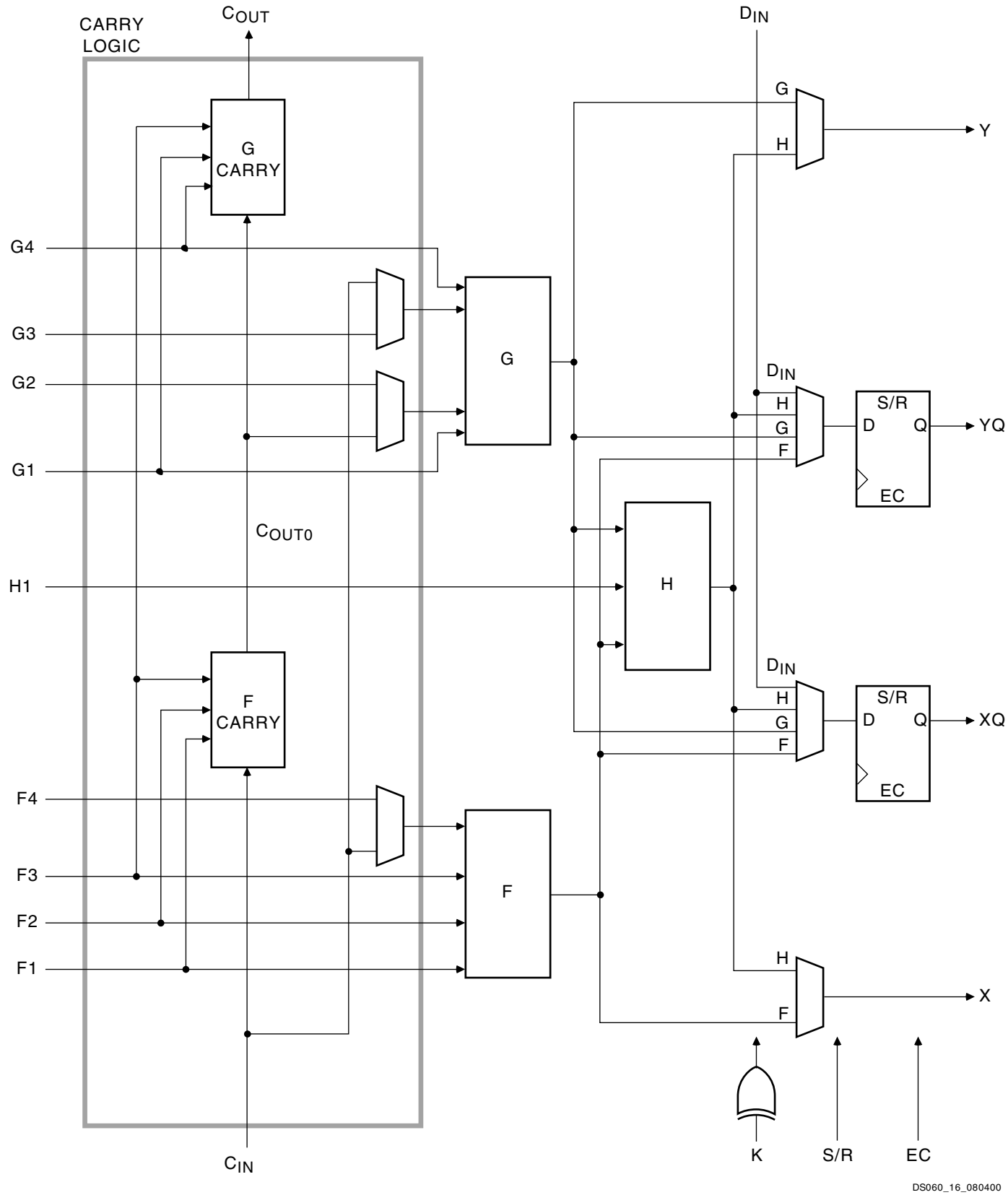
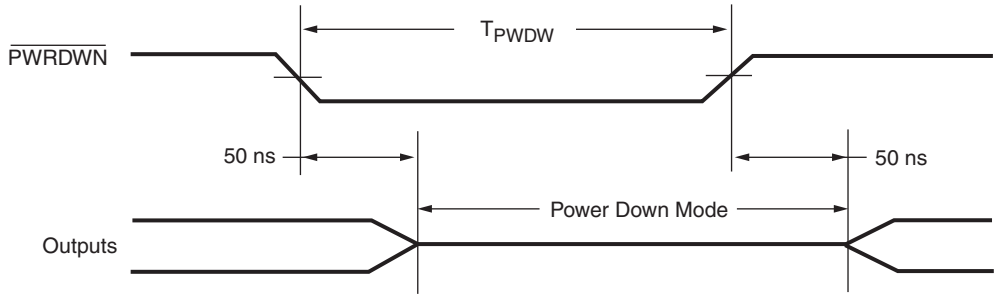



*Figure 16:* **Fast Carry Logic in Spartan/XL CLB**




| Description | Symbol | Min |
|---|---|---|
| Power Down Time | $T_{PWD}$ | 50 ns |
| Power Down Pulse Width | $T_{PWDW}$ | 50 ns |

DS060_23_041901

*Figure 23:* **$\overline{\text{PWRDWN}}$ Pulse Timing**

Power-down retains the configuration, but loses all data stored in the device flip-flops. All inputs are interpreted as Low, but the internal combinatorial logic is fully functional. Make sure that the combination of all inputs Low and all flip-flops set or reset in your design will not generate internal oscillations, or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line.

During configuration, the $\overline{\text{PWRDWN}}$ pin must be High. If the Power Down state is entered before or during configuration, the device will restart configuration once the $\overline{\text{PWRDWN}}$ signal is removed. Note that the configuration pins are affected by Power Down and may not reflect their normal function. If there is an external pull-up resistor on the DONE pin, it will be High during Power Down even if the device is not yet configured. Similarly, if $\overline{\text{PWRDWN}}$ is asserted before configuration is completed, the $\overline{\text{INIT}}$ pin will not indicate status information.

Note that the $\overline{\text{PWRDWN}}$ pin is not part of the Boundary Scan chain. Therefore, the Spartan-XL family has a separate set of BSDL files than the 5V Spartan family. Boundary scan logic is not usable during Power Down.

## Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan/XL devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

### Configuration Mode Control

5V Spartan devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

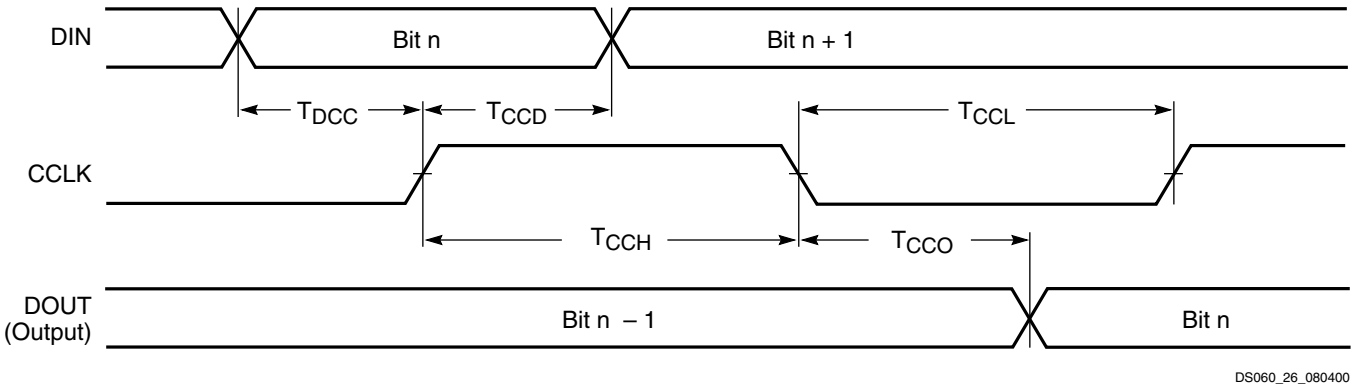
3V Spartan-XL devices have three configuration modes.

- M1/M0 = 11 sets Slave Serial mode
- M1/M0 = 10 sets Master Serial mode
- M1/M0 = 0X sets Express mode

In addition to these modes, the device can be configured through the Boundary Scan logic (See "Configuration Through the Boundary Scan Pins" on page 37.).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pin are unused. The Mode pins have a weak pull-up resistor turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the MODE/M0 pin should be connected directly to GND, or through a pull-down resistor of 1 KΩ or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during con-




| Symbol | | Description | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{DCC}$ | CCLK | DIN setup | 20 | - | ns |
| $T_{CCD}$ | | DIN hold | 0 | - | ns |
| $T_{CCO}$ | | DIN to DOUT | - | 30 | ns |
| $T_{CCH}$ | | High time | 40 | - | ns |
| $T_{CCL}$ | | Low time | 40 | - | ns |
| $F_{CC}$ | | Frequency | - | 12.5 | MHz |

**Notes:**
1. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

*Figure 26:* **Slave Serial Mode Programming Switching Characteristics**

## Express Mode (Spartan-XL Family Only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

### *Pseudo Daisy Chain*

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized

to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.

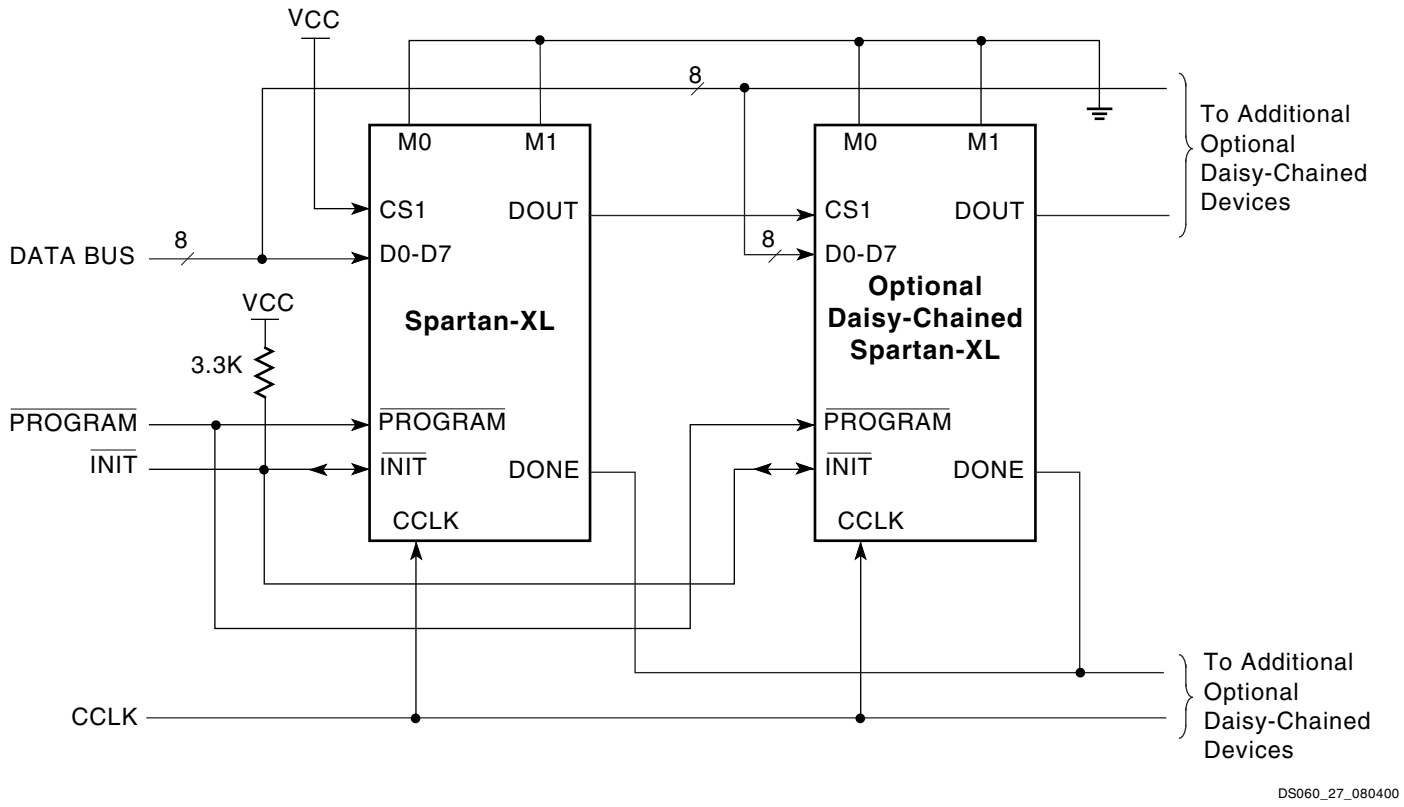
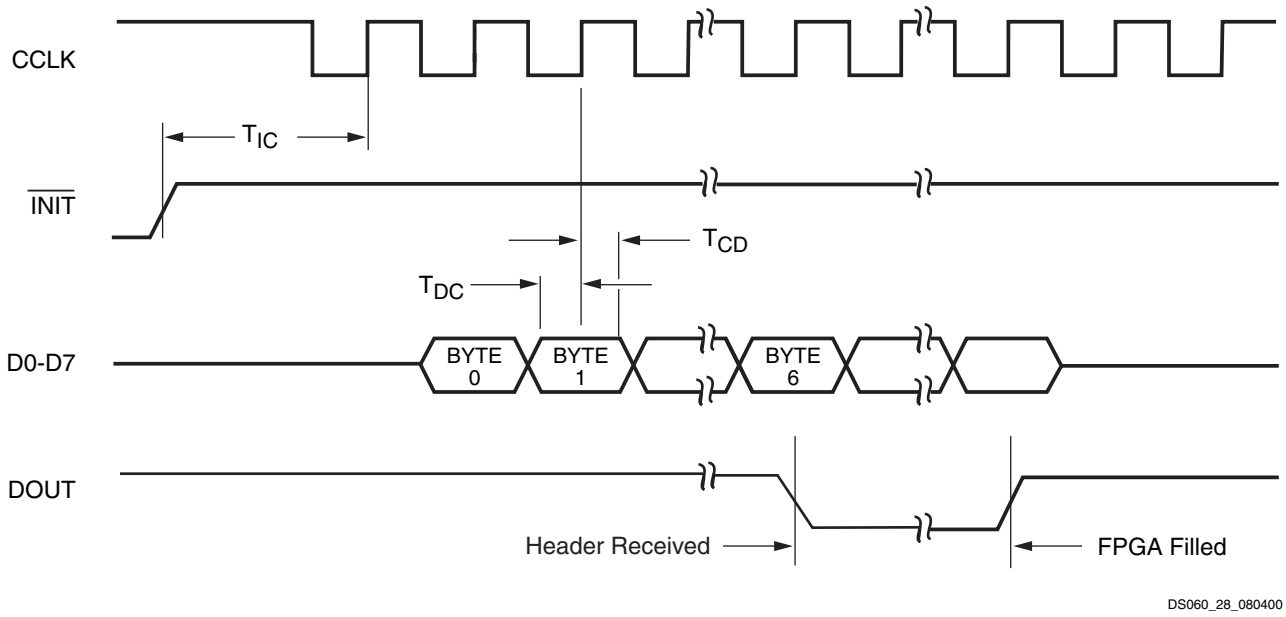



*Figure 27:* **Express Mode Circuit Diagram**




| Symbol | | Description | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{IC}$ | CCLK | $\overline{INIT}$ (High) setup time | 5 | - | µs |
| $T_{DC}$ | | D0-D7 setup time | 20 | - | ns |
| $T_{CD}$ | | D0-D7 hold time | 0 | - | ns |
| $T_{CCH}$ | | CCLK High time | 45 | - | ns |
| $T_{CCL}$ | | CCLK Low time | 45 | - | ns |
| $F_{CC}$ | | CCLK Frequency | - | 10 | MHz |

**Notes:**
1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

*Figure 28:* **Express Mode Programming Switching Characteristics**

## Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

## Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right. Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

### Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

### Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

### Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 16 and Table 17.

## Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.

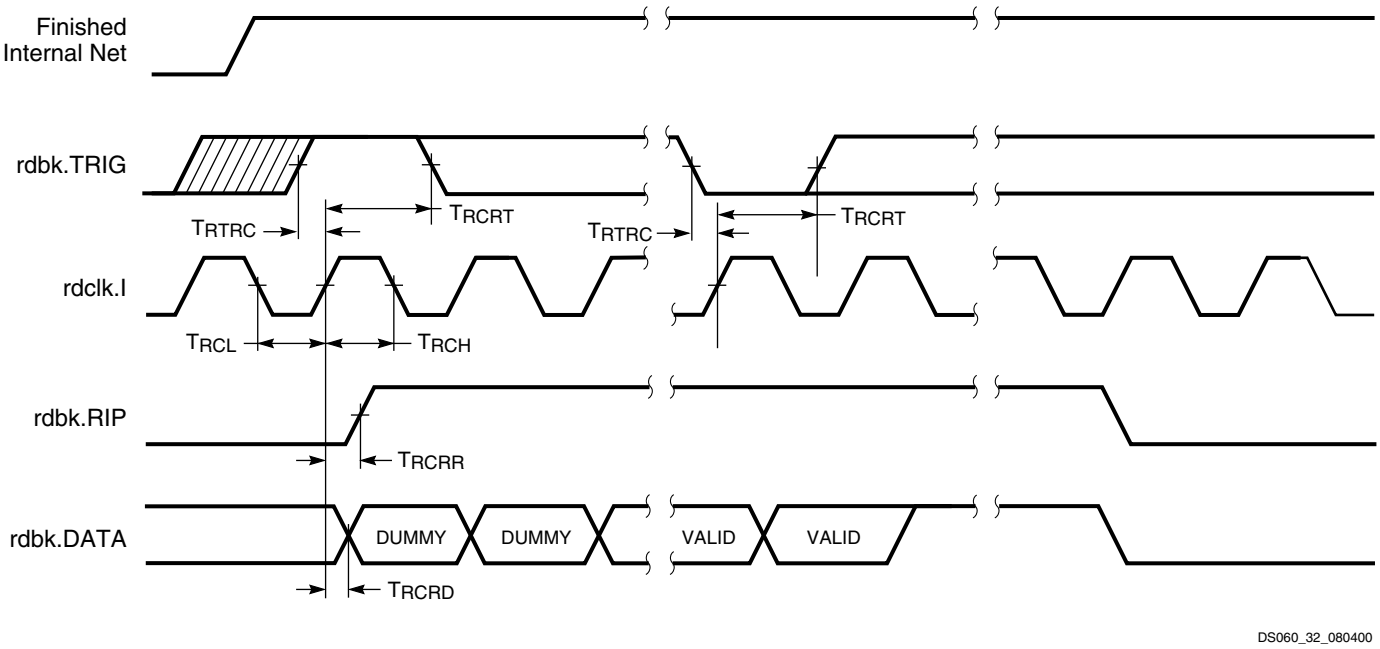



*Figure 33:* **Spartan and Spartan-XL Readback Timing Diagram**

**Spartan and Spartan-XL Readback Switching Characteristics**

| Symbol | | Description | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{RTRC}$ | rdbk.TRIG | rdbk.TRIG setup to initiate and abort Readback | 200 | - | ns |
| $T_{RCRT}$ | | rdbk.TRIG hold to initiate and abort Readback | 50 | - | ns |
| $T_{RCRD}$ | rdclk.I | rdbk.DATA delay | - | 250 | ns |
| $T_{RCRR}$ | | rdbk.RIP delay | - | 250 | ns |
| $T_{RCH}$ | | High time | 250 | 500 | ns |
| $T_{RCL}$ | | Low time | 250 | 500 | ns |

**Notes:**
1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

## Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -4 | | -3 | | |
| | | Min | Max | Min | Max | |
| **Clocks** | | | | | | |
| $T_{CH}$ | Clock High time | 3.0 | - | 4.0 | - | ns |
| $T_{CL}$ | Clock Low time | 3.0 | - | 4.0 | - | ns |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | F/G inputs to X/Y outputs | - | 1.2 | - | 1.6 | ns |
| $T_{IHO}$ | F/G inputs via H to X/Y outputs | - | 2.0 | - | 2.7 | ns |
| $T_{HH1O}$ | C inputs via H1 via H to X/Y outputs | - | 1.7 | - | 2.2 | ns |
| **CLB Fast Carry Logic** | | | | | | |
| $T_{OPCY}$ | Operand inputs (F1, F2, G1, G4) to $C_{OUT}$ | - | 1.7 | - | 2.1 | ns |
| $T_{ASCY}$ | Add/Subtract input (F3) to $C_{OUT}$ | - | 2.8 | - | 3.7 | ns |
| $T_{INCY}$ | Initialization inputs (F1, F3) to $C_{OUT}$ | - | 1.2 | - | 1.4 | ns |
| $T_{SUM}$ | $C_{IN}$ through function generators to X/Y outputs | - | 2.0 | - | 2.6 | ns |
| $T_{BYP}$ | $C_{IN}$ to $C_{OUT}$, bypass function generators | - | 0.5 | - | 0.6 | ns |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | Clock K to Flip-Flop outputs Q | - | 2.1 | - | 2.8 | ns |
| **Setup Time before Clock K** | | | | | | |
| $T_{ICK}$ | F/G inputs | 1.8 | - | 2.4 | - | ns |
| $T_{IHCK}$ | F/G inputs via H | 2.9 | - | 3.9 | - | ns |
| $T_{HH1CK}$ | C inputs via H1 through H | 2.3 | - | 3.3 | - | ns |
| $T_{DICK}$ | C inputs via DIN | 1.3 | - | 2.0 | - | ns |
| $T_{ECCK}$ | C inputs via EC | 2.0 | - | 2.6 | - | ns |
| $T_{RCK}$ | C inputs via S/R, going Low (inactive) | 2.5 | - | 4.0 | - | ns |
| **Hold Time after Clock K** | | | | | | |
| | All Hold times, all devices | 0.0 | - | 0.0 | - | ns |
| **Set/Reset Direct** | | | | | | |
| $T_{RPW}$ | Width (High) | 3.0 | - | 4.0 | - | ns |
| $T_{RIO}$ | Delay from C inputs via S/R, going High to Q | - | 3.0 | - | 4.0 | ns |
| **Global Set/Reset** | | | | | | |
| $T_{MRW}$ | Minimum GSR pulse width | 11.5 | - | 13.5 | - | ns |
| $T_{MRQ}$ | Delay from GSR input to any Q | See page 50 for $T_{RRI}$ values per device. | | | | |
| $F_{TOG}$ | Toggle Frequency (MHz) (for export control purposes) | - | 166 | - | 125 | MHz |

## Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

### *Spartan Family Primary and Secondary Setup and Hold*

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -4 | -3 | |
| | | | Min | Min | |
| **Input Setup/Hold Times Using Primary Clock and IFF** | | | | | |
| $T_{PSUF}/T_{PHF}$ | No Delay | XCS05 | 1.2 / 1.7 | 1.8 / 2.5 | ns |
| | | XCS10 | 1.0 / 2.3 | 1.5 / 3.4 | ns |
| | | XCS20 | 0.8 / 2.7 | 1.2 / 4.0 | ns |
| | | XCS30 | 0.6 / 3.0 | 0.9 / 4.5 | ns |
| | | XCS40 | 0.4 / 3.5 | 0.6 / 5.2 | ns |
| $T_{PSU}/T_{PH}$ | With Delay | XCS05 | 4.3 / 0.0 | 6.0 / 0.0 | ns |
| | | XCS10 | 4.3 / 0.0 | 6.0 / 0.0 | ns |
| | | XCS20 | 4.3 / 0.0 | 6.0 / 0.0 | ns |
| | | XCS30 | 4.3 / 0.0 | 6.0 / 0.0 | ns |
| | | XCS40 | 5.3 / 0.0 | 6.8 / 0.0 | ns |
| **Input Setup/Hold Times Using Secondary Clock and IFF** | | | | | |
| $T_{SSUF}/T_{SHF}$ | No Delay | XCS05 | 0.9 / 2.2 | 1.5 / 3.0 | ns |
| | | XCS10 | 0.7 / 2.8 | 1.2 / 3.9 | ns |
| | | XCS20 | 0.5 / 3.2 | 0.9 / 4.5 | ns |
| | | XCS30 | 0.3 / 3.5 | 0.6 / 5.0 | ns |
| | | XCS40 | 0.1 / 4.0 | 0.3 / 5.7 | ns |
| $T_{SSU}/T_{SH}$ | With Delay | XCS05 | 4.0 / 0.0 | 5.7 / 0.0 | ns |
| | | XCS10 | 4.0 / 0.0 | 5.7 / 0.0 | ns |
| | | XCS20 | 4.0 / 0.5 | 5.7 / 0.5 | ns |
| | | XCS30 | 4.0 / 0.5 | 5.7 / 0.5 | ns |
| | | XCS40 | 5.0 / 0.0 | 6.5 / 0.0 | ns |

**Notes:**

1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

# Spartan-XL Family Detailed Specifications

## Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.
**Preliminary:** Based on preliminary characterization. Further changes are not expected.
**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

## Spartan-XL Family Absolute Maximum Ratings(1)

| Symbol | Description | | Value | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND | | –0.5 to 4.0 | V |
| $V_{IN}$ | Input voltage relative to GND | 5V Tolerant I/O Checked(2, 3) | –0.5 to 5.5 | V |
| | | Not 5V Tolerant I/Os(4, 5) | –0.5 to $V_{CC}$ + 0.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output | 5V Tolerant I/O Checked(2, 3) | –0.5 to 5.5 | V |
| | | Not 5V Tolerant I/Os(4, 5) | –0.5 to $V_{CC}$ + 0.5 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | °C |
| $T_J$ | Junction temperature | Plastic packages | +125 | °C |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
5. Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0V or overshoot to $V_{CC}$ + 2.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Package Information on the Xilinx website.

## Spartan-XL Family Recommended Operating Conditions

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND, $T_J$ = 0°C to +85°C | Commercial | 3.0 | 3.6 | V |
| | Supply voltage relative to GND, $T_J$ = –40°C to +100°C(1) | Industrial | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage(2) | | 50% of $V_{CC}$ | 5.5 | V |
| $V_{IL}$ | Low-level input voltage(2) | | 0 | 30% of $V_{CC}$ | V |
| $T_{IN}$ | Input signal transition time | | - | 250 | ns |

**Notes:**
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold is ~50% of $V_{CC}$.

## Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

| Symbol | Single Port RAM | Size(1) | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -5 | | -4 | | |
| | | | Min | Max | Min | Max | |
| **Write Operation** | | | | | | | |
| $T_{WCS}$ | Address write cycle time (clock K period) | 16x2 | 7.7 | - | 8.4 | - | ns |
| $T_{WCTS}$ | | 32x1 | 7.7 | - | 8.4 | - | ns |
| $T_{WPS}$ | Clock K pulse width (active edge) | 16x2 | 3.1 | - | 3.6 | - | ns |
| $T_{WPTS}$ | | 32x1 | 3.1 | - | 3.6 | - | ns |
| $T_{ASS}$ | Address setup time before clock K | 16x2 | 1.3 | - | 1.5 | - | ns |
| $T_{ASTS}$ | | 32x1 | 1.5 | - | 1.7 | - | ns |
| $T_{DSS}$ | DIN setup time before clock K | 16x2 | 1.5 | - | 1.7 | - | ns |
| $T_{DSTS}$ | | 32x1 | 1.8 | - | 2.1 | - | ns |
| $T_{WSS}$ | WE setup time before clock K | 16x2 | 1.4 | - | 1.6 | - | ns |
| $T_{WSTS}$ | | 32x1 | 1.3 | - | 1.5 | - | ns |
| | All hold times after clock K | 16x2 | 0.0 | - | 0.0 | - | ns |
| $T_{WOS}$ | Data valid after clock K | 32x1 | - | 4.5 | - | 5.3 | ns |
| $T_{WOTS}$ | | 16x2 | - | 5.4 | - | 6.3 | ns |
| **Read Operation** | | | | | | | |
| $T_{RC}$ | Address read cycle time | 16x2 | 2.6 | - | 3.1 | - | ns |
| $T_{RCT}$ | | 32x1 | 3.8 | - | 5.5 | - | ns |
| $T_{ILO}$ | Data Valid after address change (no Write Enable) | 16x2 | - | 1.0 | - | 1.1 | ns |
| $T_{IHO}$ | | 32x1 | - | 1.7 | - | 2.0 | ns |
| $T_{ICK}$ | Address setup time before clock K | 16x2 | 0.6 | - | 0.7 | - | ns |
| $T_{IHCK}$ | | 32x1 | 1.3 | - | 1.6 | - | ns |

**Notes:**
1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

## Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

***Spartan-XL Family Setup and Hold***

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -5 | -4 | |
| | | | Max | Max | |
| **Input Setup/Hold Times Using Global Clock and IFF** | | | | | |
| $T_{SUF}/T_{HF}$ | No Delay | XCS05XL | 1.1/2.0 | 1.6/2.6 | ns |
| | | XCS10XL | 1.0/2.2 | 1.5/2.8 | ns |
| | | XCS20XL | 0.9/2.4 | 1.4/3.0 | ns |
| | | XCS30XL | 0.8/2.6 | 1.3/3.2 | ns |
| | | XCS40XL | 0.7/2.8 | 1.2/3.4 | ns |
| $T_{SU}/T_{H}$ | Full Delay | XCS05XL | 3.9/0.0 | 5.1/0.0 | ns |
| | | XCS10XL | 4.1/0.0 | 5.3/0.0 | ns |
| | | XCS20XL | 4.3/0.0 | 5.5/0.0 | ns |
| | | XCS30XL | 4.5/0.0 | 5.7/0.0 | ns |
| | | XCS40XL | 4.7/0.0 | 5.9/0.0 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

### Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

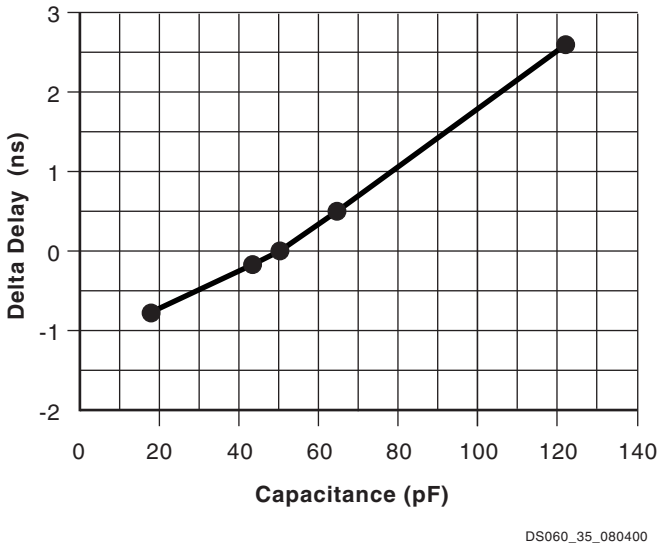



*Figure 35:* **Delay Factor at Various Capacitive Loads**

## Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -5 | | -4 | | |
| | | | Min | Max | Min | Max | |
| **Propagation Delays** | | | | | | | |
| $T_{OKPOF}$ | Clock (OK) to Pad, fast | All devices | - | 3.2 | - | 3.7 | ns |
| $T_{OPF}$ | Output (O) to Pad, fast | All devices | - | 2.5 | - | 2.9 | ns |
| $T_{TSHZ}$ | 3-state to Pad High-Z (slew-rate independent) | All devices | - | 2.8 | - | 3.3 | ns |
| $T_{TSONF}$ | 3-state to Pad active and valid, fast | All devices | - | 2.6 | - | 3.0 | ns |
| $T_{OFPF}$ | Output (O) to Pad via Output MUX, fast | All devices | - | 3.7 | - | 4.4 | ns |
| $T_{OKFPF}$ | Select (OK) to Pad via Output MUX, fast | All devices | - | 3.3 | - | 3.9 | ns |
| $T_{SLOW}$ | For Output SLOW option add | All devices | - | 1.5 | - | 1.7 | ns |
| **Setup and Hold Times** | | | | | | | |
| $T_{OOK}$ | Output (O) to clock (OK) setup time | All devices | 0.5 | - | 0.5 | - | ns |
| $T_{OKO}$ | Output (O) to clock (OK) hold time | All devices | 0.0 | - | 0.0 | - | ns |
| $T_{ECOK}$ | Clock Enable (EC) to clock (OK) setup time | All devices | 0.0 | - | 0.0 | - | ns |
| $T_{OKEC}$ | Clock Enable (EC) to clock (OK) hold time | All devices | 0.1 | - | 0.2 | - | ns |
| **Global Set/Reset** | | | | | | | |
| $T_{MRW}$ | Minimum GSR pulse width | All devices | 10.5 | - | 11.5 | - | ns |
| $T_{RPO}$ | Delay from GSR input to any Pad | XCS05XL | - | 11.9 | - | 14.0 | ns |
| | | XCS10XL | - | 12.4 | - | 14.5 | ns |
| | | XCS20XL | - | 12.9 | - | 15.0 | ns |
| | | XCS30XL | - | 13.9 | - | 16.0 | ns |
| | | XCS40XL | - | 14.9 | - | 17.0 | ns |

**Notes:**

1. Output timing is measured at ~50% $V_{CC}$ threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## XCS20 and XCS20XL Device Pinouts

| XCS20/XL Pad Name | VQ100 | CS144[2,4] | TQ144 | PQ208 | Bndry Scan |
|---|---|---|---|---|---|
| PROGRAM | P52 | M13 | P74 | P106 | - |
| I/O (D7[2]) | P53 | L12 | P75 | P107 | 367 [3] |
| I/O, PGCK3[1], GCK5[2] | P54 | L13 | P76 | P108 | 370 [3] |
| I/O | - | K10 | P77 | P109 | 373 [3] |
| I/O | - | K11 | P78 | P110 | 376 [3] |
| I/O (D6[2]) | P55 | K12 | P79 | P112 | 379 [3] |
| I/O | P56 | K13 | P80 | P113 | 382 [3] |
| I/O | - | - | - | P114 | 385 [3] |
| I/O | - | - | - | P115 | 388 [3] |
| I/O | - | - | - | P116 | 391 [3] |
| I/O | - | - | - | P117 | 394 [3] |
| GND | - | J10 | P81 | P118 | - |
| I/O | - | J11 | P82 | P119 | 397 [3] |
| I/O | - | J12 | P83 | P120 | 400 [3] |
| VCC[2] | - | - | - | P121 | - |
| I/O (D5[2]) | P57 | J13 | P84 | P122 | 403 [3] |
| I/O | P58 | H10 | P85 | P123 | 406 [3] |
| I/O | - | - | - | P124 | 409 [3] |
| I/O | - | - | - | P125 | 412 [3] |
| I/O | P59 | H11 | P86 | P126 | 415 [3] |
| I/O | P60 | H12 | P87 | P127 | 418 [3] |
| I/O (D4[2]) | P61 | H13 | P88 | P128 | 421 [3] |
| I/O | P62 | G12 | P89 | P129 | 424 [3] |
| VCC | P63 | G13 | P90 | P130 | - |
| GND | P64 | G11 | P91 | P131 | - |
| I/O (D3[2]) | P65 | G10 | P92 | P132 | 427 [3] |
| I/O | P66 | F13 | P93 | P133 | 430 [3] |
| I/O | P67 | F12 | P94 | P134 | 433 [3] |
| I/O | - | F11 | P95 | P135 | 436 [3] |
| I/O | - | - | - | P136 | 439 [3] |
| I/O | - | - | - | P137 | 442 [3] |
| I/O (D2[2]) | P68 | F10 | P96 | P138 | 445 [3] |
| I/O | P69 | E13 | P97 | P139 | 448 [3] |
| VCC[2] | - | - | - | P140 | - |
| I/O | - | E12 | P98 | P141 | 451 [3] |
| I/O | - | E11 | P99 | P142 | 454 [3] |
| GND | - | E10 | P100 | P143 | - |
| I/O | - | - | - | P145 | 457 [3] |
| I/O | - | - | - | P146 | 460 [3] |
| I/O | - | - | - | P147 | 463 [3] |
| I/O | - | - | - | P148 | 466 [3] |
| I/O (D1[2]) | P70 | D13 | P101 | P149 | 469 [3] |
| I/O | P71 | D12 | P102 | P150 | 472 [3] |
| I/O | - | D11 | P103 | P151 | 475 [3] |

## XCS20 and XCS20XL Device Pinouts

| XCS20/XL Pad Name | VQ100 | CS144[2,4] | TQ144 | PQ208 | Bndry Scan |
|---|---|---|---|---|---|
| I/O | - | C13 | P104 | P152 | 478 [3] |
| I/O (D0[2], DIN) | P72 | C12 | P105 | P153 | 481 [3] |
| I/O, SGCK4[1], GCK6[2] (DOUT) | P73 | C11 | P106 | P154 | 484 [3] |
| CCLK | P74 | B13 | P107 | P155 | - |
| VCC | P75 | B12 | P108 | P156 | - |
| O, TDO | P76 | A13 | P109 | P157 | 0 |
| GND | P77 | A12 | P110 | P158 | - |
| I/O | P78 | B11 | P111 | P159 | 2 |
| I/O, PGCK4[1], GCK7[2] | P79 | A11 | P112 | P160 | 5 |
| I/O | - | D10 | P113 | P161 | 8 |
| I/O | - | C10 | P114 | P162 | 11 |
| I/O (CS1[2]) | P80 | B10 | P115 | P163 | 14 |
| I/O | P81 | A10 | P116 | P164 | 17 |
| I/O | - | D9 | P117 | P166 | 20 |
| I/O | - | - | - | P167 | 23 |
| I/O | - | - | - | P168 | 26 |
| I/O | - | - | - | P169 | 29 |
| GND | - | C9 | P118 | P170 | - |
| I/O | - | B9 | P119 | P171 | 32 |
| I/O | - | A9 | P120 | P172 | 35 |
| VCC[2] | - | - | - | P173 | - |
| I/O | P82 | D8 | P121 | P174 | 38 |
| I/O | P83 | C8 | P122 | P175 | 41 |
| I/O | - | - | - | P176 | 44 |
| I/O | - | - | - | P177 | 47 |
| I/O | P84 | B8 | P123 | P178 | 50 |
| I/O | P85 | A8 | P124 | P179 | 53 |
| I/O | P86 | B7 | P125 | P180 | 56 |
| I/O | P87 | A7 | P126 | P181 | 59 |
| GND | P88 | C7 | P127 | P182 | - |

2/8/00

## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| GND | P25 | P29 | GND(4) | GND(4) | - |
| VCC | P26 | P30 | VCC(4) | VCC(4) | - |
| I/O | P27 | P31 | L2 | K3 | 254 |
| I/O | P28 | P32 | L3 | K4 | 257 |
| I/O | P29 | P33 | L4 | K5 | 260 |
| I/O | P30 | P34 | M1 | L1 | 263 |
| I/O | P31 | P35 | M2 | L2 | 266 |
| I/O | P32 | P36 | M3 | L3 | 269 |
| I/O | - | - | M4 | L4 | 272 |
| I/O | - | - | - | M1 | 275 |
| I/O | - | P38 | N1 | M2 | 278 |
| I/O | - | P39 | N2 | M3 | 281 |
| VCC | P33 | P40 | VCC(4) | VCC(4) | - |
| I/O | P34 | P41 | P1 | N1 | 284 |
| I/O | P35 | P42 | P2 | N2 | 287 |
| I/O | P36 | P43 | R1 | N3 | 290 |
| I/O | P37 | P44 | P3 | N4 | 293 |
| GND | P38 | P45 | GND(4) | GND(4) | - |
| I/O | - | P46 | T1 | P1 | 296 |
| I/O | P39 | P47 | R3 | P2 | 299 |
| I/O | P40 | P48 | T2 | P3 | 302 |
| I/O | P41 | P49 | U1 | P4 | 305 |
| I/O | P42 | P50 | T3 | P5 | 308 |
| I/O | P43 | P51 | U2 | R1 | 311 |
| I/O | - | - | - | R2 | 314 |
| I/O | - | - | - | R4 | 317 |
| I/O | P44 | P52 | V1 | T1 | 320 |
| I/O | P45 | P53 | T4 | T2 | 323 |
| I/O | P46 | P54 | U3 | T3 | 326 |
| I/O | P47 | P55 | V2 | U1 | 329 |
| I/O | P48 | P56 | W1 | V1 | 332 |
| I/O, SGCK2(1), GCK2 (2) | P49 | P57 | V3 | U2 | 335 |
| Not Connected(1) M1(2) | P50 | P58 | W2 | V2 | 338 |
| GND | P51 | P59 | GND(4) | GND(4) | - |
| MODE(1), M0(2) | P52 | P60 | Y1 | W1 | 341 |
| VCC | P53 | P61 | VCC(4) | VCC(4) | - |
| Not Connected(1) $\overline{\text{PWRDWN}}$(2) | P54 | P62 | W3 | V3 | 342(1) |
| I/O, PGCK2(1), GCK3(2) | P55 | P63 | Y2 | W2 | 343 (3) |

## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| I/O (HDC) | P56 | P64 | W4 | W3 | 346 (3) |
| I/O | P57 | P65 | V4 | T4 | 349 (3) |
| I/O | P58 | P66 | U5 | U4 | 352 (3) |
| I/O | P59 | P67 | Y3 | V4 | 355 (3) |
| I/O ($\overline{\text{LDC}}$) | P60 | P68 | Y4 | W4 | 358 (3) |
| I/O | - | - | - | R5 | 361 (3) |
| I/O | - | - | - | U5 | 364 (3) |
| I/O | P61 | P69 | V5 | T5 | 367 (3) |
| I/O | P62 | P70 | W5 | W5 | 370 (3) |
| I/O | P63 | P71 | Y5 | R6 | 373 (3) |
| I/O | P64 | P72 | V6 | U6 | 376 (3) |
| I/O | P65 | P73 | W6 | V6 | 379 (3) |
| I/O | - | P74 | Y6 | T6 | 382 (3) |
| GND | P66 | P75 | GND(4) | GND(4) | - |
| I/O | P67 | P76 | W7 | W6 | 385 (3) |
| I/O | P68 | P77 | Y7 | U7 | 388 (3) |
| I/O | P69 | P78 | V8 | V7 | 391 (3) |
| I/O | P70 | P79 | W8 | W7 | 394 (3) |
| VCC | P71 | P80 | VCC(4) | VCC(4) | - |
| I/O | P72 | P81 | Y8 | W8 | 397 (3) |
| I/O | P73 | P82 | U9 | U8 | 400 (3) |
| I/O | - | - | V9 | V8 | 403 (3) |
| I/O | - | - | W9 | T8 | 406 (3) |
| I/O | - | P84 | Y9 | W9 | 409 (3) |
| I/O | - | P85 | W10 | V9 | 412 (3) |
| I/O | P74 | P86 | V10 | U9 | 415 (3) |
| I/O | P75 | P87 | Y10 | T9 | 418 (3) |
| I/O | P76 | P88 | Y11 | W10 | 421 (3) |
| I/O ($\overline{\text{INIT}}$) | P77 | P89 | W11 | V10 | 424 (3) |
| VCC | P78 | P90 | VCC(4) | VCC(4) | VCC(4) |
| GND | P79 | P91 | GND(4) | GND(4) | - |
| I/O | P80 | P92 | V11 | T10 | 427 (3) |
| I/O | P81 | P93 | U11 | R10 | 430 (3) |
| I/O | P82 | P94 | Y12 | W11 | 433 (3) |
| I/O | P83 | P95 | W12 | V11 | 436 (3) |
| I/O | P84 | P96 | V12 | U11 | 439 (3) |
| I/O | P85 | P97 | U12 | T11 | 442 (3) |
| I/O | - | - | Y13 | W12 | 445 (3) |
| I/O | - | - | W13 | V12 | 448 (3) |
| I/O | - | P99 | V13 | U12 | 451 (3) |
| I/O | - | P100 | Y14 | T12 | 454 (3) |
| VCC | P86 | P101 | VCC(4) | VCC(4) | - |
| I/O | P87 | P102 | Y15 | V13 | 457 (3) |
| I/O | P88 | P103 | V14 | U13 | 460 (3) |
| I/O | P89 | P104 | W15 | T13 | 463 (3) |

## Revision History

The following table shows the revision history for this document.

| Date | Version | Description |
|---|---|---|
| 11/20/98 | 1.3 | Added Spartan-XL specs and Power Down. |
| 01/06/99 | 1.4 | All Spartan-XL -4 specs designated Preliminary with no changes. |
| 03/02/00 | 1.5 | Added CS package, updated Spartan-XL specs to Final. |
| 09/19/01 | 1.6 | Reformatted, updated power specs, clarified configuration information. Removed $T_{SOL}$ soldering information from Absolute Maximum Ratings table. Changed Figure 26: Slave Serial Mode Characteristics: $T_{CCH}$, $T_{CCL}$ from 45 to 40 ns. Changed Master Mode Configuration Switching Characteristics: $T_{CCLK}$ min. from 80 to 100 ns. Added Total Dist. RAM Bits to Table 1; added **Start-Up**, page 36 characteristics. |
| 06/27/02 | 1.7 | Clarified Express Mode pseudo daisy chain. Added new Industrial options. Clarified XCS30XL CS280 $V_{CC}$ pinout. |
| 06/26/08 | 1.8 | Noted that PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, are discontinued by **PDN2004-01**. Extended description of recommended maximum delay of reconfiguration in **Delaying Configuration After Power-Up**, page 35. Added reference to Pb-free package options and provided link to **Package Specifications**, page 81. Updated links. |
| 03/01/13 | 2.0 | The products listed in this data sheet are obsolete. See **XCN10016** and **XCN11010** for further information. |