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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	466
Total RAM Bits	6272
Number of I/O	77
Number of Gates	10000
Voltage - Supply	4.5V ~ 5.5V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs10-3vq100i

General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in Figure 1. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.

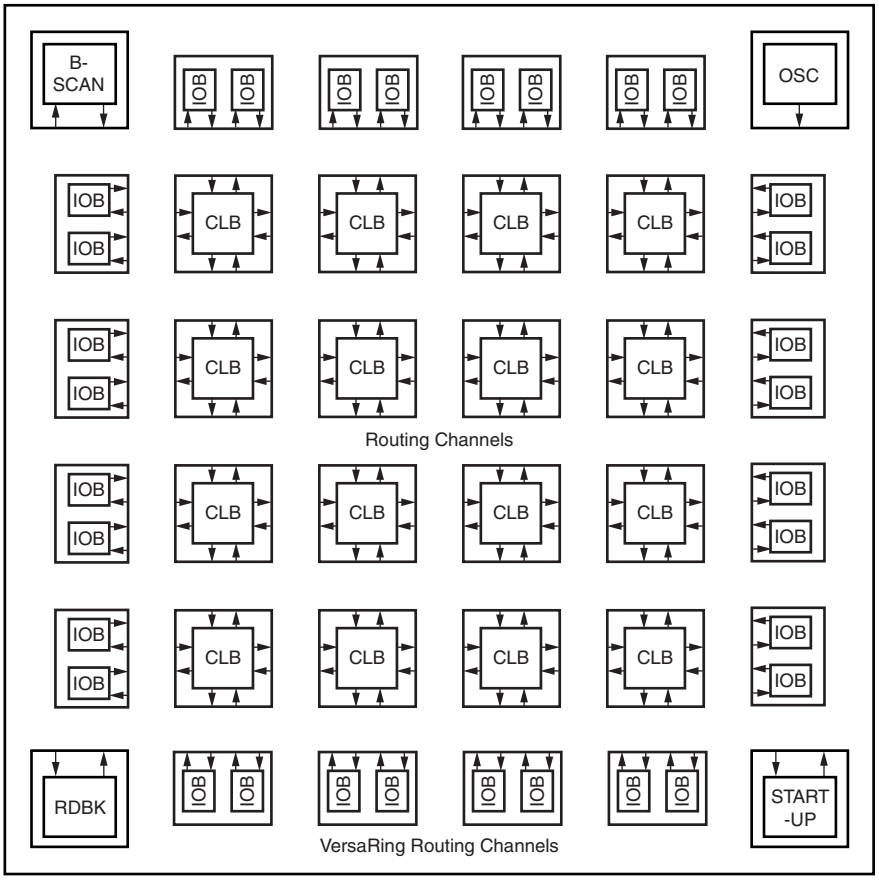


Figure 1: **Basic FPGA Block Diagram**

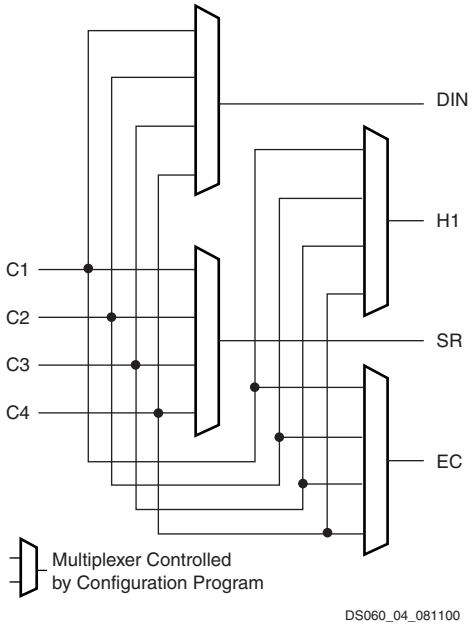


Figure 4: **CLB Control Signal Interface**

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

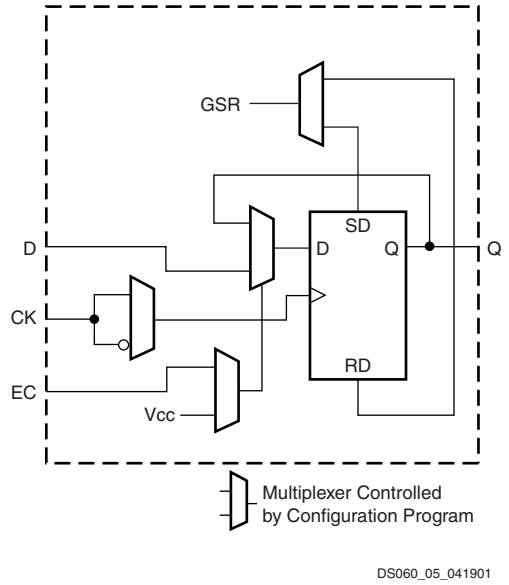


Figure 5: **IOB Flip-Flop/Latch Functional Block Diagram**

IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: **Input Register Functionality**

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	⌐	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care.
⌐	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Output Multiplexer/2-Input Function Generator (Spartan-XL Family Only)

The output path in the Spartan-XL family IOB contains an additional multiplexer not available in the Spartan family IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass gate, AND gate, OR gate, or XOR gate, with 0, 1, or 2 inverted inputs.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. The select input is the pin used for the output flip-flop clock, OK.

When the multiplexer is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe driven by a global buffer.

The user can specify that the IOB function generator be used by placing special library symbols beginning with the letter "O." For example, a 2-input AND gate in the IOB function generator is called OAND2. Use the symbol input pin labeled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in Figure 7.

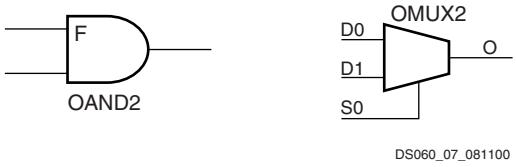


Figure 7: **AND and MUX Symbols in Spartan-XL IOB**

Output Buffer

An active High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (O) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB (see Figure 6, page 7). An output can be configured as open-drain (open-collector) by tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground.

By default, a 5V Spartan device output buffer pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below V_{CC}. Alternatively, the outputs can be globally configured as CMOS drivers, with additional p-channel pull-up transistors pulling to V_{CC}. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable.

All Spartan-XL device outputs are configured as CMOS drivers, therefore driving rail-to-rail. The Spartan-XL family outputs are individually programmable for 12 mA or 24 mA output drive.

Any 5V Spartan device with its outputs configured in TTL mode can drive the inputs of any typical 3.3V device. Supported destinations for Spartan/XL device outputs are shown in Table 7.

Three-State Register (Spartan-XL Family Only)

Spartan-XL devices incorporate an optional register controlling the three-state enable in the IOBs. The use of the three-state control register can significantly improve output enable and disable time.

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

Spartan/XL devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Pull-up and Pull-down Network

Programmable pull-up and pull-down resistors are used for tying unused pins to V_{CC} or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to V_{CC}. The configurable pull-down resistor is an n-channel transistor that pulls to Ground. The value of these resistors is typically 20 KΩ – 100 KΩ (See "Spartan Family DC Characteristics Over Operating Conditions" on page 43.).

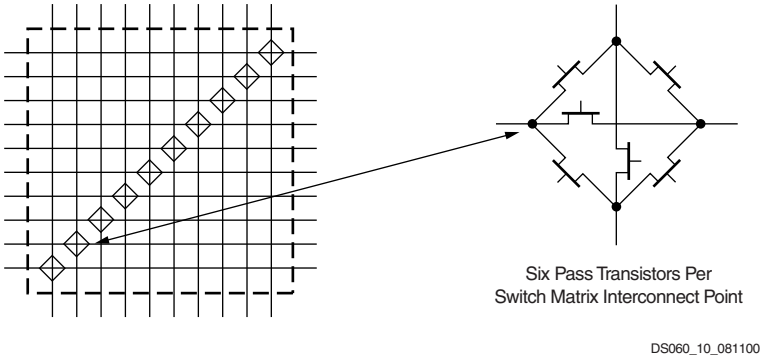


Figure 10: **Programmable Switch Matrix**

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 8).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 8. The longlines also interface to some 3-state buffers which is described later in **3-State Long Line Drivers**, page 19.

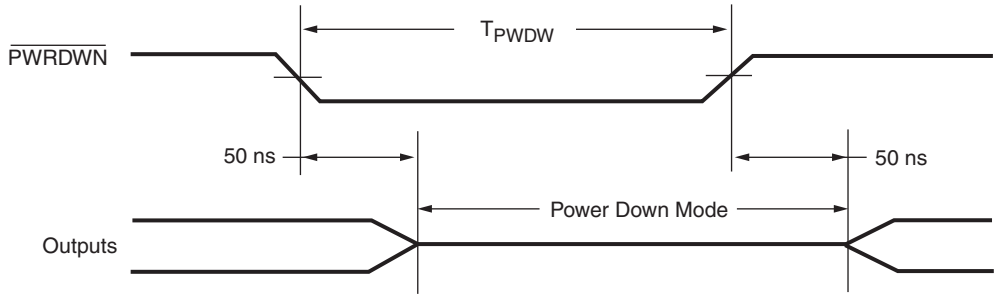
I/O Routing

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 11. In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.



Description	Symbol	Min
Power Down Time	T_{PWD}	50 ns
Power Down Pulse Width	T_{PWDW}	50 ns

DS060_23_041901

Figure 23: **$\overline{\text{PWRDWN}}$ Pulse Timing**

Power-down retains the configuration, but loses all data stored in the device flip-flops. All inputs are interpreted as Low, but the internal combinatorial logic is fully functional. Make sure that the combination of all inputs Low and all flip-flops set or reset in your design will not generate internal oscillations, or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line.

During configuration, the $\overline{\text{PWRDWN}}$ pin must be High. If the Power Down state is entered before or during configuration, the device will restart configuration once the $\overline{\text{PWRDWN}}$ signal is removed. Note that the configuration pins are affected by Power Down and may not reflect their normal function. If there is an external pull-up resistor on the DONE pin, it will be High during Power Down even if the device is not yet configured. Similarly, if $\overline{\text{PWRDWN}}$ is asserted before configuration is completed, the $\overline{\text{INIT}}$ pin will not indicate status information.

Note that the $\overline{\text{PWRDWN}}$ pin is not part of the Boundary Scan chain. Therefore, the Spartan-XL family has a separate set of BSDL files than the 5V Spartan family. Boundary scan logic is not usable during Power Down.

Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan/XL devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Configuration Mode Control

5V Spartan devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

3V Spartan-XL devices have three configuration modes.

- M1/M0 = 11 sets Slave Serial mode
- M1/M0 = 10 sets Master Serial mode
- M1/M0 = 0X sets Express mode

In addition to these modes, the device can be configured through the Boundary Scan logic (See "Configuration Through the Boundary Scan Pins" on page 37.).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pin are unused. The Mode pins have a weak pull-up resistor turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the MODE/M0 pin should be connected directly to GND, or through a pull-down resistor of 1 KΩ or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during con-

to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.

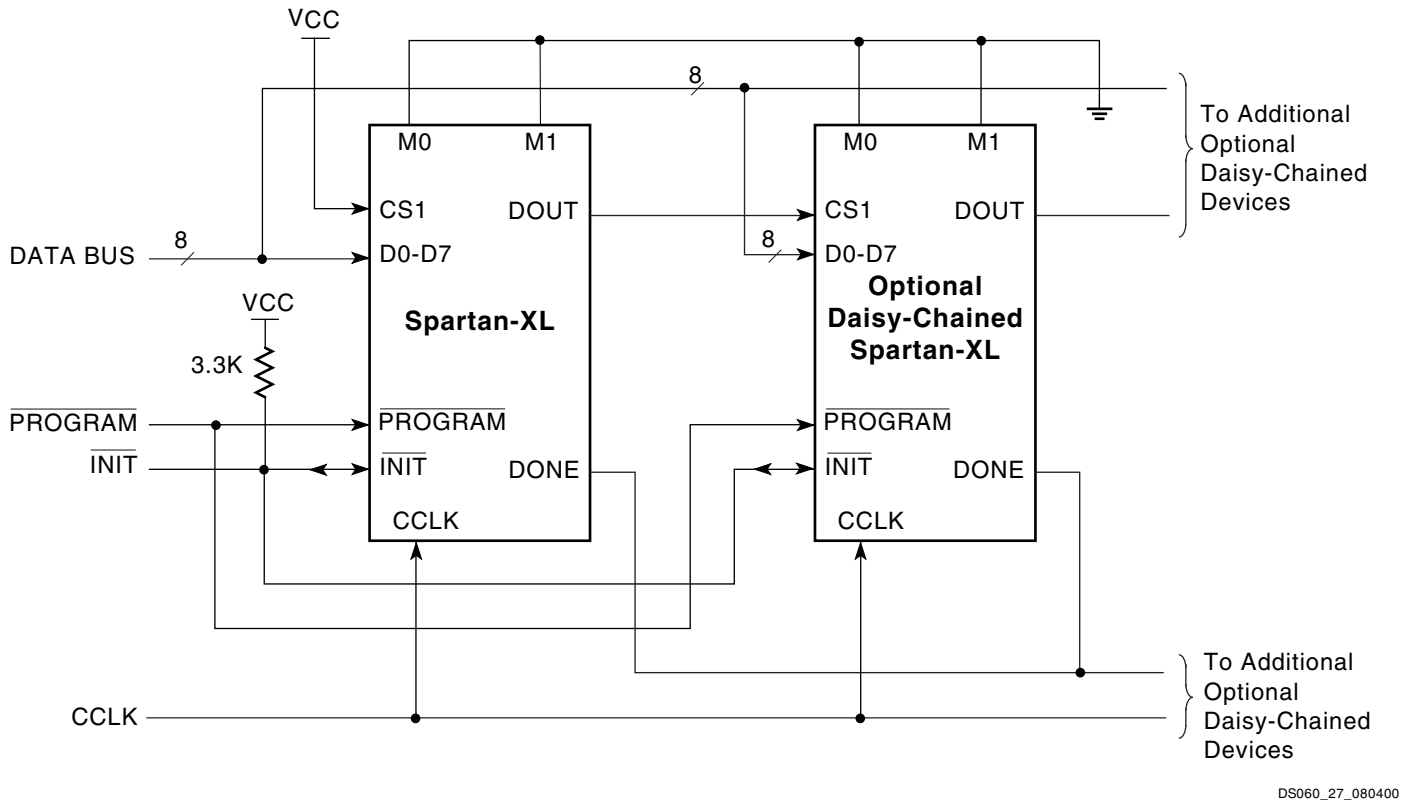
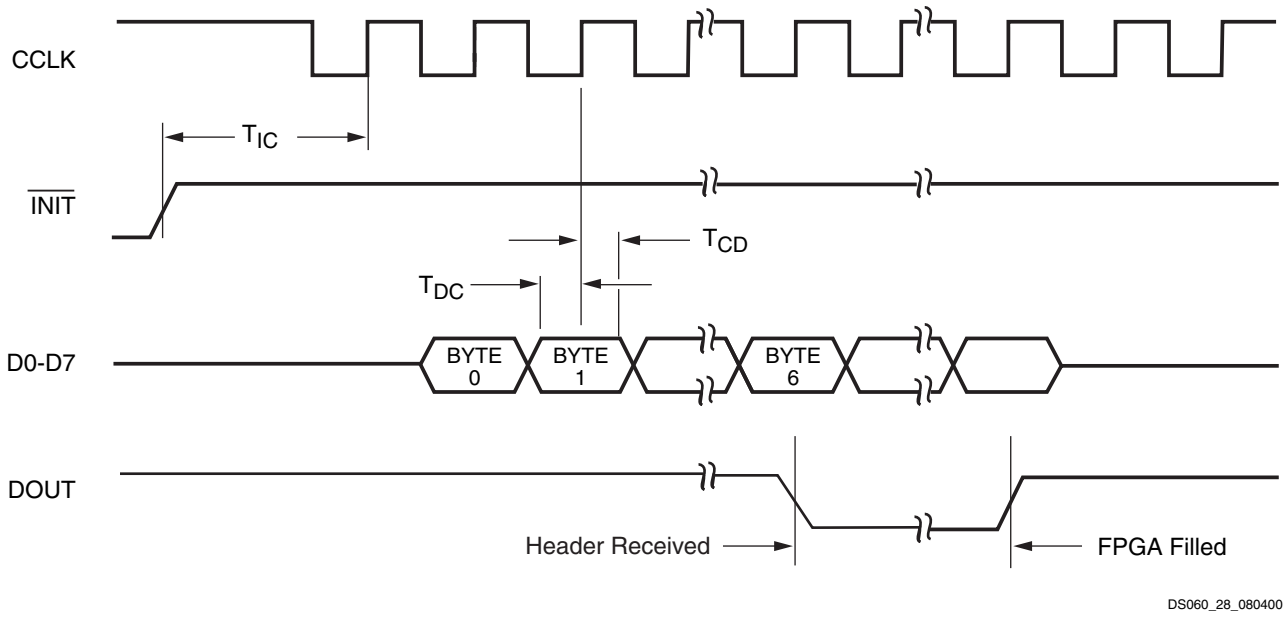


Figure 27: **Express Mode Circuit Diagram**



Symbol		Description	Min	Max	Units
T_{IC}	CCLK	$\overline{INIT}$ (High) setup time	5	-	µs
T_{DC}		D0-D7 setup time	20	-	ns
T_{CD}		D0-D7 hold time	0	-	ns
T_{CCH}		CCLK High time	45	-	ns
T_{CCL}		CCLK Low time	45	-	ns
F_{CC}		CCLK Frequency	-	10	MHz

Notes:
1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: **Express Mode Programming Switching Characteristics**

Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right. Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

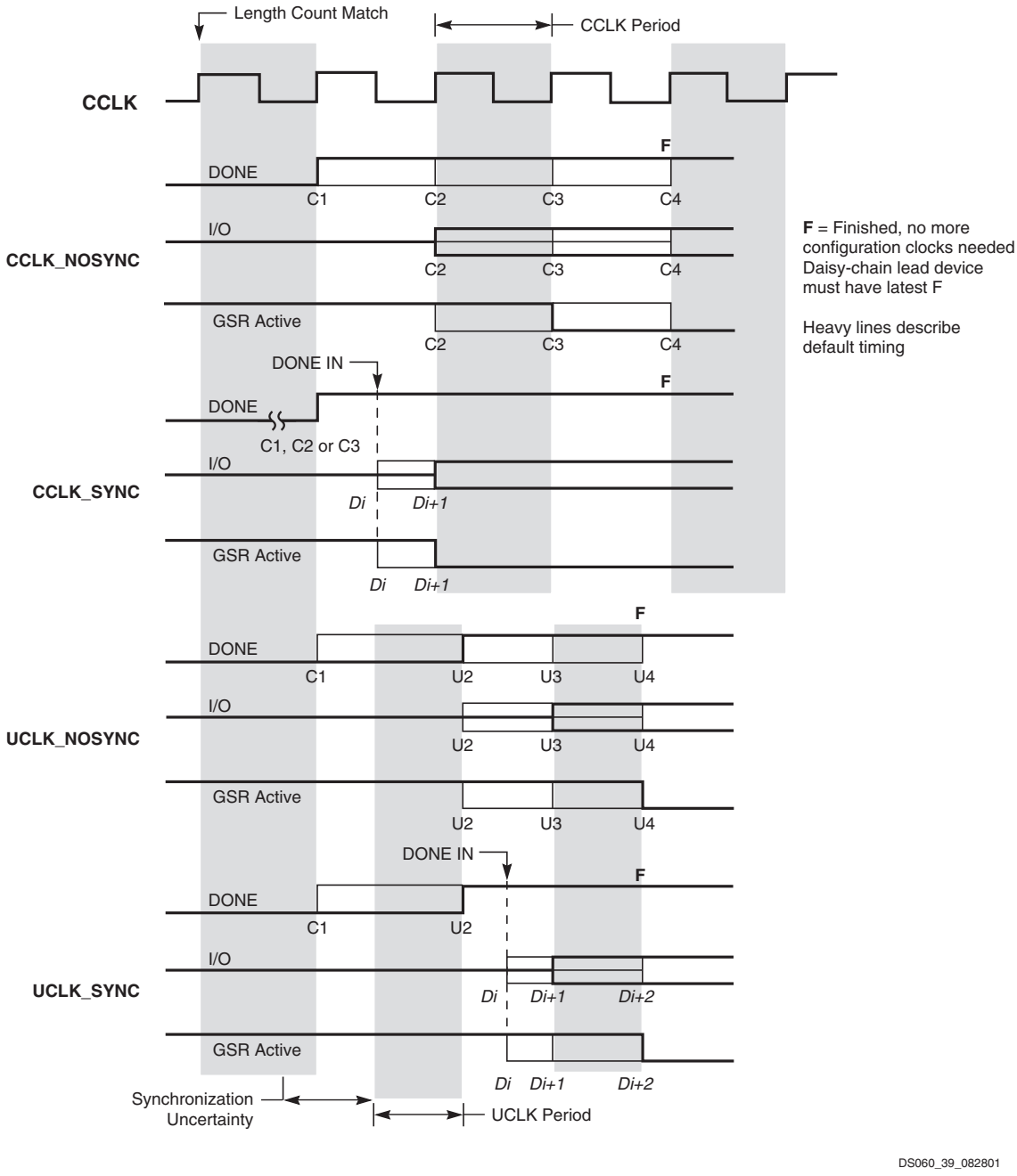


Figure 31: **Start-up Timing**

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input.
- Wait for $\overline{\text{INIT}}$ to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after $\overline{\text{INIT}}$ goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and Spartan-XL devices.

Spartan Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan Family Absolute Maximum Ratings(1)

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND(2,3)		–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output(2,3)		–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot (above V_{CC}) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = –40°C to +100°C(1)	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage(2)	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage(2)	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

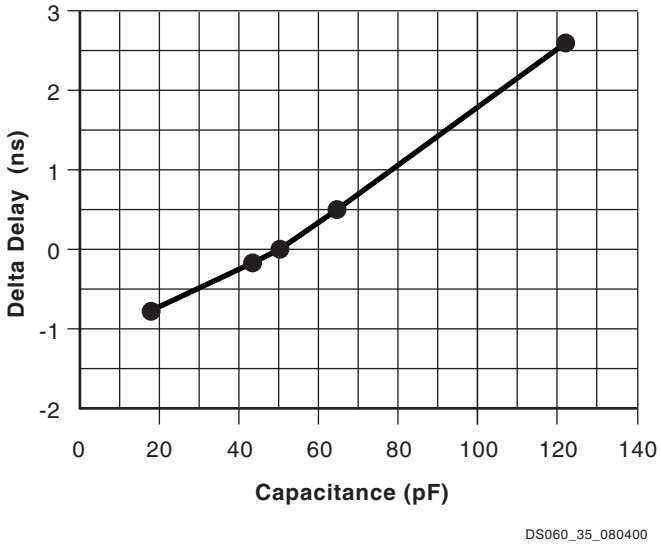


Figure 34: **Delay Factor at Various Capacitive Loads**

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings(1)

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked(2, 3)	–0.5 to 5.5	V
		Not 5V Tolerant I/Os(4, 5)	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked(2, 3)	–0.5 to 5.5	V
		Not 5V Tolerant I/Os(4, 5)	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
5. Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0V or overshoot to V_{CC} + 2.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C(1)	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage(2)		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage(2)		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold is ~50% of V_{CC}.

Spartan-XL Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Global Clock to Output using OFF					
T_{ICKOF}	Fast	XCS05XL	4.6	5.2	ns
		XCS10XL	4.9	5.5	ns
		XCS20XL	5.2	5.8	ns
		XCS30XL	5.5	6.2	ns
		XCS40XL	5.8	6.5	ns
Slew Rate Adjustment					
T_{SLOW}	For Output SLOW option add	All Devices	1.5	1.7	ns

Notes:
1. Output delays are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.
3. OFF = Output Flip Flop

Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Setup and Hold

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Input Setup/Hold Times Using Global Clock and IFF					
T_{SUF}/T_{HF}	No Delay	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
T_{SU}/T_{H}	Full Delay	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

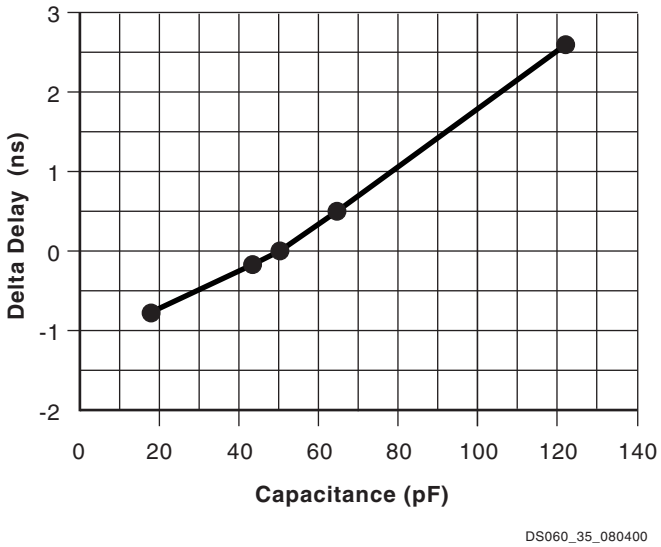


Figure 35: **Delay Factor at Various Capacitive Loads**

Table 18: **Pin Descriptions *(Continued)***

Pin Name	I/O During Config.	I/O After Config.	Pin Description
$\overline{\text{PWRDWN}}$	I	I	$\overline{\text{PWRDWN}}$ is an active Low input that forces the FPGA into the Power Down state and reduces power consumption. When $\overline{\text{PWRDWN}}$ is Low, the FPGA disables all I/O and initializes all flip-flops. All inputs are interpreted as Low independent of their actual level. VCC must be maintained, and the configuration data is maintained. $\overline{\text{PWRDWN}}$ halts configuration if asserted before or during configuration, and re-starts configuration when removed. When $\overline{\text{PWRDWN}}$ returns High, the FPGA becomes operational by first enabling the inputs and flip-flops and then enabling the outputs. $\overline{\text{PWRDWN}}$ has a default internal pull-up resistor.
User I/O Pins That Can Have Special Functions			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ to 10 kΩ external pull-up resistor is recommended. As an active Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.

Table 18: **Pin Descriptions *(Continued)***

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
VCC	P33	P25	N1	P37	-
Not Connect-ed[1] PWRDWN[2]	P34	P26	N2	P38	174 [1]
I/O, PGCK2[1] GCK3[2]	P35	P27	M3	P39	175[3]
I/O (HDC)	P36	P28	N3	P40	178 [3]
I/O	-	-	K4	P41	181 [3]
I/O	-	-	L4	P42	184 [3]
I/O	-	P29	M4	P43	187 [3]
I/O ($\overline{LDC}$)	P37	P30	N4	P44	190 [3]
GND	-	-	K5	P45	-
I/O	-	-	L5	P46	193 [3]
I/O	-	-	M5	P47	196 [3]
I/O	P38	P31	N5	P48	199 [3]
I/O	P39	P32	K6	P49	202 [3]
I/O	-	P33	L6	P50	205 [3]
I/O	-	P34	M6	P51	208 [3]
I/O	P40	P35	N6	P52	211 [3]
I/O ($\overline{INIT}$)	P41	P36	M7	P53	214 [3]
VCC	P42	P37	N7	P54	-
GND	P43	P38	L7	P55	-
I/O	P44	P39	K7	P56	217 [3]
I/O	P45	P40	N8	P57	220 [3]
I/O	-	P41	M8	P58	223 [3]
I/O	-	P42	L8	P59	226 [3]
I/O	P46	P43	K8	P60	229 [3]
I/O	P47	P44	N9	P61	232 [3]
I/O	-	-	M9	P62	235 [3]
I/O	-	-	L9	P63	238 [3]
GND	-	-	K9	P64	-
I/O	P48	P45	N10	P65	241 [3]
I/O	P49	P46	M10	P66	244 [3]
I/O	-	-	L10	P67	247 [3]
I/O	-	-	N11	P68	250 [3]
I/O	P50	P47	M11	P69	253 [3]
I/O, SGCK3[1] GCK4[2]	P51	P48	L11	P70	256 [3]
GND	P52	P49	N12	P71	-
DONE	P53	P50	M12	P72	-
VCC	P54	P51	N13	P73	-
$\overline{PROGRAM}$	P55	P52	M13	P74	-
I/O (D7[2])	P56	P53	L12	P75	259 [3]

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O, PGCK3[1] GCK5[2]	P57	P54	L13	P76	262 [3]
I/O	-	-	K10	P77	265 [3]
I/O	-	-	K11	P78	268 [3]
I/O (D6[2])	P58	P55	K12	P79	271 [3]
I/O	-	P56	K13	P80	274 [3]
GND	-	-	J10	P81	-
I/O	-	-	J11	P82	277 [3]
I/O	-	-	J12	P83	280 [3]
I/O (D5[2])	P59	P57	J13	P84	283 [3]
I/O	P60	P58	H10	P85	286 [3]
I/O	-	P59	H11	P86	289 [3]
I/O	-	P60	H12	P87	292 [3]
I/O (D4[2])	P61	P61	H13	P88	295 [3]
I/O	P62	P62	G12	P89	298 [3]
VCC	P63	P63	G13	P90	-
GND	P64	P64	G11	P91	-
I/O (D3[2])	P65	P65	G10	P92	301 [3]
I/O	P66	P66	F13	P93	304 [3]
I/O	-	P67	F12	P94	307 [3]
I/O	-	-	F11	P95	310 [3]
I/O (D2[2])	P67	P68	F10	P96	313 [3]
I/O	P68	P69	E13	P97	316 [3]
I/O	-	-	E12	P98	319 [3]
I/O	-	-	E11	P99	322 [3]
GND	-	-	E10	P100	-
I/O (D1[2])	P69	P70	D13	P101	325 [3]
I/O	P70	P71	D12	P102	328 [3]
I/O	-	-	D11	P103	331 [3]
I/O	-	-	C13	P104	334 [3]
I/O (D0[2], DIN)	P71	P72	C12	P105	337 [3]
I/O, SGCK4[1] GCK6[2] (DOUT)	P72	P73	C11	P106	340 [3]
CCLK	P73	P74	B13	P107	-
VCC	P74	P75	B12	P108	-
O, TDO	P75	P76	A13	P109	0
GND	P76	P77	A12	P110	-
I/O	P77	P78	B11	P111	2
I/O, PGCK4[1] GCK7[2]	P78	P79	A11	P112	5
I/O	-	-	D10	P113	8
I/O	-	-	C10	P114	11
I/O (CS1[2])	P79	P80	B10	P115	14

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC[2]	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2[1], GCK2[2]	P21	L2	P33	P49	239
Not Connected[1] M1[2]	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE[1], M0[2]	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected[1] $\overline{\text{PWRDWN}}$[2]	P26	N2	P38	P54	246 [1]
I/O, PGCK2[1], GCK3[2]	P27	M3	P39	P55	247 [3]
I/O (HDC)	P28	N3	P40	P56	250 [3]
I/O	-	K4	P41	P57	253 [3]
I/O	-	L4	P42	P58	256 [3]
I/O	P29	M4	P43	P59	259 [3]

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O ($\overline{\text{LDC}}$)	P30	N4	P44	P60	262 [3]
I/O	-	-	-	P61	265 [3]
I/O	-	-	-	P62	268 [3]
I/O	-	-	-	P63	271 [3]
I/O	-	-	-	P64	274 [3]
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 [3]
I/O	-	M5	P47	P68	280 [3]
I/O	P31	N5	P48	P69	283 [3]
I/O	P32	K6	P49	P70	286 [3]
VCC[2]	-	-	-	P71	-
I/O	-	-	-	P72	289 [3]
I/O	-	-	-	P73	292 [3]
I/O	P33	L6	P50	P74	295 [3]
I/O	P34	M6	P51	P75	298 [3]
I/O	P35	N6	P52	P76	301 [3]
I/O ($\overline{\text{INIT}}$)	P36	M7	P53	P77	304 [3]
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 [3]
I/O	P40	N8	P57	P81	310 [3]
I/O	P41	M8	P58	P82	313 [3]
I/O	P42	L8	P59	P83	316 [3]
I/O	-	-	-	P84	319 [3]
I/O	-	-	-	P85	322 [3]
VCC[2]	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 [3]
I/O	P44	N9	P61	P88	328 [3]
I/O	-	M9	P62	P89	331 [3]
I/O	-	L9	P63	P90	334 [3]
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 [3]
I/O	-	-	-	P94	340 [3]
I/O	-	-	-	P95	343 [3]
I/O	-	-	-	P96	346 [3]
I/O	P45	N10	P65	P97	349 [3]
I/O	P46	M10	P66	P98	352 [3]
I/O	-	L10	P67	P99	355 [3]
I/O	-	N11	P68	P100	358 [3]
I/O	P47	M11	P69	P101	361 [3]
I/O, SGCK3[1], GCK4[2]	P48	L11	P70	P102	364 [3]
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 (1)	P33 (1)	P39	P65	P71 (1)
P86 (1)	P92	P111	P121(1)	P140(1)	P144
P165	P173(1)	P192(1)	P202	P203	-
9/16/98					

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by PDN2004-01

XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100(5)	TQ144	PQ208	PQ240	BG256(5)	CS280(2,5)	Bndry Scan
VCC	P89	P128	P183	P212	VCC(4)	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC(4)	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND(4)	GND(4)	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1(1), GCK8(2)	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC(4)	A1	-
GND	P1	P1	P1	P1	GND(4)	GND(4)	-
I/O, PGCK1(1), GCK1(2)	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: **Component Availability Chart for Spartan/XL FPGAs**

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84(3)	VQ100(3)	CS144(3)	TQ144	PQ208	PQ240	BG256(3)	CS280(3)
XCS05	-3	C(3)	C, I	-	-	-	-	-	-
	-4	C(3)	C	-	-	-	-	-	-
XCS10	-3	C(3)	C, I	-	C	-	-	-	-
	-4	C(3)	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C(3)	-	C, I	C, I	C	C(3)	-
	-4	-	C(3)	-	C	C	C	C(3)	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C(3)	C, I	-	-	-	-	-	-
	-5	C(3)	C	-	-	-	-	-	-
XCS10XL	-4	C(3)	C, I	C(3)	C	-	-	-	-
	-5	C(3)	C	C(3)	C	-	-	-	-
XCS20XL	-4	-	C, I	C(3)	C, I	C, I	-	-	-
	-5	-	C	C(3)	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C(3)
	-5	-	C	-	C	C	C	C	C(3)
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C(3)
	-5	-	-	-	-	C	C	C	C(3)

6/25/08

Notes:

1. C = Commercial T_J = 0° to +85°C
2. I = Industrial T_J = –40°C to +100°C
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

www.xilinx.com/support/documentation/spartan-xl.htm#19687

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

www.xilinx.com/cgi-bin/thermal/thermal.pl

Revision History

The following table shows the revision history for this document.

Date	Version	Description
11/20/98	1.3	Added Spartan-XL specs and Power Down.
01/06/99	1.4	All Spartan-XL -4 specs designated Preliminary with no changes.
03/02/00	1.5	Added CS package, updated Spartan-XL specs to Final.
09/19/01	1.6	Reformatted, updated power specs, clarified configuration information. Removed T_{SOL} soldering information from Absolute Maximum Ratings table. Changed Figure 26: Slave Serial Mode Characteristics: T_{CCH}, T_{CCL} from 45 to 40 ns. Changed Master Mode Configuration Switching Characteristics: T_{CCLK} min. from 80 to 100 ns. Added Total Dist. RAM Bits to Table 1; added **Start-Up**, page 36 characteristics.
06/27/02	1.7	Clarified Express Mode pseudo daisy chain. Added new Industrial options. Clarified XCS30XL CS280 V_{CC} pinout.
06/26/08	1.8	Noted that PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, are discontinued by **PDN2004-01**. Extended description of recommended maximum delay of reconfiguration in **Delaying Configuration After Power-Up**, page 35. Added reference to Pb-free package options and provided link to **Package Specifications**, page 81. Updated links.
03/01/13	2.0	The products listed in this data sheet are obsolete. See **XCN10016** and **XCN11010** for further information.