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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	466
Total RAM Bits	6272
Number of I/O	61
Number of Gates	10000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs10-4pc84c

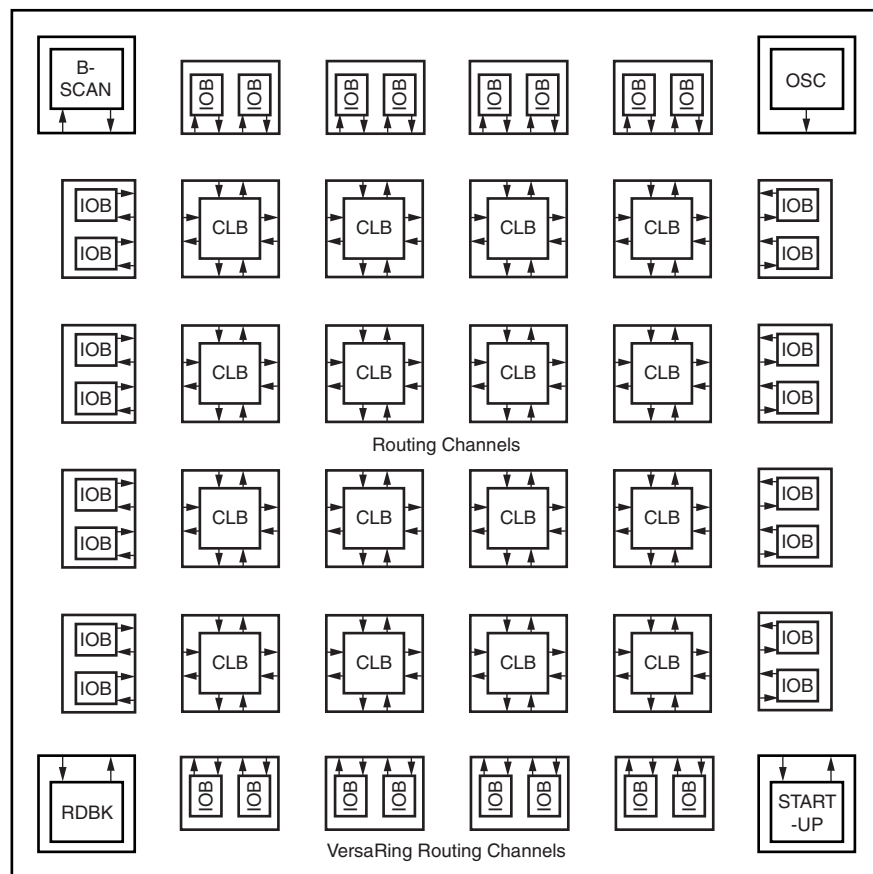
General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in **Figure 1**. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these

memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.



DS060_01_081100

Figure 1: Basic FPGA Block Diagram

Spartan and Spartan-XL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In addition to the conventional benefit of high volume programmable logic solutions, Spartan series FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan/XL families leverage the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA process developments.

Logic Functional Description

The Spartan series uses a standard FPGA structure as shown in [Figure 1, page 2](#). The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in [Figure 2](#). There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the [Advanced Features Description, page 13](#).

Function Generators

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box "A" of [Figure 2](#)). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

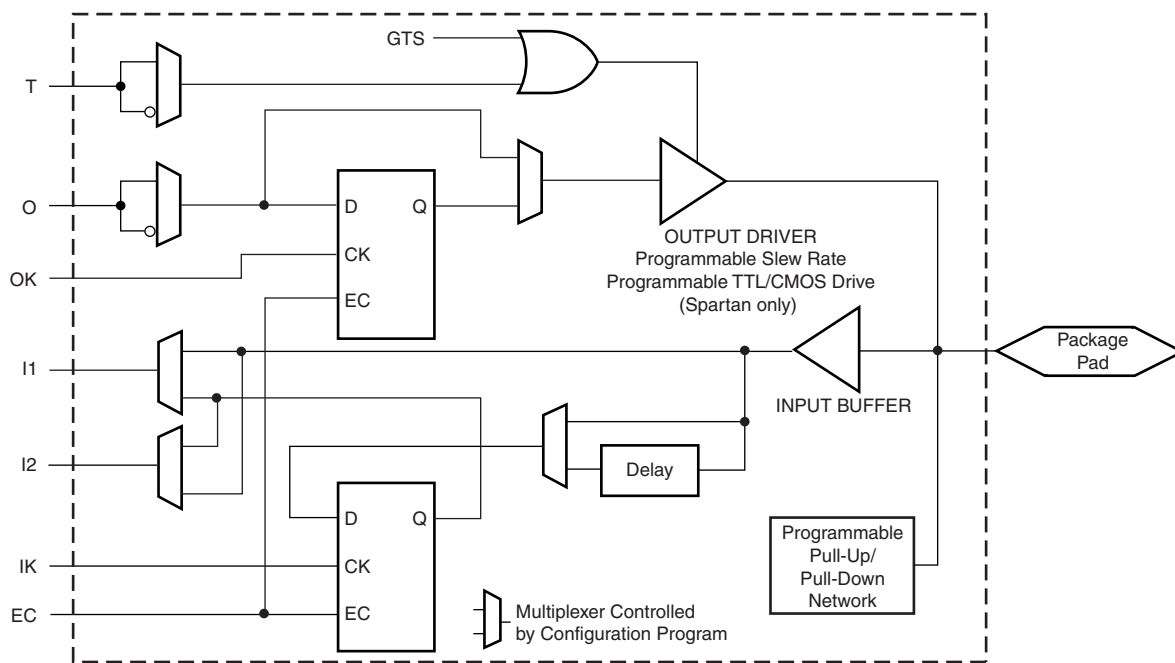
The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop. The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds,

using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.



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Figure 6: Simplified Spartan/XL IOB Block Diagram

- The 16 x 1 single-port configuration contains a RAM array with 16 locations, each one-bit wide. One 4-bit address decoder determines the RAM location for write and read operations. There is one input for writing data and one output for reading data, all at the selected address.
- The (16 x 1) x 2 single-port configuration combines two 16 x 1 single-port configurations (each according to the preceding description). There is one data input, one data output and one address decoder for each array. These arrays can be addressed independently.
- The 32 x 1 single-port configuration contains a RAM array with 32 locations, each one-bit wide. There is one data input, one data output, and one 5-bit address decoder.
- The dual-port mode 16 x 1 configuration contains a RAM array with 16 locations, each one-bit wide. There are two 4-bit address decoders, one for each port. One port consists of an input for writing and an output for reading, all at a selected address. The other port consists of one output for reading from an independently selected address.

The appropriate choice of RAM configuration mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Selection criteria include the following: Whereas the 32 x 1 single-port, the (16 x 1) x 2 single-port, and the 16 x 1 dual-port configurations each use one entire CLB, the 16 x 1 single-port configuration uses only one half of a CLB. Due to its simultaneous read/write capability, the dual-port RAM can transfer twice as much data as the single-port RAM, which permits only one data operation at any given time.

CLB memory configuration options are selected by using the appropriate library symbol in the design entry.

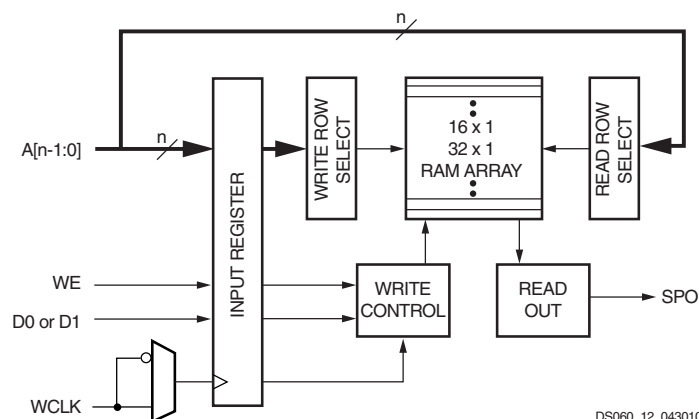
Single-Port Mode

There are three CLB memory configurations for the single-port RAM: 16 x 1, (16 x 1) x 2, and 32 x 1, the functional organization of which is shown in [Figure 12](#).

The single-port RAM signals and the CLB signals ([Figure 2](#), [page 4](#)) from which they are originally derived are shown in [Table 9](#).

Table 9: Single-Port RAM Signals

RAM Signal	Function	CLB Signal
D0 or D1	Data In	DIN or H1
A[3:0]	Address	F[4:1] or G[4:1]
A4 (32 x 1 only)	Address	H1
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (Data Out)	F _{OUT} or G _{OUT}



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Notes:

1. The (16 x 1) x 2 configuration combines two 16 x 1 single-port RAMs, each with its own independent address bus and data input. The same WE and WCLK signals are connected to both RAMs.
2. n = 4 for the 16 x 1 and (16 x 1) x 2 configurations. n = 5 for the 32 x 1 configuration.

Figure 12: Logic Diagram for the Single-Port RAM

Writing data to the single-port RAM is essentially the same as writing to a data register. It is an edge-triggered (synchronous) operation performed by applying an address to the A inputs and data to the D input during the active edge of WCLK while WE is High.

The timing relationships are shown in [Figure 13](#). The High logic level on WE enables the input data register for writing. The active edge of WCLK latches the address, input data, and WE signals. Then, an internal write pulse is generated that loads the data into the memory cell.

and Spartan-XL families, speeding up arithmetic and counting functions.

The carry chain in 5V Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in Spartan-XL devices can only run up the column, providing even higher speed.

Figure 16, page 18 shows a Spartan/XL FPGA CLB with dedicated fast carry logic. The carry logic shares operand

and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 17, page 19 shows the details of the Spartan/XL FPGA carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 16.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

Even if the boundary scan symbol is used in a design, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state.
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "Boundary Scan in FPGA Devices."

Boundary Scan Enhancements (Spartan-XL Family Only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

IDCODE: The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

- c = the company code (49h for Xilinx)
- a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)
- f = the family code (02h for Spartan-XL family)
- v = the die version number

Table 13: IDCODEs Assigned to Spartan-XL FPGAs

FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

Configuration State: The configuration state is available to JTAG controllers.

Configuration Disable: The JTAG port can be prevented from configuring the FPGA.

TCK Startup: TCK can now be used to clock the start-up block in addition to other user clocks.

CCLK Holdoff: Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

Reissue Configure: The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

Bypass FF: Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

Power-Down (Spartan-XL Family Only)

All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low power-down pin (PWRDWN) to reduce supply current to 100 μ A typical. The PWRDWN pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The PWRDWN pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

V_{CC} must continue to be supplied during Power-down, and configuration data is maintained. When the PWRDWN pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The PROGRAM pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

PWRDWN has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before PWRDWN to affect the order of events. When the PWRDWN signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of PWRDWN before using the device.

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

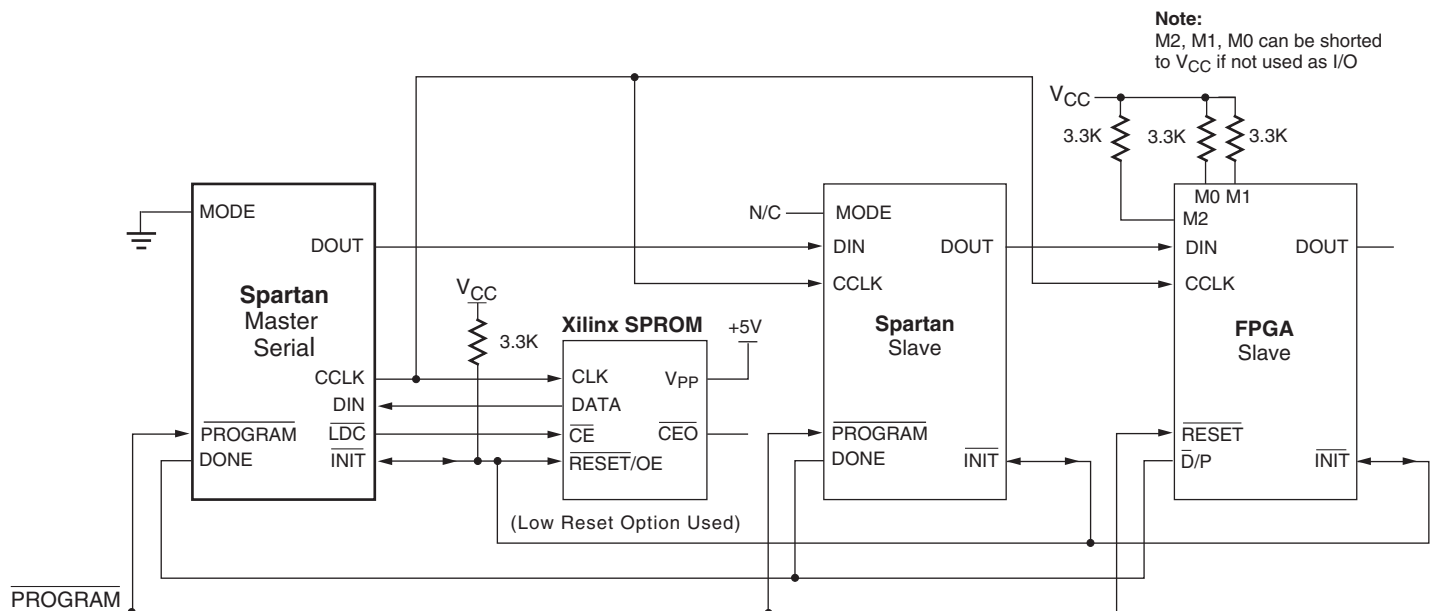
Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through

and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

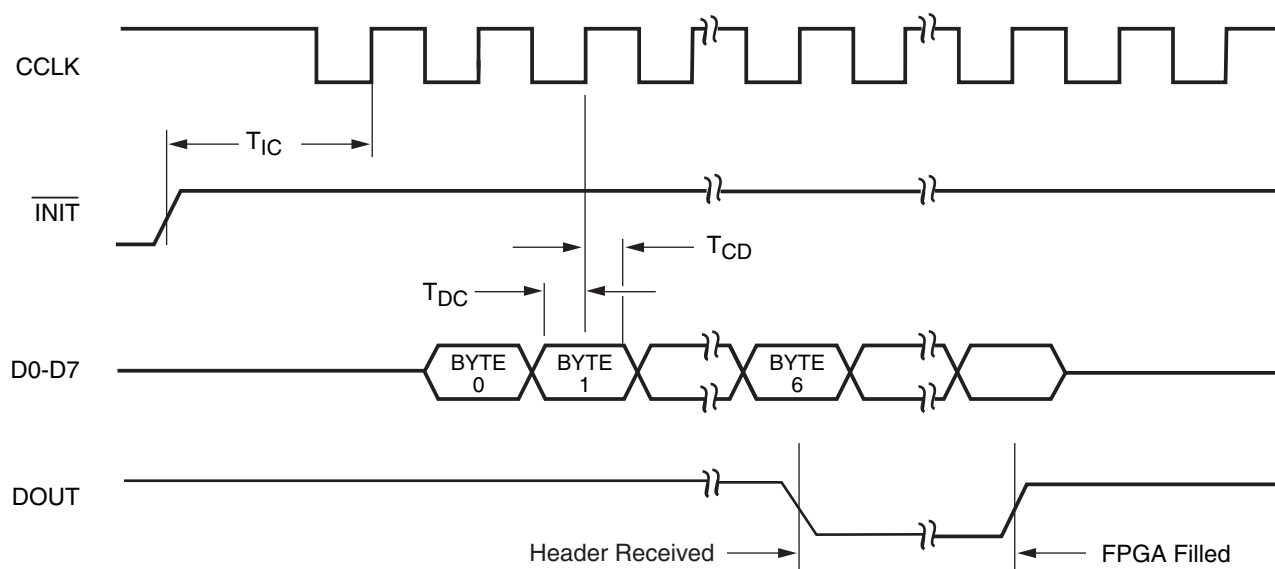
After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.



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Figure 25: Master/Slave Serial Mode Circuit Diagram



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Symbol		Description	Min	Max	Units
T_{IC}	CCLK	\overline{INIT} (High) setup time	5	-	μs
T_{DC}		D0-D7 setup time	20	-	ns
T_{CD}		D0-D7 hold time	0	-	ns
T_{CCH}		CCLK High time	45	-	ns
T_{CCL}		CCLK Low time	45	-	ns
F_{CC}		CCLK Frequency	-	10	MHz

Notes:

1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: Express Mode Programming Switching Characteristics

Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right.

Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

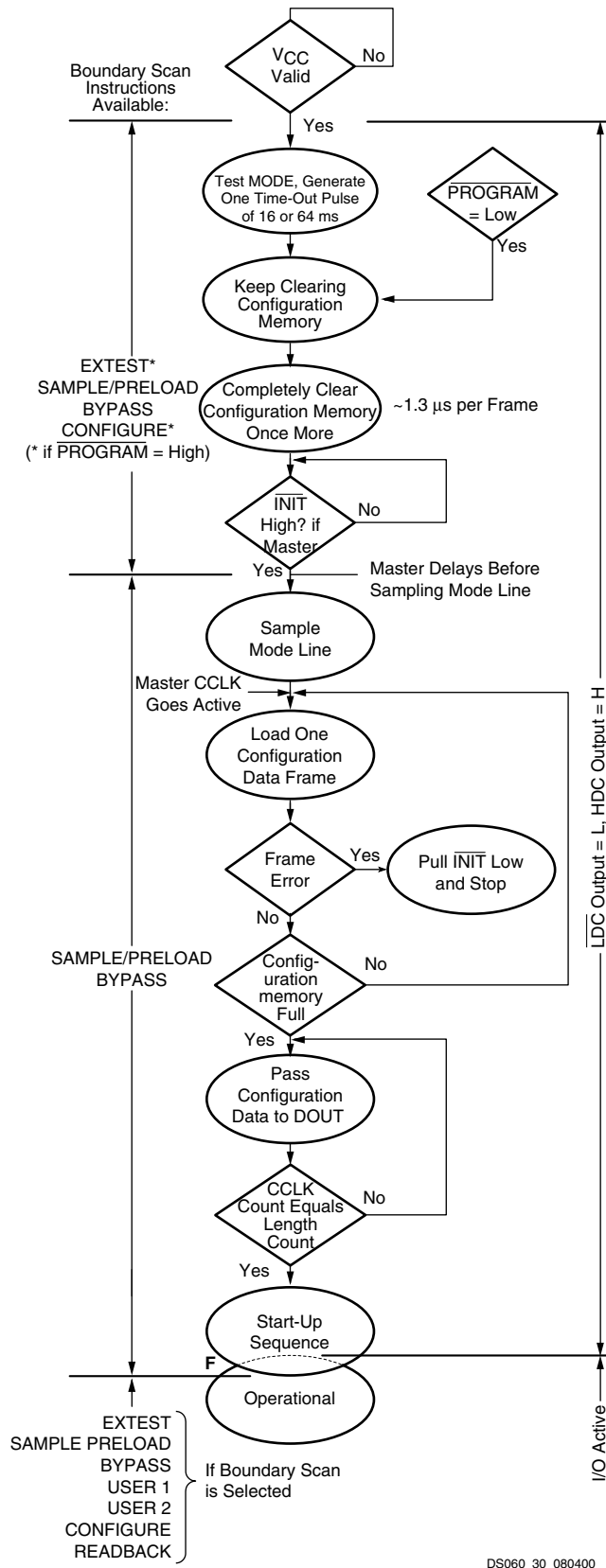


Figure 30: Power-up Configuration Sequence

Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count for serial modes. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Spartan-XL family Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{\text{INIT}}$ pin Low. After all configuration frames have been loaded into an FPGA using a serial mode, DOUT again follows the input data so that the remaining data is passed on to the next device. In Spartan-XL family Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See Figure 30.)

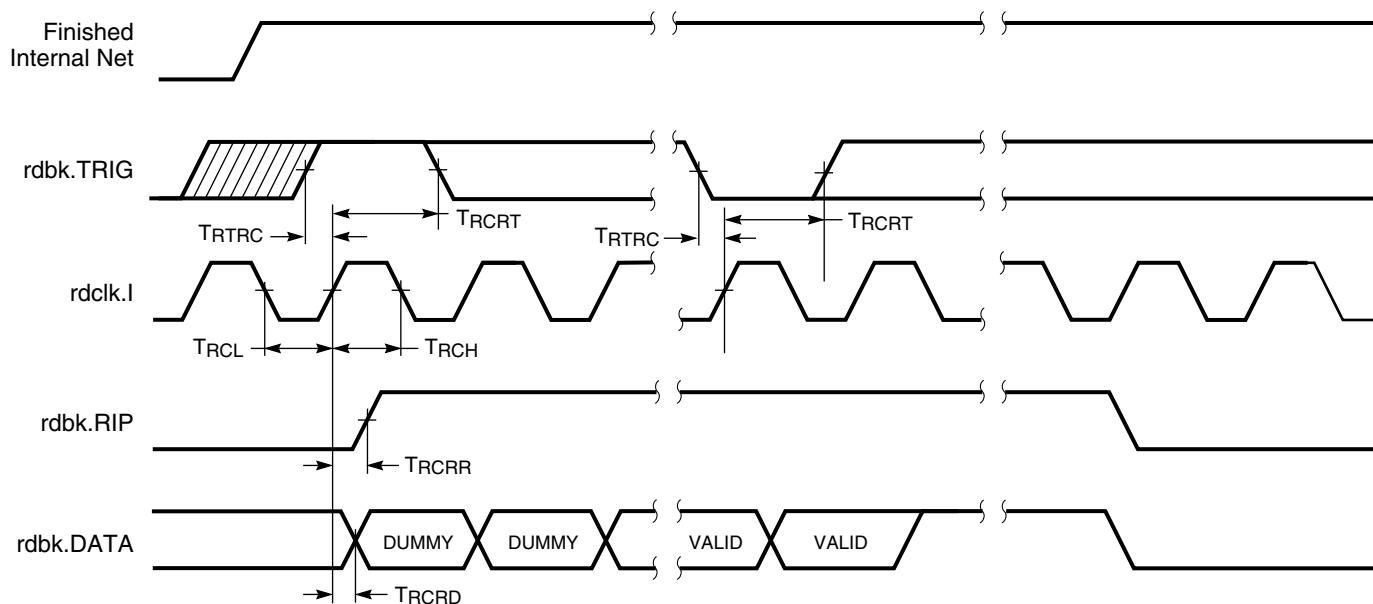
A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the FPGA keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the $\overline{\text{INIT}}$ input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output. The Spartan/XL FPGA $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up.

Avoid holding $\overline{\text{PROGRAM}}$ Low for more than 500 μs . The 500 μs maximum limit is only a recommendation, not a requirement. The only effect of holding $\overline{\text{PROGRAM}}$ Low for more than 500 μs is an increase in current, measured at about 40 mA in the XCS40XL. This increased current cannot damage the device. This applies only during reconfiguration, not during power-up. The $\overline{\text{INIT}}$ pin can also be held Low to delay reconfiguration, and the same characteristics apply as for the $\overline{\text{PROGRAM}}$ pin.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration causes the FPGA

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.



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Figure 33: Spartan and Spartan-XL Readback Timing Diagram

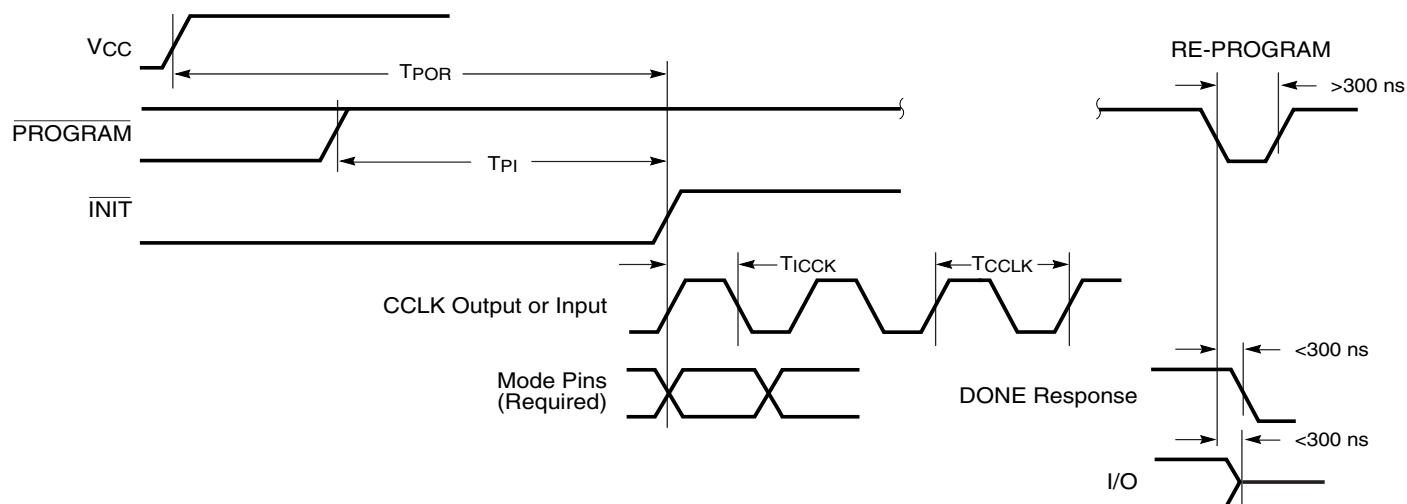
Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:

1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Configuration Switching Characteristics



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Master Mode

Symbol	Description	Min	Max	Units
T _{POR}	Power-on reset	40	130	ms
T _{PI}	Program Latency	30	200	μs per CLB column
T _{IOCK}	CCLK (output) delay	40	250	μs
T _{CCLK}	CCLK (output) period, slow	640	2000	ns
T _{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Max	Units
T _{POR}	Power-on reset	10	33	ms
T _{PI}	Program latency	30	200	μs per CLB column
T _{ICCK}	CCLK (input) delay (required)	4	-	μs
T _{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

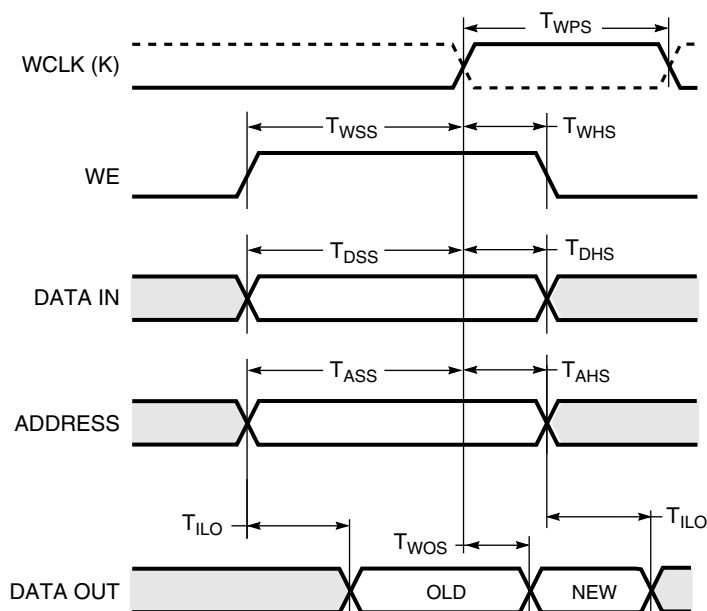
Symbol	Dual Port RAM	Size ⁽¹⁾	-4		-3		Units
			Min	Max	Min	Max	
Write Operation							
T _{WCDS}	Address write cycle time (clock K period)	16x1	8.0	-	11.6	-	ns
T _{WPDS}	Clock K pulse width (active edge)	16x1	4.0	-	5.8	-	ns
T _{ASDS}	Address setup time before clock K	16x1	1.5	-	2.1	-	ns
T _{AHDS}	Address hold time after clock K	16x1	0	-	0	-	ns
T _{DSDS}	DIN setup time before clock K	16x1	1.5	-	1.6	-	ns
T _{DHDS}	DIN hold time after clock K	16x1	0	-	0	-	ns
T _{WSDS}	WE setup time before clock K	16x1	1.5	-	1.6	-	ns
T _{WHDS}	WE hold time after clock K	16x1	0	-	0	-	ns
T _{WODS}	Data valid after clock K	16x1	-	6.5	-	7.0	ns

Notes:

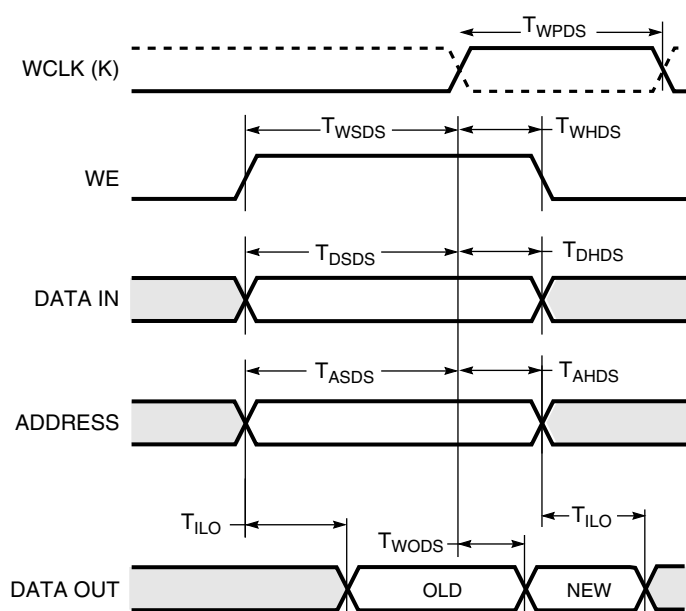
- Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



DS060_34_011300

Spartan Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to

the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Clocks							
T _{CH}	Clock High	All devices	3.0	-	4.0	-	ns
T _{CL}	Clock Low	All devices	3.0	-	4.0	-	ns
Propagation Delays - TTL Outputs ^(1,2)							
T _{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.3	-	4.5	ns
T _{OKPOS}	Clock (OK to Pad, slew-rate limited	All devices	-	6.9	-	7.0	ns
T _{OPF}	Output (O) to Pad, fast	All devices	-	3.6	-	4.8	ns
T _{OPS}	Output (O) to Pad, slew-rate limited	All devices	-	7.2	-	7.3	ns
T _{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	3.0	-	3.8	ns
T _{TSONF}	3-state to Pad active and valid, fast	All devices	-	6.0	-	7.3	ns
T _{TSONS}	3-state to Pad active and valid, slew-rate limited	All devices	-	9.6	-	9.8	ns
Setup and Hold Times							
T _{OOK}	Output (O) to clock (OK) setup time	All devices	2.5	-	3.8	-	ns
T _{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T _{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	2.0	-	2.7	-	ns
T _{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.0	-	0.5	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	11.5		13.5		ns
T _{RPO}	Delay from GSR input to any Pad	XCS05	-	12.0	-	15.0	ns
		XCS10	-	12.5	-	15.7	ns
		XCS20	-	13.0	-	16.2	ns
		XCS30	-	13.5	-	16.9	ns
		XCS40	-	14.0	-	17.5	ns

Notes:

1. Delay adder for CMOS Outputs option (with fast slew rate option): for -3 speed grade, add 1.0 ns; for -4 speed grade, add 0.8 ns.
2. Delay adder for CMOS Outputs option (with slow slew rate option): for -3 speed grade, add 2.0 ns; for -4 speed grade, add 1.5 ns.
3. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
4. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings⁽¹⁾

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		−0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked ^(2, 3)	−0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	−0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked ^(2, 3)	−0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	−0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)		−65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to −2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to −2.0V or overshoot to $V_{CC} + 2.0V$, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ ⁽¹⁾	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage ⁽²⁾		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage ⁽²⁾		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:

- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement threshold is ~50% of V_{CC} .

Spartan-XL Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For

more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
T_{GLS}	From pad through buffer, to any clock K	XCS05XL	1.4	1.5	ns
		XCS10XL	1.7	1.8	ns
		XCS20XL	2.0	2.1	ns
		XCS30XL	2.3	2.5	ns
		XCS40XL	2.6	2.8	ns

Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Setup and Hold

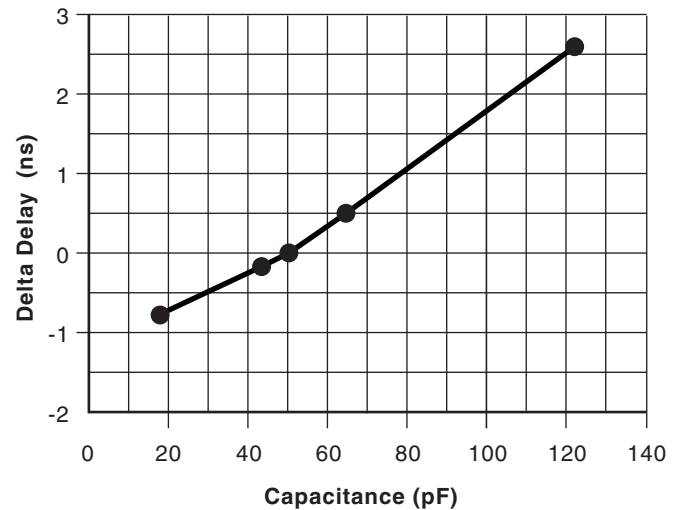
Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Input Setup/Hold Times Using Global Clock and IFF					
T _{SUF} /T _{HF}	No Delay	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
T _{SU} /T _H	Full Delay	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



DS060_35_080400

Figure 35: Delay Factor at Various Capacitive Loads

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	<p>Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin.</p> <p>The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.</p>
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	<p>Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin.</p> <p>The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.</p>
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	<p>During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input.</p> <p>In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices.</p> <p>After configuration, DOUT is a user-programmable I/O pin.</p>
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	P124	P144	M20	L19	493 ⁽³⁾
I/O	-	-	P125	P145	L19	L18	496 ⁽³⁾
I/O	P59	P86	P126	P146	L18	L17	499 ⁽³⁾
I/O	P60	P87	P127	P147	L20	L16	502 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	P88	P128	P148	K20	K19	505 ⁽³⁾
I/O	P62	P89	P129	P149	K19	K18	508 ⁽³⁾
VCC	P63	P90	P130	P150	VCC ⁽⁴⁾	K17	-
GND	P64	P91	P131	P151	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O (D3 ⁽²⁾)	P65	P92	P132	P152	K18	K16	511 ⁽³⁾
I/O	P66	P93	P133	P153	K17	K15	514 ⁽³⁾
I/O	P67	P94	P134	P154	J20	J19	517 ⁽³⁾
I/O	-	P95	P135	P155	J19	J18	520 ⁽³⁾
I/O	-	-	P136	P156	J18	J17	523 ⁽³⁾
I/O	-	-	P137	P157	J17	J16	526 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	P96	P138	P159	H19	H17	529 ⁽³⁾
I/O	P69	P97	P139	P160	H18	H16	532 ⁽³⁾
VCC	-	-	P140	P161	VCC ⁽⁴⁾	G19	-
I/O	-	P98	P141	P162	G19	G18	535 ⁽³⁾
I/O	-	P99	P142	P163	F20	G17	538 ⁽³⁾
I/O	-	-	-	P164	G18	G16	541 ⁽³⁾
I/O	-	-	-	P165	F19	F19	544 ⁽³⁾
GND	-	P100	P143	P166	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P167	F18	F18	547 ⁽³⁾
I/O	-	-	P144	P168	E19	F17	550 ⁽³⁾
I/O	-	-	P145	P169	D20	F16	553 ⁽³⁾
I/O	-	-	P146	P170	E18	F15	556 ⁽³⁾
I/O	-	-	P147	P171	D19	E19	559 ⁽³⁾
I/O	-	-	P148	P172	C20	E17	562 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	P101	P149	P173	E17	E16	565 ⁽³⁾
I/O	P71	P102	P150	P174	D18	D19	568 ⁽³⁾
I/O	-	P103	P151	P175	C19	C19	571 ⁽³⁾
I/O	-	P104	P152	P176	B20	B19	574 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	P105	P153	P177	C18	C18	577 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	P106	P154	P178	B19	B18	580 ⁽³⁾
CCLK	P74	P107	P155	P179	A20	A19	-
VCC	P75	P108	P156	P180	VCC ⁽⁴⁾	C17	-
O, TDO	P76	P109	P157	P181	A19	B17	0
GND	P77	P110	P158	P182	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P78	P111	P159	P183	B18	A18	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	P112	P160	P184	B17	A17	5
I/O	-	P113	P161	P185	C17	D16	8
I/O	-	P114	P162	P186	D16	C16	11
I/O (CS1 ⁽²⁾)	P80	P115	P163	P187	A18	B16	14
I/O	P81	P116	P164	P188	A17	A16	17
I/O	-	-	P165	P189	C16	D15	20

CS280

VCC Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-
Not Connected Pins					
A4	A12	C8	C12	C15	D1
D2	D5	D8	D17	D18	E15
H2	H3	H18	H19	L4	M1
M16	M18	R2	R4	R5	R15
R17	T8	T15	U5	V8	V12
W12	W16	-	-	-	-
Not Connected Pins (VCC in XCS40XL)					
B5	B15	E3	E18	R3	R18
V5	V15	-	-	-	-

5/21/02

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
VCC	P183	P212	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P184	P213	C10	D10	86
I/O	P185	P214	D10	E10	89
I/O	P186	P215	A9	A9	92
I/O	P187	P216	B9	B9	95
I/O	P188	P217	C9	C9	98
I/O	P189	P218	D9	D9	101
I/O	P190	P220	A8	A8	104
I/O	P191	P221	B8	B8	107
I/O	-	-	C8	C8	110
I/O	-	-	A7	D8	113
VCC	P192	P222	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	P223	A6	B7	116
I/O	-	P224	C7	C7	119
I/O	P193	P225	B6	D7	122
I/O	P194	P226	A5	A6	125
GND	P195	P227	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P196	P228	C6	B6	128
I/O	P197	P229	B5	C6	131
I/O	P198	P230	A4	D6	134
I/O	P199	P231	C5	E6	137

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
I/O	P200	P232	B4	A5	140
I/O	P201	P233	A3	C5	143
I/O	-	-	-	D5	146
I/O	-	-	-	A4	149
I/O	P202	P234	D5	B4	152
I/O	P203	P235	C4	C4	155
I/O	P204	P236	B3	A3	158
I/O	P205	P237	B2	A2	161
I/O	P206	P238	A2	B3	164
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P207	P239	C3	B2	167
VCC	P208	P240	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
GND	P1	P1	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	P2	B1	C3	170
I/O	P3	P3	C2	C2	173
I/O	P4	P4	D2	B1	176
I/O	P5	P5	D3	C1	179
I/O, TDI	P6	P6	E4	D4	182
I/O, TCK	P7	P7	C1	D3	185
I/O	-	-	-	D2	188
I/O	-	-	-	D1	191
I/O	P8	P8	D1	E2	194
I/O	P9	P9	E3	E4	197
I/O	P10	P10	E2	E1	200
I/O	P11	P11	E1	F5	203
I/O	P12	P12	F3	F3	206
I/O	-	P13	F2	F2	209
GND	P13	P14	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P14	P15	G3	F4	212
I/O	P15	P16	G2	F1	215
I/O, TMS	P16	P17	G1	G3	218
I/O	P17	P18	H3	G2	221
VCC	P18	P19	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	P20	H2	G4	224
I/O	-	P21	H1	H1	227
I/O	-	-	J4	H3	230
I/O	-	-	J3	H2	233
I/O	P19	P23	J2	H4	236
I/O	P20	P24	J1	J1	239
I/O	P21	P25	K2	J2	242
I/O	P22	P26	K3	J3	245
I/O	P23	P27	K1	J4	248
I/O	P24	P28	L1	K1	251

Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: Component Availability Chart for Spartan/XL FPGAs

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84 ⁽³⁾	VQ100 ⁽³⁾	CS144 ⁽³⁾	TQ144	PQ208	PQ240	BG256 ⁽³⁾	CS280 ⁽³⁾
XCS05	-3	C ⁽³⁾	C, I	-	-	-	-	-	-
	-4	C ⁽³⁾	C	-	-	-	-	-	-
XCS10	-3	C ⁽³⁾	C, I	-	C	-	-	-	-
	-4	C ⁽³⁾	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C ⁽³⁾	-	C, I	C, I	C	C ⁽³⁾	-
	-4	-	C ⁽³⁾	-	C	C	C	C ⁽³⁾	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C ⁽³⁾	C, I	-	-	-	-	-	-
	-5	C ⁽³⁾	C	-	-	-	-	-	-
XCS10XL	-4	C ⁽³⁾	C, I	C ⁽³⁾	C	-	-	-	-
	-5	C ⁽³⁾	C	C ⁽³⁾	C	-	-	-	-
XCS20XL	-4	-	C, I	C ⁽³⁾	C, I	C, I	-	-	-
	-5	-	C	C ⁽³⁾	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C ⁽³⁾
	-5	-	C	-	C	C	C	C	C ⁽³⁾
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C ⁽³⁾
	-5	-	-	-	-	C	C	C	C ⁽³⁾

6/25/08

Notes:

1. C = Commercial $T_J = 0^\circ$ to $+85^\circ\text{C}$
2. I = Industrial $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

www.xilinx.com/support/documentation/spartan-xl.htm#19687

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

www.xilinx.com/cgi-bin/thermal/thermal.pl