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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	466
Total RAM Bits	6272
Number of I/O	77
Number of Gates	10000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcs10-4vq100c">https://www.e-xfl.com/product-detail/xilinx/xcs10-4vq100c</a>

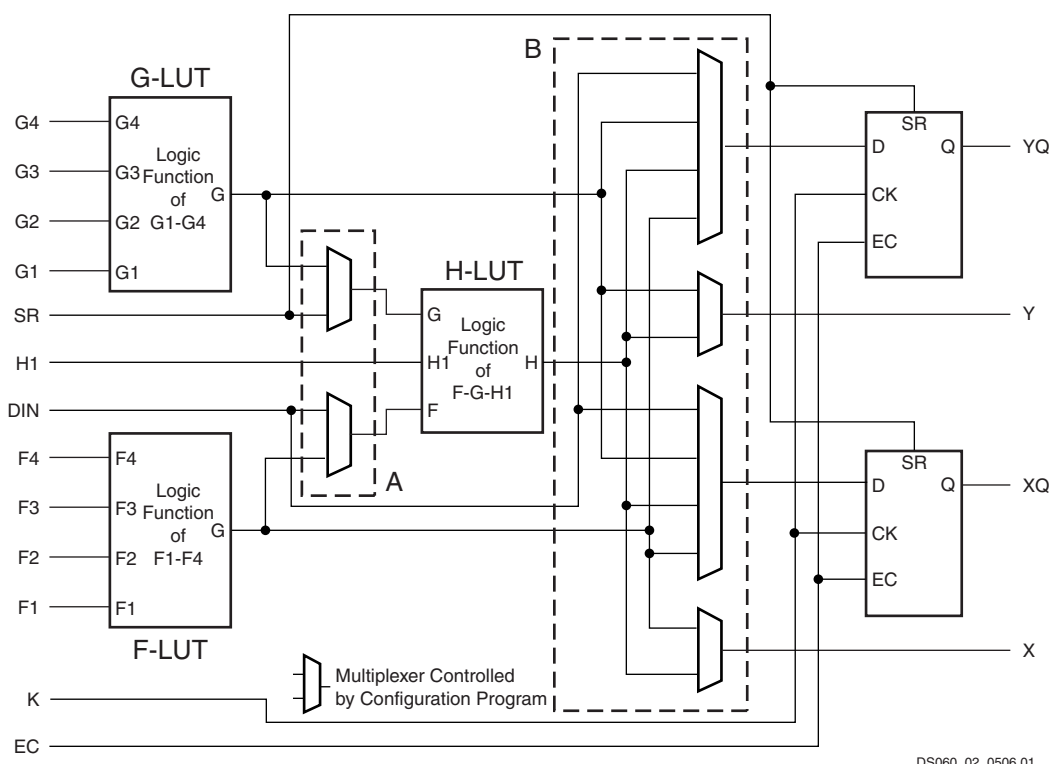


Figure 2: Spartan/XL Simplified CLB Logic Diagram (some features not shown)

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

**Note:** When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

### Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.

### Latches (Spartan-XL Family Only)

The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.

This high value makes them unsuitable as wired-AND pull-up resistors.

**Table 7: Supported Destinations for Spartan/XL Outputs**

Destination	Spartan-XL Outputs	Spartan Outputs	
	3.3V, CMOS	5V, TTL	5V, CMOS
Any device, $V_{CC} = 3.3V$ , CMOS-threshold inputs	✓	✓	Some <sup>(1)</sup>
Any device, $V_{CC} = 5V$ , TTL-threshold inputs	✓	✓	✓
Any device, $V_{CC} = 5V$ , CMOS-threshold inputs	Unreliable Data		✓

**Notes:**

1. Only if destination device has 5V tolerant inputs.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULL-DOWN library component to the net attached to the pad.

### Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops (Figure 5). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

### Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either

falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

### Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (see EC signal in Figure 5), which through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan/XL FPGA CLB. It cannot be inverted within the IOB.

### Routing Channel Description

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

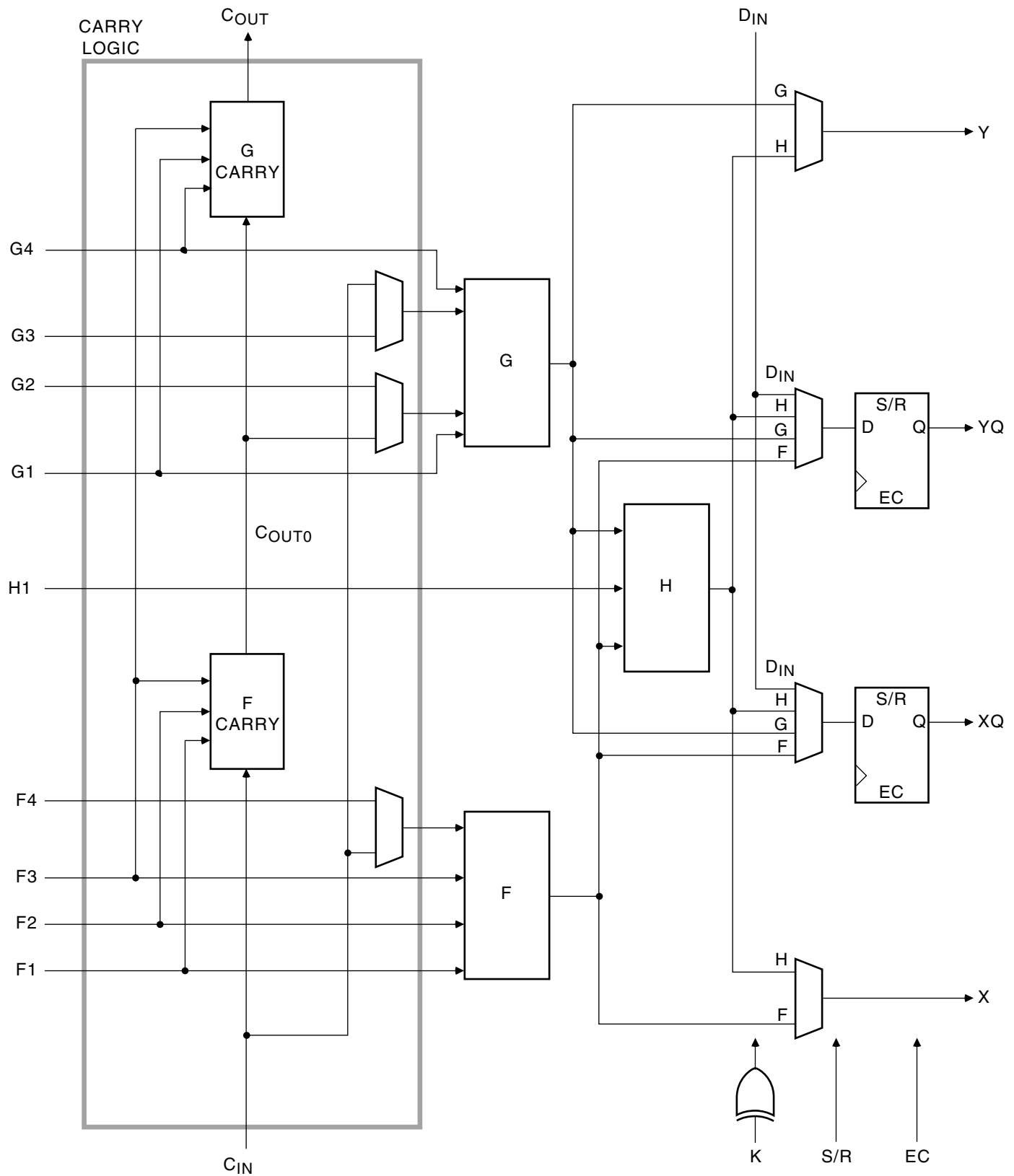
This section describes the routing channels available in Spartan/XL devices. Figure 8 shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the designer should open a design in the FPGA Editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

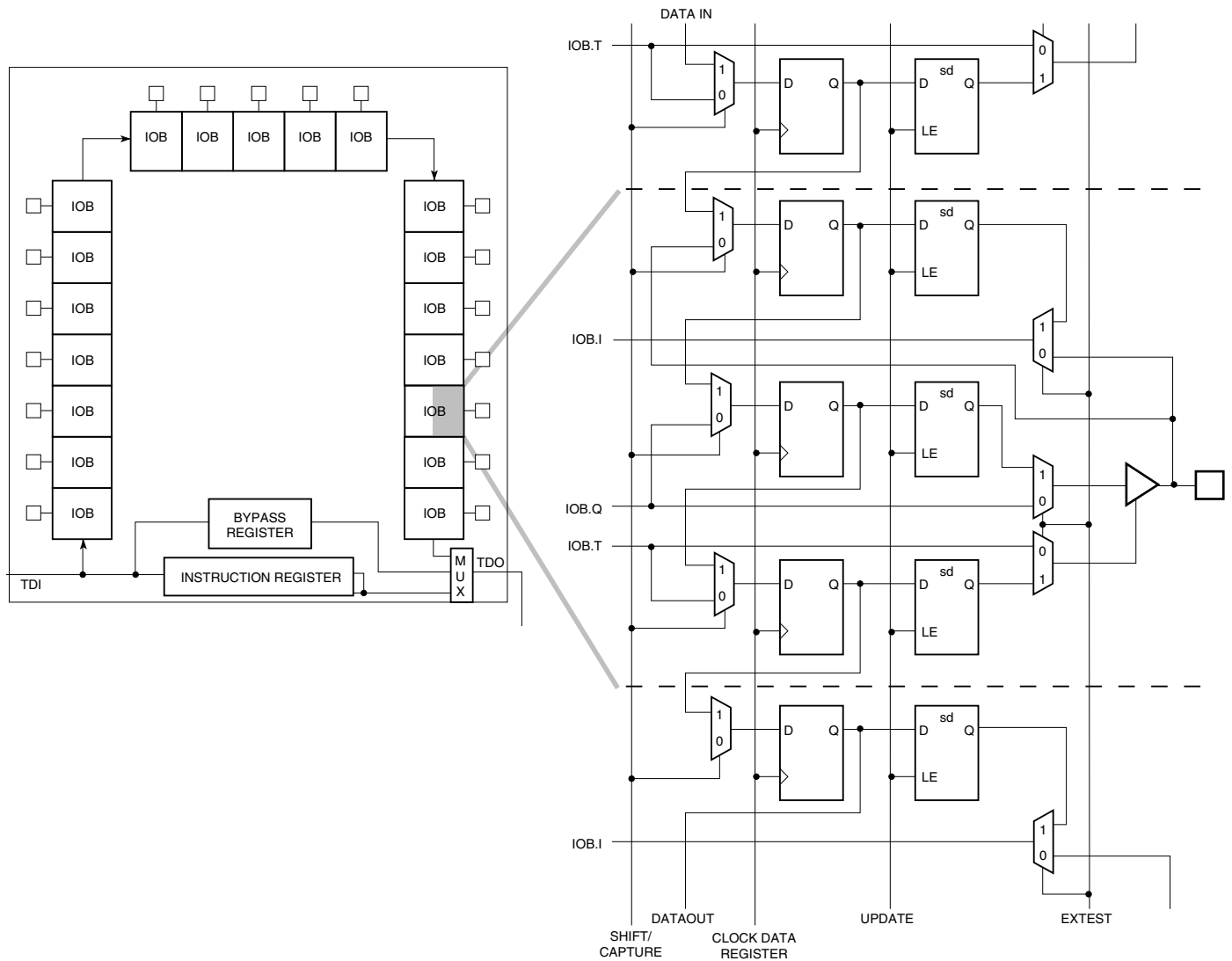
### CLB Routing Channels

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). Figure 8 shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.



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Figure 16: Fast Carry Logic in Spartan/XL CLB



DS060\_20\_080400

Figure 20: Spartan/XL Boundary Scan Logic

figuration are shown in Table 14 and Table 15.

**Table 14: Pin Functions During Configuration (Spartan Family Only)**

Configuration Mode (MODE Pin)		User Operation
Slave Serial (High)	Master Serial (Low)	
MODE (I)	MODE (I)	MODE
HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

**Notes:**

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3.  $\overline{\text{INIT}}$  is an open-drain output during configuration.

**Table 15: Pin Functions During Configuration (Spartan-XL Family Only)**

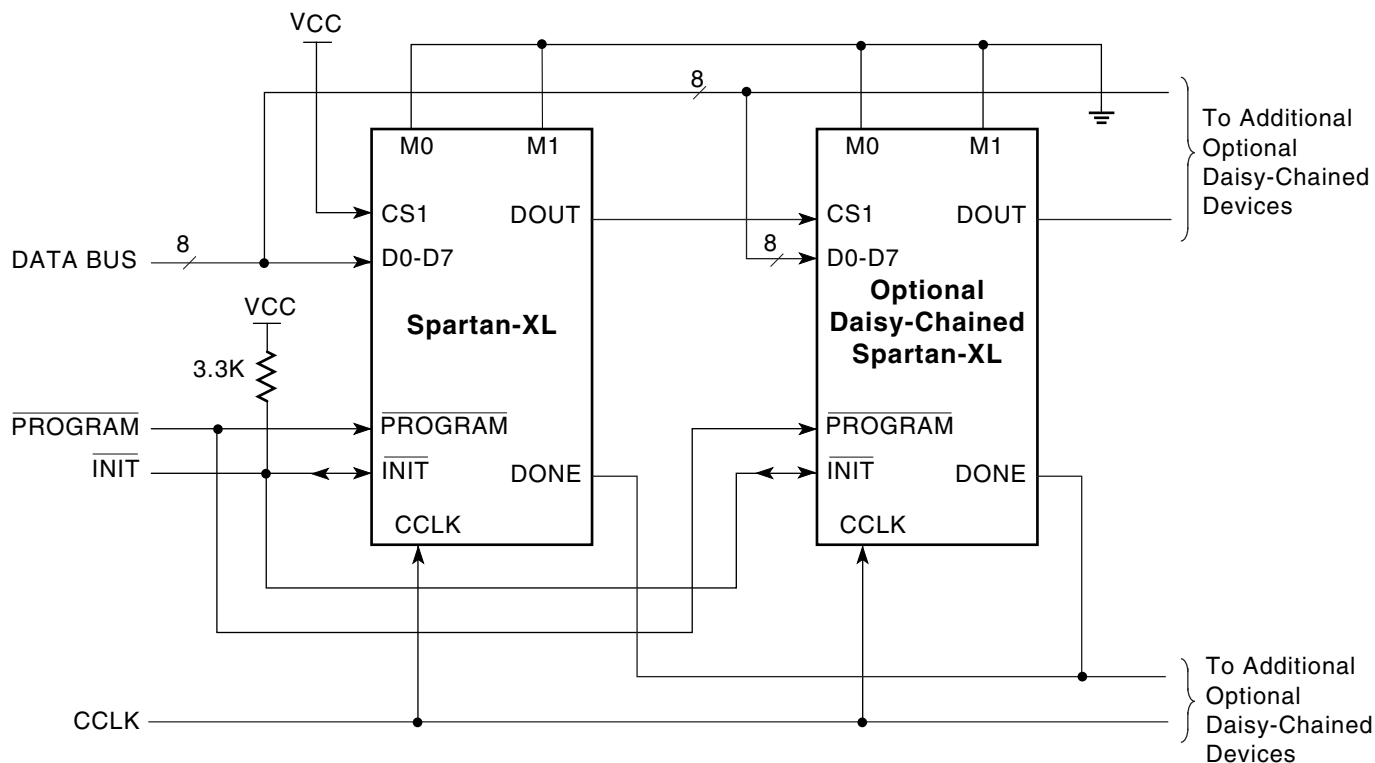
CONFIGURATION MODE <M1:M0>			User Operation
Slave Serial [1:1]	Master Serial [1:0]	Express [0:X]	
M1 (High) (I)	M1 (High) (I)	M1(Low) (I)	M1
M0 (High) (I)	M0 (Low) (I)	M0 (I)	M0
HDC (High)	HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

**Notes:**

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3.  $\overline{\text{INIT}}$  is an open-drain output during configuration.

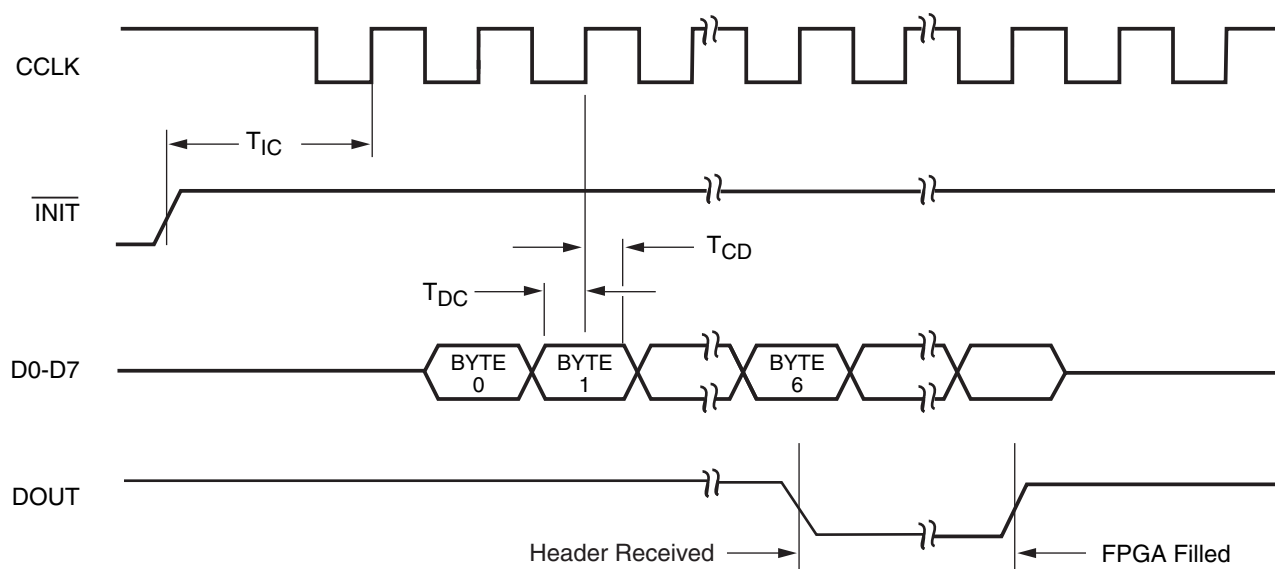
to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device

in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.



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Figure 27: Express Mode Circuit Diagram



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Symbol		Description	Min	Max	Units
$T_{IC}$	CCLK	$\overline{INIT}$ (High) setup time	5	-	$\mu s$
$T_{DC}$		D0-D7 setup time	20	-	ns
$T_{CD}$		D0-D7 hold time	0	-	ns
$T_{CCH}$		CCLK High time	45	-	ns
$T_{CCL}$		CCLK Low time	45	-	ns
$F_{CC}$		CCLK Frequency	-	10	MHz

**Notes:**

1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: Express Mode Programming Switching Characteristics

## Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

## Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right.

Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".



Table 16: Spartan/XL Data Stream Formats

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0] <sup>(1)</sup>
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	11111110b <sup>(2)</sup>
Data Frame	DATA[n-1:0]	DATA[n-1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes <sup>(3)</sup>	FFh	FFFFFFFFFFFFFFh

**Legend:**

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

**Notes:**

1. Not used by configuration logic.
2. 11111111b for XCS40XL only.
3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the  $\overline{\text{INIT}}$  pin. In Master serial mode, CCLK continues to operate externally. The user must detect  $\overline{\text{INIT}}$  and initialize a new configuration by pulsing the PROGRAM pin Low or cycling VCC.

**Cyclic Redundancy Check (CRC) for Configuration and Readback**

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the  $\overline{\text{INIT}}$  pin Low and goes into a Wait state.

Table 17: Spartan/XL Program Data

Device	XCS05		XCS10		XCS20		XCS30		XCS40	
Max System Gates	5,000		10,000		20,000		30,000		40,000	
CLBs (Row x Col.)	100 (10 x 10)		196 (14 x 14)		400 (20 x 20)		576 (24 x 24)		784 (28 x 28)	
I/Os	80		112		160		192		205 <sup>(4)</sup>	
Part Number	XCS05	XCS05XL	XCS10	XCS10XL	XCS20	XCS20XL	XCS30	XCS30XL	XCS40	XCS40XL
Supply Voltage	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V
Bits per Frame	126	127	166	167	226	227	266	267	306	307
Frames	428	429	572	573	788	789	932	933	1,076	1,077
Program Data	53,936	54,491	94,960	95,699	178,096	179,111	247,920	249,119	329,264	330,647
PROM Size (bits)	53,984	54,544	95,008	95,752	178,144	179,160	247,968	249,168	329,312	330,696
Express Mode PROM Size (bits)	-	79,072	-	128,488	-	221,056	-	298,696	-	387,856

### Notes:

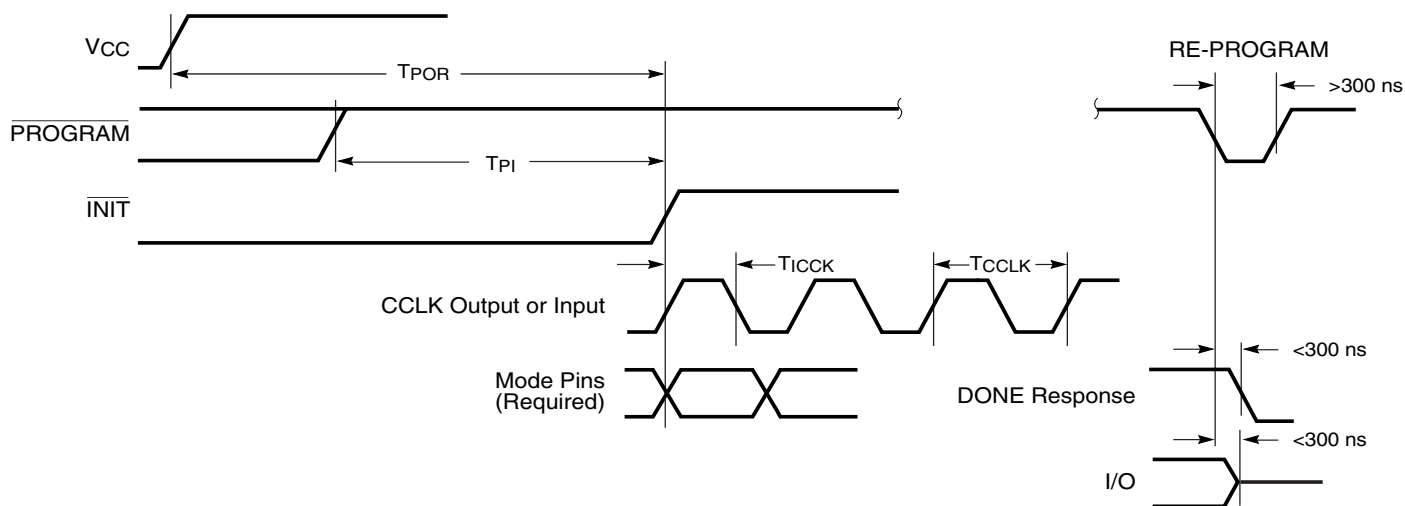
- Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits (+1 for Spartan-XL device)  
 Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1 (+ 1 for Spartan-XL device)  
 Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits  
 PROM Size = Program Data + 40 (header) + 8, rounded up to the nearest byte
- The user can add more "1" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.
- Express mode adds 57 (XCS05XL, XCS10XL), or 53 (XCS20XL, XCS30XL, XCS40XL) bits per frame, + additional start-up bits.
- XCS40XL provided 224 max I/O in CS280 package discontinued by [PDN2004-01](#).

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in [Figure 29](#). The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback

data is independent of the current device state. CLB outputs should not be included (Readback Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

## Configuration Switching Characteristics



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### Master Mode

Symbol	Description	Min	Max	Units
T <sub>POR</sub>	Power-on reset	40	130	ms
T <sub>PI</sub>	Program Latency	30	200	μs per CLB column
T <sub>ICCK</sub>	CCLK (output) delay	40	250	μs
T <sub>CCLK</sub>	CCLK (output) period, slow	640	2000	ns
T <sub>CCLK</sub>	CCLK (output) period, fast	100	250	ns

### Slave Mode

Symbol	Description	Min	Max	Units
T <sub>POR</sub>	Power-on reset	10	33	ms
T <sub>PI</sub>	Program latency	30	200	μs per CLB column
T <sub>ICCK</sub>	CCLK (input) delay (required)	4	-	μs
T <sub>CCLK</sub>	CCLK (input) period (required)	80	-	ns

## Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

## Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

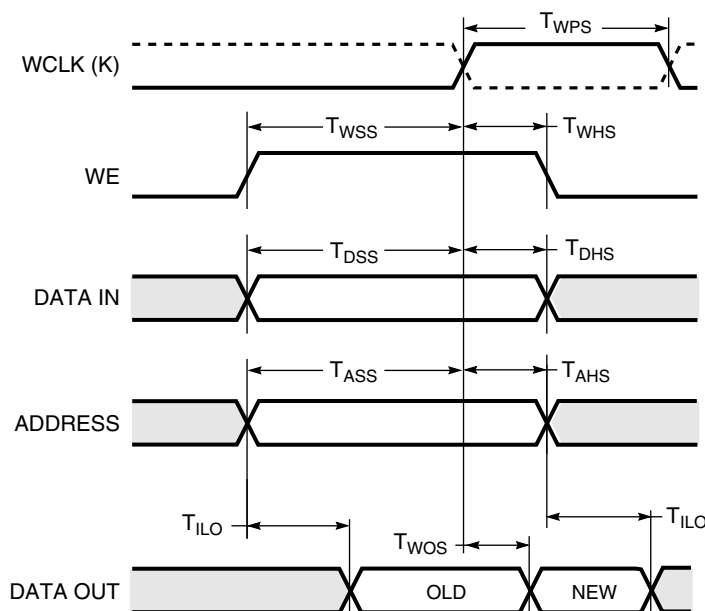
Symbol	Dual Port RAM	Size <sup>(1)</sup>	-4		-3		Units
			Min	Max	Min	Max	
Write Operation							
T <sub>WCDS</sub>	Address write cycle time (clock K period)	16x1	8.0	-	11.6	-	ns
T <sub>WPDS</sub>	Clock K pulse width (active edge)	16x1	4.0	-	5.8	-	ns
T <sub>ASDS</sub>	Address setup time before clock K	16x1	1.5	-	2.1	-	ns
T <sub>AHDS</sub>	Address hold time after clock K	16x1	0	-	0	-	ns
T <sub>DSDS</sub>	DIN setup time before clock K	16x1	1.5	-	1.6	-	ns
T <sub>DHDS</sub>	DIN hold time after clock K	16x1	0	-	0	-	ns
T <sub>WSDS</sub>	WE setup time before clock K	16x1	1.5	-	1.6	-	ns
T <sub>WHDS</sub>	WE hold time after clock K	16x1	0	-	0	-	ns
T <sub>WODS</sub>	Data valid after clock K	16x1	-	6.5	-	7.0	ns

### Notes:

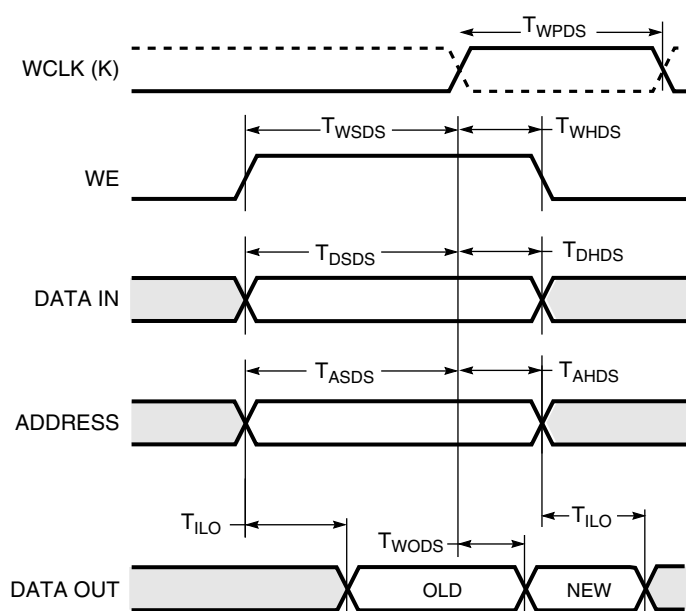
- Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

## Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Timing

### Single Port



### Dual Port



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### Spartan Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more pre-

cise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

#### Spartan Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
Global Primary Clock to TTL Output using OFF					
T <sub>ICKOF</sub>	Fast	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
T <sub>ICKO</sub>	Slew-rate limited	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
T <sub>ICKSOF</sub>	Fast	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
T <sub>ICKSO</sub>	Slew-rate limited	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
T <sub>CMOSOF</sub>	Fast	All devices	0.8	1.0	ns
T <sub>CMOSO</sub>	Slew-rate limited	All devices	1.5	2.0	ns

#### Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V<sub>CC</sub> threshold with 50 pF external capacitive load. For different loads, see [Figure 34](#).
3. OFF = Output Flip-Flop

## Spartan Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Setup Times - TTL Inputs <sup>(1)</sup>							
T <sub>ECIK</sub>	Clock Enable (EC) to Clock (IK), no delay	All devices	1.6	-	2.1	-	ns
T <sub>PICK</sub>	Pad to Clock (IK), no delay	All devices	1.5	-	2.0	-	ns
Hold Times							
T <sub>IKEC</sub>	Clock Enable (EC) to Clock (IK), no delay	All devices	0.0	-	0.9	-	ns
	All Other Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays - TTL Inputs <sup>(1)</sup>							
T <sub>PID</sub>	Pad to I1, I2	All devices	-	1.5	-	2.0	ns
T <sub>PLI</sub>	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.8	-	3.6	ns
T <sub>IKRI</sub>	Clock (IK) to I1, I2 (flip-flop)	All devices	-	2.7	-	2.8	ns
T <sub>IKLI</sub>	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	3.2	-	3.9	ns
Delay Adder for Input with Delay Option							
T <sub>Delay</sub>	T <sub>ECIKD</sub> = T <sub>ECIK</sub> + T <sub>Delay</sub> T <sub>PICKD</sub> = T <sub>PICK</sub> + T <sub>Delay</sub> T <sub>PDLI</sub> = T <sub>PLI</sub> + T <sub>Delay</sub>	XCS05	3.6	-	4.0	-	ns
		XCS10	3.7	-	4.1	-	ns
		XCS20	3.8	-	4.2	-	ns
		XCS30	4.5	-	5.0	-	ns
		XCS40	5.5	-	5.5	-	ns
Global Set/Reset							
T <sub>MRW</sub>	Minimum GSR pulse width	All devices	11.5	-	13.5	-	ns
T <sub>RRI</sub>	Delay from GSR input to any Q	XCS05	-	9.0	-	11.3	ns
		XCS10	-	9.5	-	11.9	ns
		XCS20	-	10.0	-	12.5	ns
		XCS30	-	10.5	-	13.1	ns
		XCS40	-	11.0	-	13.8	ns

### Notes:

1. Delay adder for CMOS Inputs option: for -3 speed grade, add 0.4 ns; for -4 speed grade, add 0.2 ns.
2. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
3. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## Spartan-XL Family Detailed Specifications

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

### Spartan-XL Family Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Description		Value	Units
$V_{CC}$	Supply voltage relative to GND		−0.5 to 4.0	V
$V_{IN}$	Input voltage relative to GND	5V Tolerant I/O Checked <sup>(2, 3)</sup>	−0.5 to 5.5	V
		Not 5V Tolerant I/Os <sup>(4, 5)</sup>	−0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	5V Tolerant I/O Checked <sup>(2, 3)</sup>	−0.5 to 5.5	V
		Not 5V Tolerant I/Os <sup>(4, 5)</sup>	−0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)		−65 to +150	°C
$T_J$	Junction temperature	Plastic packages	+125	°C

#### Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to −2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to −2.0V or overshoot to  $V_{CC} + 2.0V$ , provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

### Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CC}$	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ <sup>(1)</sup>	Industrial	3.0	3.6	V
$V_{IH}$	High-level input voltage <sup>(2)</sup>		50% of $V_{CC}$	5.5	V
$V_{IL}$	Low-level input voltage <sup>(2)</sup>		0	30% of $V_{CC}$	V
$T_{IN}$	Input signal transition time		-	250	ns

#### Notes:

- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement threshold is ~50% of  $V_{CC}$ .

### Spartan-XL Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clocks						
T <sub>CH</sub>	Clock High time	2.0	-	2.3	-	ns
T <sub>CL</sub>	Clock Low time	2.0	-	2.3	-	ns
Combinatorial Delays						
T <sub>ILO</sub>	F/G inputs to X/Y outputs	-	1.0	-	1.1	ns
T <sub>IHO</sub>	F/G inputs via H to X/Y outputs	-	1.7	-	2.0	ns
T <sub>ITO</sub>	F/G inputs via transparent latch to Q outputs	-	1.5	-	1.8	ns
T <sub>HH1O</sub>	C inputs via H1 via H to X/Y outputs	-	1.5	-	1.8	ns
Sequential Delays						
T <sub>CKO</sub>	Clock K to Flip-Flop or latch outputs Q	-	1.2	-	1.4	ns
Setup Time before Clock K						
T <sub>ICK</sub>	F/G inputs	0.6	-	0.7	-	ns
T <sub>IHCK</sub>	F/G inputs via H	1.3	-	1.6	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T <sub>RPW</sub>	Width (High)	2.5	-	2.8	-	ns
T <sub>RIO</sub>	Delay from C inputs via S/R, going High to Q	-	2.3	-	2.7	ns
Global Set/Reset						
T <sub>MRW</sub>	Minimum GSR Pulse Width	10.5	-	11.5	-	ns
T <sub>MRQ</sub>	Delay from GSR input to any Q	See <a href="#">page 60</a> for T <sub>RRI</sub> values per device.				
F <sub>TOG</sub>	Toggle Frequency (MHz) (for export control purposes)	-	250	-	217	MHz



### Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation <sup>(1)</sup>							
T <sub>WCDS</sub>	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T <sub>WPDS</sub>	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T <sub>ASDS</sub>	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T <sub>DSDS</sub>	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T <sub>WSDS</sub>	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T <sub>WODS</sub>	Data valid after clock K	16x1	-	5.2	-	6.1	ns

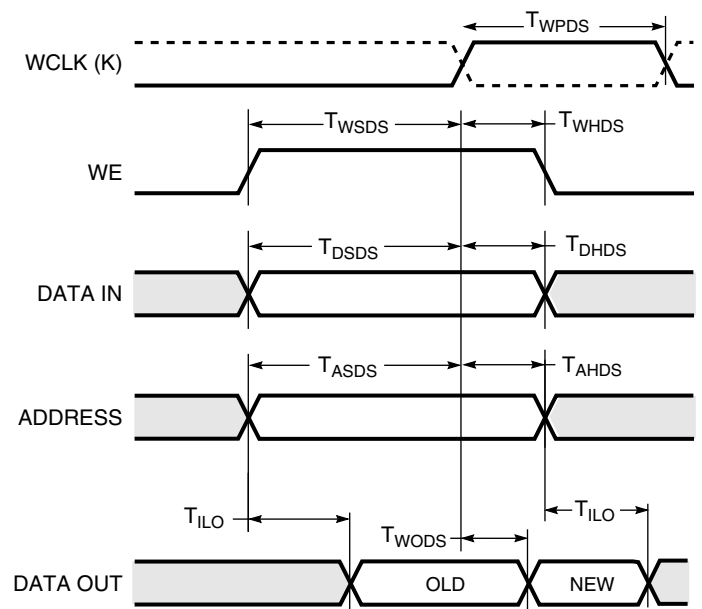
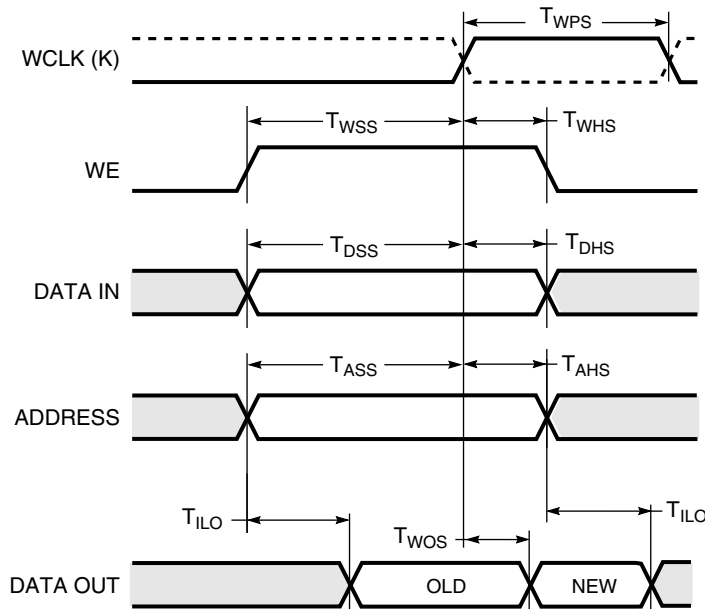
#### Notes:

1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

### Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

#### Single Port

#### Dual Port



DS060\_34\_011300

### Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and Spartan-XL device. They follow the pad locations around the die, and include boundary scan register locations.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

#### XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	Bndry Scan
VCC	P2	P89	-
I/O	P3	P90	32
I/O	P4	P91	35
I/O	-	P92	38
I/O	-	P93	41
I/O	P5	P94	44
I/O	P6	P95	47
I/O	P7	P96	50
I/O	P8	P97	53
I/O	P9	P98	56
I/O, SGCK1 <sup>(1)</sup> , GCK8 <sup>(2)</sup>	P10	P99	59
VCC	P11	P100	-
GND	P12	P1	-
I/O, PGCK1 <sup>(1)</sup> , GCK1 <sup>(2)</sup>	P13	P2	62
I/O	P14	P3	65
I/O, TDI	P15	P4	68
I/O, TCK	P16	P5	71
I/O, TMS	P17	P6	74
I/O	P18	P7	77
I/O	-	P8	83
I/O	P19	P9	86
I/O	P20	P10	89
GND	P21	P11	-
VCC	P22	P12	-
I/O	P23	P13	92
I/O	P24	P14	95
I/O	-	P15	98
I/O	P25	P16	104
I/O	P26	P17	107
I/O	P27	P18	110
I/O	-	P19	113
I/O	P28	P20	116
I/O, SGCK2 <sup>(1)</sup> , GCK2 <sup>(2)</sup>	P29	P21	119
Not Connected <sup>(1)</sup> , M1 <sup>(2)</sup>	P30	P22	122
GND	P31	P23	-
MODE <sup>(1)</sup> , M0 <sup>(2)</sup>	P32	P24	125
VCC	P33	P25	-

#### XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	Bndry Scan
Not Connected <sup>(1)</sup> , PWRDWN <sup>(2)</sup>	P34	P26	126 <sup>(1)</sup>
I/O, PGCK2 <sup>(1)</sup> , GCK3 <sup>(2)</sup>	P35	P27	127 <sup>(3)</sup>
I/O (HDC)	P36	P28	130 <sup>(3)</sup>
I/O	-	P29	133 <sup>(3)</sup>
I/O (LDC)	P37	P30	136 <sup>(3)</sup>
I/O	P38	P31	139 <sup>(3)</sup>
I/O	P39	P32	142 <sup>(3)</sup>
I/O	-	P33	145 <sup>(3)</sup>
I/O	-	P34	148 <sup>(3)</sup>
I/O	P40	P35	151 <sup>(3)</sup>
I/O (INIT)	P41	P36	154 <sup>(3)</sup>
VCC	P42	P37	-
GND	P43	P38	-
I/O	P44	P39	157 <sup>(3)</sup>
I/O	P45	P40	160 <sup>(3)</sup>
I/O	-	P41	163 <sup>(3)</sup>
I/O	-	P42	166 <sup>(3)</sup>
I/O	P46	P43	169 <sup>(3)</sup>
I/O	P47	P44	172 <sup>(3)</sup>
I/O	P48	P45	175 <sup>(3)</sup>
I/O	P49	P46	178 <sup>(3)</sup>
I/O	P50	P47	181 <sup>(3)</sup>
I/O, SGCK3 <sup>(1)</sup> , GCK4 <sup>(2)</sup>	P51	P48	184 <sup>(3)</sup>
GND	P52	P49	-
DONE	P53	P50	-
VCC	P54	P51	-
PROGRAM	P55	P52	-
I/O (D7 <sup>(2)</sup> )	P56	P53	187 <sup>(3)</sup>
I/O, PGCK3 <sup>(1)</sup> , GCK5 <sup>(2)</sup>	P57	P54	190 <sup>(3)</sup>
I/O (D6 <sup>(2)</sup> )	P58	P55	193 <sup>(3)</sup>
I/O	-	P56	196 <sup>(3)</sup>
I/O (D5 <sup>(2)</sup> )	P59	P57	199 <sup>(3)</sup>
I/O	P60	P58	202 <sup>(3)</sup>
I/O	-	P59	205 <sup>(3)</sup>
I/O	-	P60	208 <sup>(3)</sup>
I/O (D4 <sup>(2)</sup> )	P61	P61	211 <sup>(3)</sup>
I/O	P62	P62	214 <sup>(3)</sup>
VCC	P63	P63	-
GND	P64	P64	-
I/O (D3 <sup>(2)</sup> )	P65	P65	217 <sup>(3)</sup>
I/O	P66	P66	220 <sup>(3)</sup>
I/O	-	P67	223 <sup>(3)</sup>
I/O (D2 <sup>(2)</sup> )	P67	P68	229 <sup>(3)</sup>
I/O	P68	P69	232 <sup>(3)</sup>
I/O (D1 <sup>(2)</sup> )	P69	P70	235 <sup>(3)</sup>

### CS280

VCC Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-
Not Connected Pins					
A4	A12	C8	C12	C15	D1
D2	D5	D8	D17	D18	E15
H2	H3	H18	H19	L4	M1
M16	M18	R2	R4	R5	R15
R17	T8	T15	U5	V8	V12
W12	W16	-	-	-	-
Not Connected Pins (VCC in XCS40XL)					
B5	B15	E3	E18	R3	R18
V5	V15	-	-	-	-

5/21/02

### XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 <sup>(2,5)</sup>	Bndry Scan
VCC	P183	P212	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	P184	P213	C10	D10	86
I/O	P185	P214	D10	E10	89
I/O	P186	P215	A9	A9	92
I/O	P187	P216	B9	B9	95
I/O	P188	P217	C9	C9	98
I/O	P189	P218	D9	D9	101
I/O	P190	P220	A8	A8	104
I/O	P191	P221	B8	B8	107
I/O	-	-	C8	C8	110
I/O	-	-	A7	D8	113
VCC	P192	P222	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	-	P223	A6	B7	116
I/O	-	P224	C7	C7	119
I/O	P193	P225	B6	D7	122
I/O	P194	P226	A5	A6	125
GND	P195	P227	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P196	P228	C6	B6	128
I/O	P197	P229	B5	C6	131
I/O	P198	P230	A4	D6	134
I/O	P199	P231	C5	E6	137

### XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 <sup>(2,5)</sup>	Bndry Scan
I/O	P200	P232	B4	A5	140
I/O	P201	P233	A3	C5	143
I/O	-	-	-	D5	146
I/O	-	-	-	A4	149
I/O	P202	P234	D5	B4	152
I/O	P203	P235	C4	C4	155
I/O	P204	P236	B3	A3	158
I/O	P205	P237	B2	A2	161
I/O	P206	P238	A2	B3	164
I/O, SGCK1 <sup>(1)</sup> , GCK8 <sup>(2)</sup>	P207	P239	C3	B2	167
VCC	P208	P240	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
GND	P1	P1	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O, PGCK1 <sup>(1)</sup> , GCK1 <sup>(2)</sup>	P2	P2	B1	C3	170
I/O	P3	P3	C2	C2	173
I/O	P4	P4	D2	B1	176
I/O	P5	P5	D3	C1	179
I/O, TDI	P6	P6	E4	D4	182
I/O, TCK	P7	P7	C1	D3	185
I/O	-	-	-	D2	188
I/O	-	-	-	D1	191
I/O	P8	P8	D1	E2	194
I/O	P9	P9	E3	E4	197
I/O	P10	P10	E2	E1	200
I/O	P11	P11	E1	F5	203
I/O	P12	P12	F3	F3	206
I/O	-	P13	F2	F2	209
GND	P13	P14	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P14	P15	G3	F4	212
I/O	P15	P16	G2	F1	215
I/O, TMS	P16	P17	G1	G3	218
I/O	P17	P18	H3	G2	221
VCC	P18	P19	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	-	P20	H2	G4	224
I/O	-	P21	H1	H1	227
I/O	-	-	J4	H3	230
I/O	-	-	J3	H2	233
I/O	P19	P23	J2	H4	236
I/O	P20	P24	J1	J1	239
I/O	P21	P25	K2	J2	242
I/O	P22	P26	K3	J3	245
I/O	P23	P27	K1	J4	248
I/O	P24	P28	L1	K1	251

## XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 <sup>(2,5)</sup>	Bndry Scan
O, TDO	P157	P181	A19	B17	0
GND	P158	P182	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P159	P183	B18	A18	2
I/O, PGCK4 <sup>(1)</sup> , GCK7 <sup>(2)</sup>	P160	P184	B17	A17	5
I/O	P161	P185	C17	D16	8
I/O	P162	P186	D16	C16	11
I/O (CS1 <sup>(2)</sup> )	P163	P187	A18	B16	14
I/O	P164	P188	A17	A16	17
I/O	-	-	-	E15	20
I/O	-	-	-	C15	23
I/O	P165	P189	C16	D15	26
I/O	-	P190	B16	A15	29
I/O	P166	P191	A16	E14	32
I/O	P167	P192	C15	C14	35
I/O	P168	P193	B15	B14	38
I/O	P169	P194	A15	D14	41
GND	P170	P196	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P171	P197	B14	A14	44
I/O	P172	P198	A14	C13	47
I/O	-	P199	C13	B13	50
I/O	-	P200	B13	A13	53
VCC	P173	P201	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	-	-	A13	A12	56
I/O	-	-	D12	C12	59
I/O	P174	P202	C12	B12	62
I/O	P175	P203	B12	D12	65
I/O	P176	P205	A12	A11	68
I/O	P177	P206	B11	B11	71
I/O	P178	P207	C11	C11	74
I/O	P179	P208	A11	D11	77
I/O	P180	P209	A10	A10	80
I/O	P181	P210	B10	B10	83
GND	P182	P211	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-

2/8/00

## Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS40XL is not part of the Boundary Scan chain. For the XCS40XL, subtract 1 from all Boundary Scan numbers from GCK3 on (343 and higher).
4. Pads labeled GND<sup>(4)</sup> or VCC<sup>(4)</sup> are internally bonded to Ground or VCC planes within the package.
5. CS280 package discontinued by [PDN2004-01](#)

## Additional XCS40/XL Package Pins

## PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

2/12/98

## BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

6/17/97

## CS280

VCC Pins					
A1	A7	B5	B15	C10	C17
D13	E3	E18	G1	G19	K2
K17	M4	N16	R3	R18	T7
U3	U10	U17	V5	V15	W13
GND Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-

5/19/99

### Revision History

The following table shows the revision history for this document.

Date	Version	Description
11/20/98	1.3	Added Spartan-XL specs and Power Down.
01/06/99	1.4	All Spartan-XL -4 specs designated Preliminary with no changes.
03/02/00	1.5	Added CS package, updated Spartan-XL specs to Final.
09/19/01	1.6	Reformatted, updated power specs, clarified configuration information. Removed $T_{SOL}$ soldering information from Absolute Maximum Ratings table. Changed <b>Figure 26</b> : Slave Serial Mode Characteristics: $T_{CCH}$ , $T_{CCL}$ from 45 to 40 ns. Changed Master Mode Configuration Switching Characteristics: $T_{CCLK}$ min. from 80 to 100 ns. Added Total Dist. RAM Bits to <b>Table 1</b> ; added <b>Start-Up, page 36</b> characteristics.
06/27/02	1.7	Clarified Express Mode pseudo daisy chain. Added new Industrial options. Clarified XCS30XL CS280 $V_{CC}$ pinout.
06/26/08	1.8	Noted that PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, are discontinued by <a href="#">PDN2004-01</a> . Extended description of recommended maximum delay of reconfiguration in <b>Delaying Configuration After Power-Up, page 35</b> . Added reference to Pb-free package options and provided link to <b>Package Specifications, page 81</b> . Updated links.
03/01/13	2.0	The products listed in this data sheet are obsolete. See <a href="#">XCN10016</a> and <a href="#">XCN11010</a> for further information.