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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	466
Total RAM Bits	6272
Number of I/O	112
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs10xl-4tq144c

Spartan and Spartan-XL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In addition to the conventional benefit of high volume programmable logic solutions, Spartan series FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan/XL families leverage the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA process developments.

Logic Functional Description

The Spartan series uses a standard FPGA structure as shown in [Figure 1, page 2](#). The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in [Figure 2](#). There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the [Advanced Features Description, page 13](#).

Function Generators

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box "A" of [Figure 2](#)). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.

Table 4: Supported Sources for Spartan/XL Inputs

Source	Spartan Inputs		Spartan-XL Inputs
	5V, TTL	5V, CMOS	3.3V CMOS
Any device, $V_{CC} = 3.3V$, CMOS outputs	✓	Unreliable Data	✓
Spartan family, $V_{CC} = 5V$, TTL outputs	✓		✓
Any device, $V_{CC} = 5V$, TTL outputs ($V_{OH} \leq 3.7V$)	✓		✓
Any device, $V_{CC} = 5V$, CMOS outputs	✓	✓	✓ (default mode)

Table 5: I/O Standards Supported by Spartan-XL FPGAs

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}
LVC MOS 3V	OK	12/24 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}

Additional Fast Capture Input Latch (Spartan-XL Family Only)

The Spartan-XL family OB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active High input flip-flop. ILFLX is a transparent Low Fast Capture latch followed by a transparent High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 6.


Spartan-XL Family V_{CC} Clamping

Spartan-XL FPGAs have an optional clamping diode connected from each I/O to V_{CC} . When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. V_{CC} clamping is a global option affecting all I/O pins.


Spartan-XL devices are fully 5V TTL I/O compatible if V_{CC} clamping is not enabled. With V_{CC} clamping enabled, the Spartan-XL devices will begin to clamp input voltages to one diode voltage drop above V_{CC} . If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

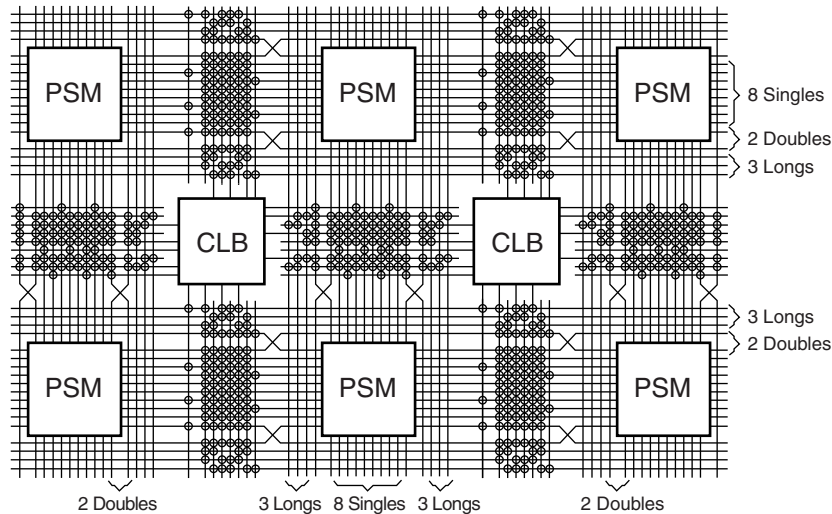
Spartan-XL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 5.

Table 6: Output Flip-Flop Functionality

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
		1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

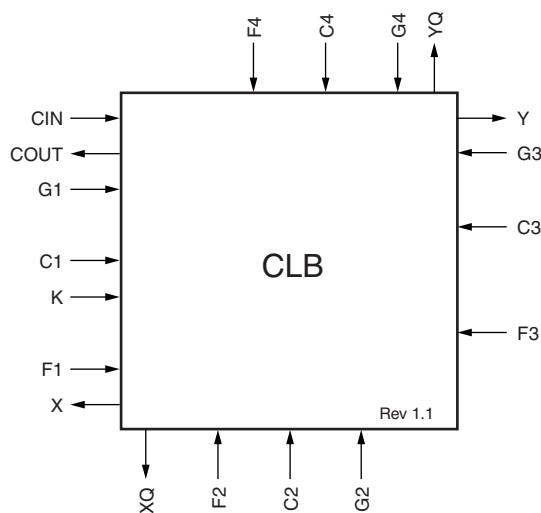


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Figure 8: Spartan/XL CLB Routing Channels and Interface Block Diagram

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.



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Figure 9: CLB Interconnect Signals

Programmable Switch Matrices

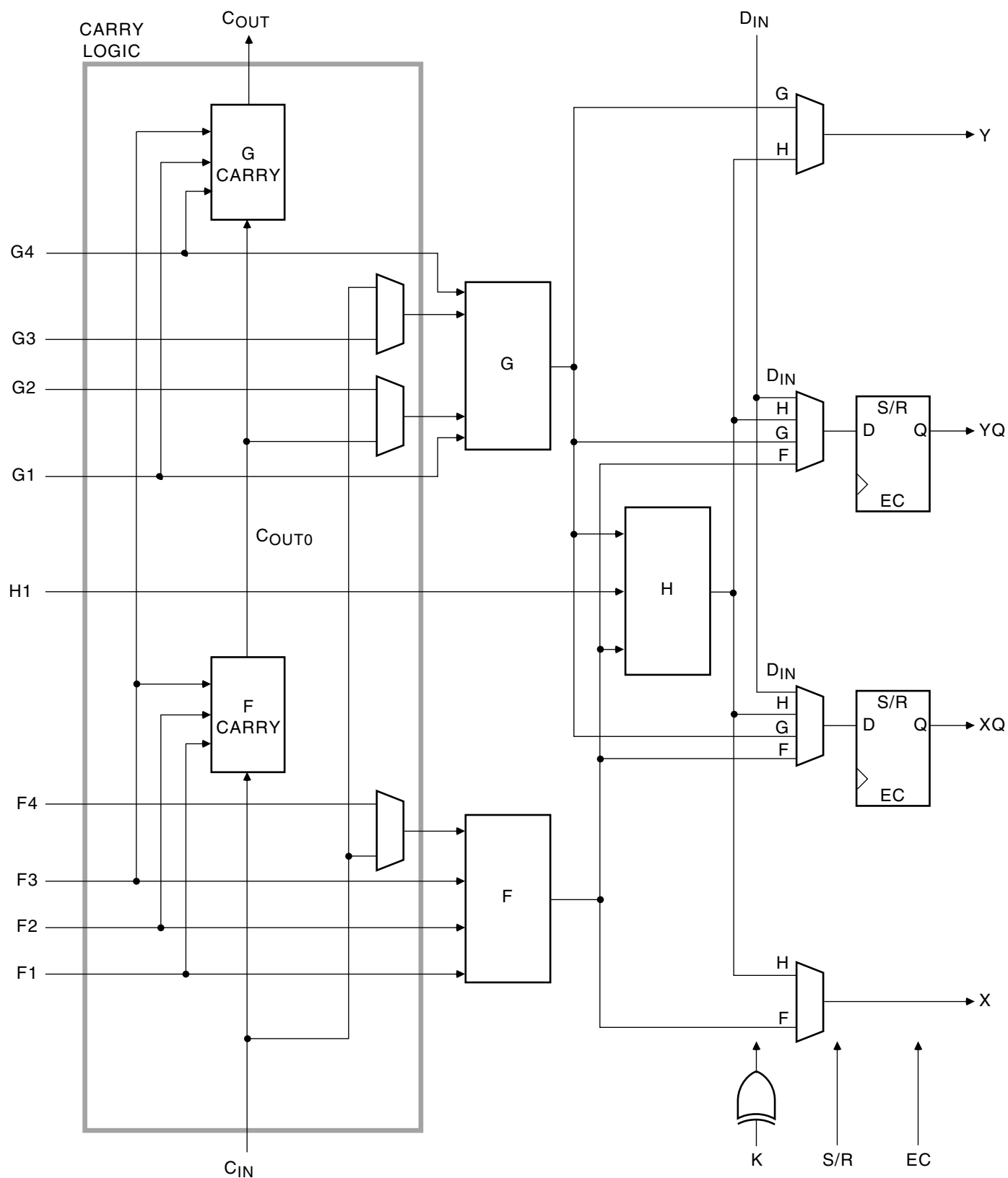
The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

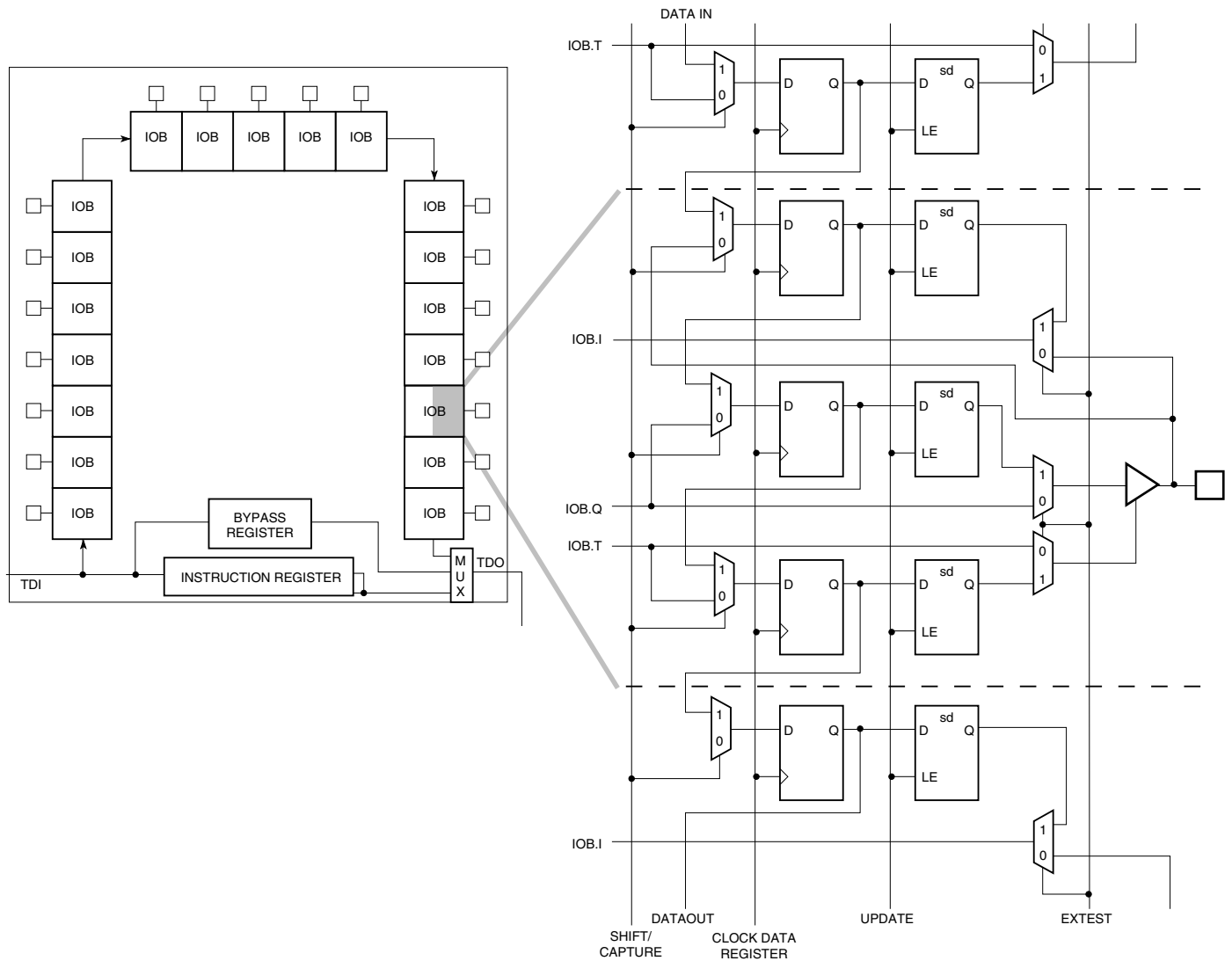
Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs. Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.



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Figure 16: Fast Carry Logic in Spartan/XL CLB



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Figure 20: Spartan/XL Boundary Scan Logic

Table 12: Boundary Scan Instructions

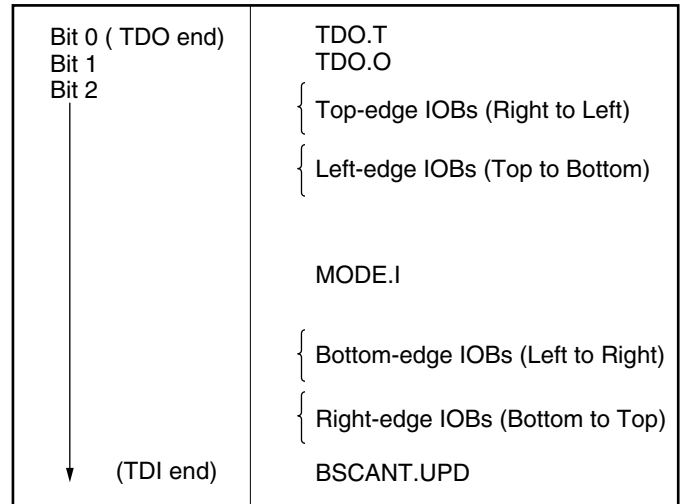
Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	IDCODE (Spartan-XL only)	IDCODE Register	-
1	1	1	BYPASS	Bypass Register	-

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-state. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contribute all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 21. The device-specific pinout tables for the Spartan/XL devices include the boundary scan locations for each IOB pin.



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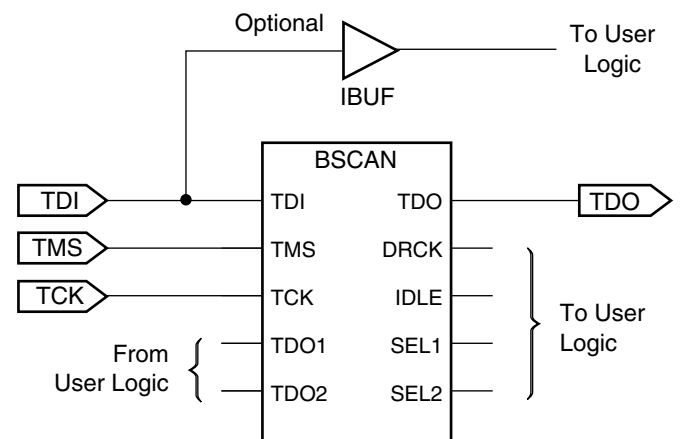
Figure 21: Boundary Scan Bit Sequence

BSDL (Boundary Scan Description Language) files for Spartan/XL devices are available on the Xilinx website in the File Download area. Note that the 5V Spartan devices and 3V Spartan-XL devices have different BSDL files.

Including Boundary Scan in a Design

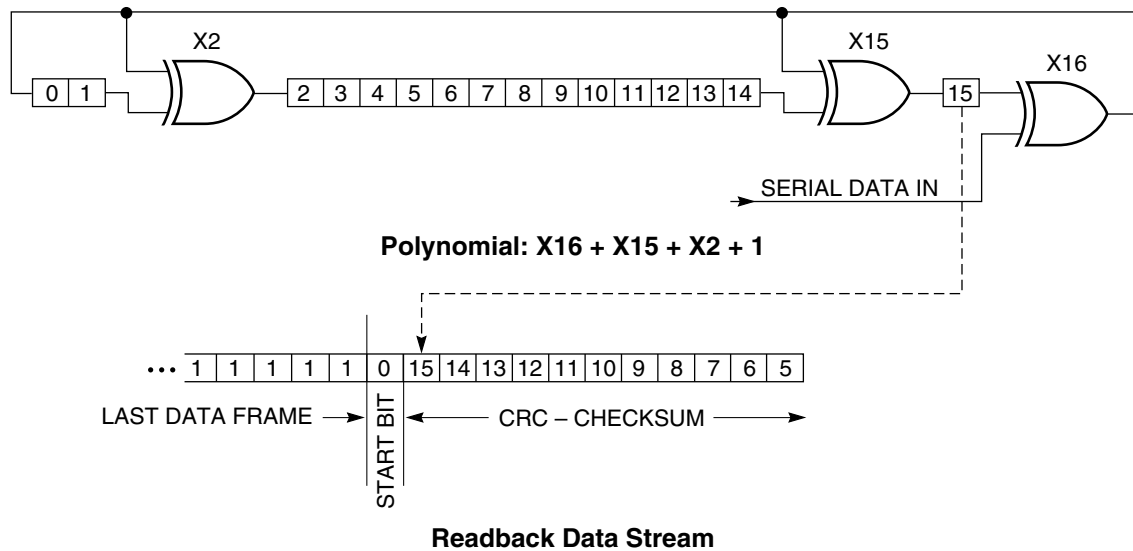
If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 22.



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Figure 22: Boundary Scan Example



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Figure 29: Circuit for Generating CRC-16

Configuration Sequence

There are four major steps in the Spartan/XL FPGA power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC} . When all \overline{INIT} pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin

Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the \overline{INIT} input.

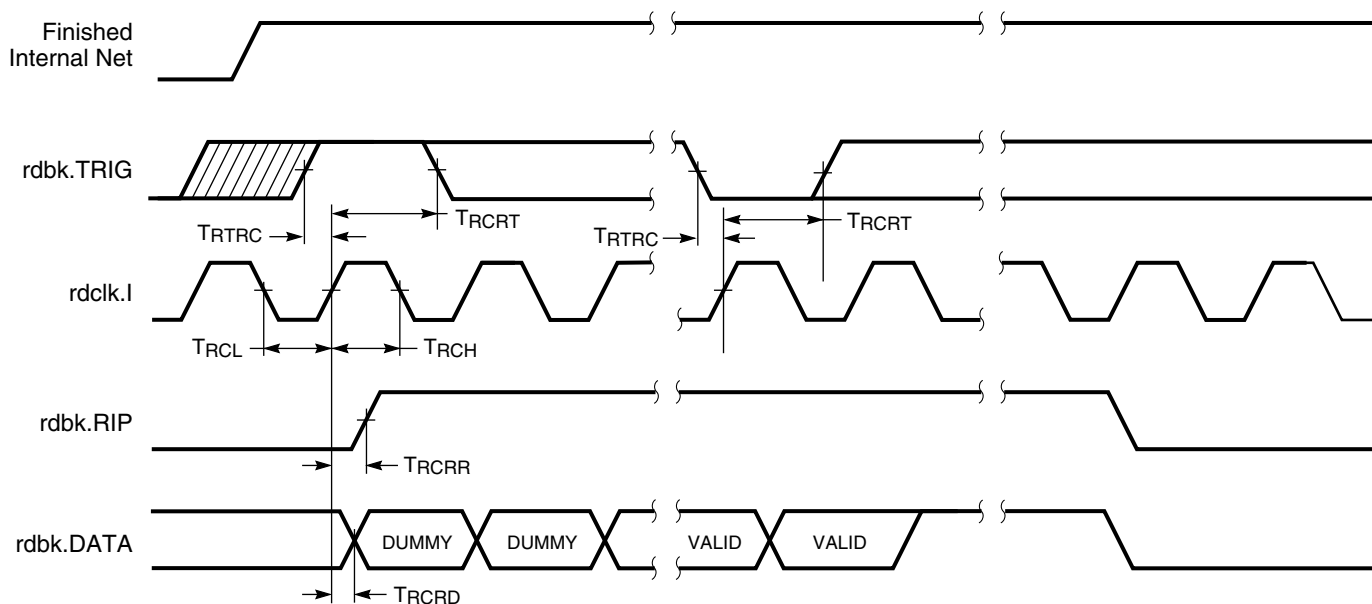
Initialization

During initialization and configuration, user pins \overline{HDC} , \overline{LDC} , \overline{INIT} and \overline{DONE} provide status outputs for the system interface. The outputs \overline{LDC} , \overline{INIT} and \overline{DONE} are held Low and \overline{HDC} is held High starting at the initial application of power.

The open drain \overline{INIT} pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive \overline{INIT} . Two internal clocks after the \overline{INIT} pin is recognized as High, the device samples the \overline{MODE} pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.



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Figure 33: Spartan and Spartan-XL Readback Timing Diagram

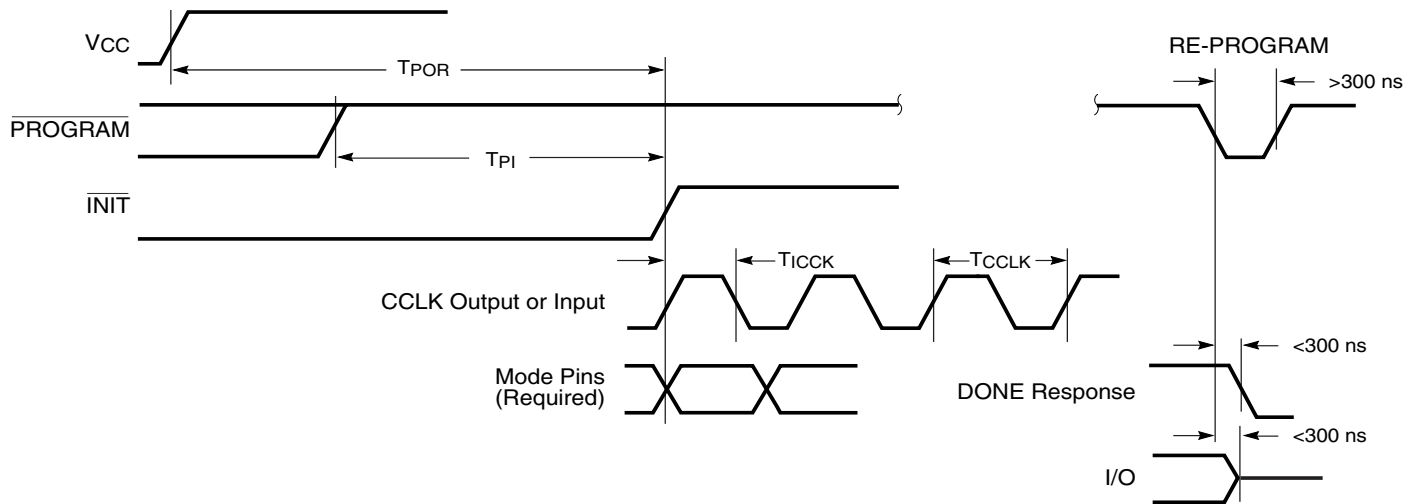
Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:

1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Configuration Switching Characteristics



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Master Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	40	130	ms
T_{PI}	Program Latency	30	200	μs per CLB column
T_{ICCK}	CCLK (output) delay	40	250	μs
T_{CCLK}	CCLK (output) period, slow	640	2000	ns
T_{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	10	33	ms
T_{PI}	Program latency	30	200	μs per CLB column
T_{ICCK}	CCLK (input) delay (required)	4	-	μs
T_{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings⁽¹⁾

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		−0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked ^(2, 3)	−0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	−0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked ^(2, 3)	−0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	−0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)		−65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to −2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to −2.0V or overshoot to $V_{CC} + 2.0V$, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ ⁽¹⁾	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage ⁽²⁾		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage ⁽²⁾		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:

- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement threshold is ~50% of V_{CC} .

Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Typ.	Max	Units
V _{OH}	High-level output voltage @ I _{OH} = −4.0 mA, V _{CC} min (LVTTL)		2.4	-	-	V
	High-level output voltage @ I _{OH} = −500 μA, (LVCMOS)		90% V _{CC}	-	-	V
V _{OL}	Low-level output voltage @ I _{OL} = 12.0 mA, V _{CC} min (LVTTL) ⁽¹⁾		-	-	0.4	V
	Low-level output voltage @ I _{OL} = 24.0 mA, V _{CC} min (LVTTL) ⁽²⁾		-	-	0.4	V
	Low-level output voltage @ I _{OL} = 1500 μA, (LVCMOS)		-	-	10% V _{CC}	V
V _{DR}	Data retention supply voltage (below which configuration data may be lost)		2.5	-	-	V
I _{CCO}	Quiescent FPGA supply current ^(3,4)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I _{CCPD}	Power Down FPGA supply current ^(3,5)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I _L	Input or output leakage current		−10	-	10	μA
C _{IN}	Input capacitance (sample tested)		-	-	10	pF
I _{RPU}	Pad pull-up (when selected) @ V _{IN} = 0V (sample tested)		0.02	-	0.25	mA
I _{RPD}	Pad pull-down (when selected) @ V _{IN} = 3.3V (sample tested)		0.02	-	-	mA

Notes:

1. With up to 64 pins simultaneously sinking 12 mA (default mode).
2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
4. With no output current loads, no active input resistors, and all package pins at V_{CC} or GND.
5. With \overline{PWRDWN} active.

Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CC} lines for a successful power on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Max	Units
I_{CCPO}	Total V_{CC} supply current required during power-on	100	-	mA
T_{CCPO}	V_{CC} ramp time ^(2,3)	-	50	ms

Notes:

1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CC} ramps from 0 to 3.3V.
2. The ramp time is measured from GND to V_{CC} max on a fully loaded board.
3. V_{CC} must not dip in the negative direction during power on.

Spartan-XL Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case oper-

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Global Clock to Output using OFF					
T _{ICKOF}	Fast	XCS05XL	4.6	5.2	ns
		XCS10XL	4.9	5.5	ns
		XCS20XL	5.2	5.8	ns
		XCS30XL	5.5	6.2	ns
		XCS40XL	5.8	6.5	ns
Slew Rate Adjustment					
T _{SLOW}	For Output SLOW option add	All Devices	1.5	1.7	ns

Notes:

1. Output delays are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.
3. OFF = Output Flip Flop

Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

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Spartan-XL Family Setup and Hold

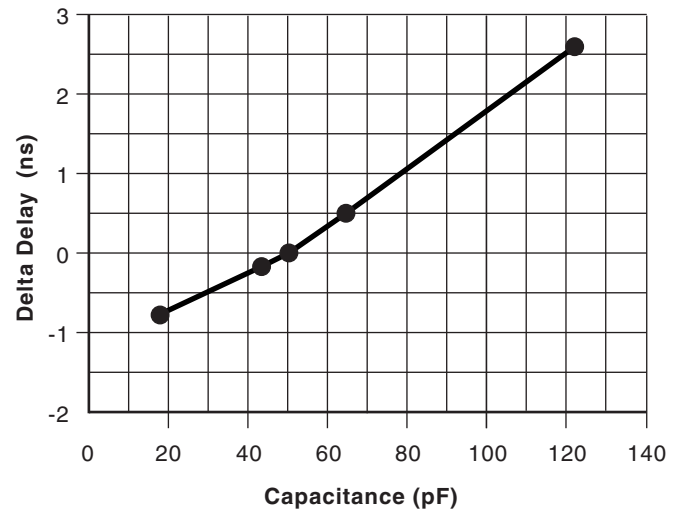
Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Input Setup/Hold Times Using Global Clock and IFF					
T _{SUF} /T _{HF}	No Delay	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
T _{SU} /T _H	Full Delay	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



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Figure 35: Delay Factor at Various Capacitive Loads

Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See **Global Signals: GSR and GTS**, page 20 for more information.

Device pins for Spartan/XL devices are described in **Table 18**.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pin-outs as the standard package options.

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
V _{CC}	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 – 0.1 μ F capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See Violating the Maximum High and Low Time Specification for the Readback Clock , page 39 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an open-drain output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7 ⁽²⁾)	P53	L12	P75	P107	367 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P54	L13	P76	P108	370 ⁽³⁾
I/O	-	K10	P77	P109	373 ⁽³⁾
I/O	-	K11	P78	P110	376 ⁽³⁾
I/O (D6 ⁽²⁾)	P55	K12	P79	P112	379 ⁽³⁾
I/O	P56	K13	P80	P113	382 ⁽³⁾
I/O	-	-	-	P114	385 ⁽³⁾
I/O	-	-	-	P115	388 ⁽³⁾
I/O	-	-	-	P116	391 ⁽³⁾
I/O	-	-	-	P117	394 ⁽³⁾
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 ⁽³⁾
I/O	-	J12	P83	P120	400 ⁽³⁾
VCC ⁽²⁾	-	-	-	P121	-
I/O (D5 ⁽²⁾)	P57	J13	P84	P122	403 ⁽³⁾
I/O	P58	H10	P85	P123	406 ⁽³⁾
I/O	-	-	-	P124	409 ⁽³⁾
I/O	-	-	-	P125	412 ⁽³⁾
I/O	P59	H11	P86	P126	415 ⁽³⁾
I/O	P60	H12	P87	P127	418 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	H13	P88	P128	421 ⁽³⁾
I/O	P62	G12	P89	P129	424 ⁽³⁾
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3 ⁽²⁾)	P65	G10	P92	P132	427 ⁽³⁾
I/O	P66	F13	P93	P133	430 ⁽³⁾
I/O	P67	F12	P94	P134	433 ⁽³⁾
I/O	-	F11	P95	P135	436 ⁽³⁾
I/O	-	-	-	P136	439 ⁽³⁾
I/O	-	-	-	P137	442 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	F10	P96	P138	445 ⁽³⁾
I/O	P69	E13	P97	P139	448 ⁽³⁾
VCC ⁽²⁾	-	-	-	P140	-
I/O	-	E12	P98	P141	451 ⁽³⁾
I/O	-	E11	P99	P142	454 ⁽³⁾
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 ⁽³⁾
I/O	-	-	-	P146	460 ⁽³⁾
I/O	-	-	-	P147	463 ⁽³⁾
I/O	-	-	-	P148	466 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	D13	P101	P149	469 ⁽³⁾
I/O	P71	D12	P102	P150	472 ⁽³⁾
I/O	-	D11	P103	P151	475 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	C12	P105	P153	481 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	C11	P106	P154	484 ⁽³⁾
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1 ⁽²⁾)	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC ⁽²⁾	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

2/8/00

Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 ⁽¹⁾	P33 ⁽¹⁾	P39	P65	P71 ⁽¹⁾
P86 ⁽¹⁾	P92	P111	P121 ⁽¹⁾	P140 ⁽¹⁾	P144
P165	P173 ⁽¹⁾	P192 ⁽¹⁾	P202	P203	-
9/16/98					

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by [PDN2004-01](#)

XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
VCC	P89	P128	P183	P212	VCC ⁽⁴⁾	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC ⁽⁴⁾	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC ⁽⁴⁾	A1	-
GND	P1	P1	P1	P1	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	P5	P5	P5	D3	C1	155
I/O, TDI	P4	P6	P6	P6	E4	D4	158
I/O, TCK	P5	P7	P7	P7	C1	D3	161
I/O	-	-	P8	P8	D1	E2	164
I/O	-	-	P9	P9	E3	E4	167
I/O	-	-	P10	P10	E2	E1	170
I/O	-	-	P11	P11	E1	F5	173
I/O	-	-	P12	P12	F3	F3	176
I/O	-	-	-	P13	F2	F2	179
GND	-	P8	P13	P14	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P9	P14	P15	G3	F4	182
I/O	-	P10	P15	P16	G2	F1	185
I/O, TMS	P6	P11	P16	P17	G1	G3	188
I/O	P7	P12	P17	P18	H3	G2	191
VCC	-	-	P18	P19	VCC ⁽⁴⁾	G1	-
I/O	-	-	-	P20	H2	G4	194
I/O	-	-	-	P21	H1	H1	197
I/O	-	-	P19	P23	J2	H4	200
I/O	-	-	P20	P24	J1	J1	203
I/O	-	P13	P21	P25	K2	J2	206
I/O	P8	P14	P22	P26	K3	J3	209
I/O	P9	P15	P23	P27	K1	J4	212
I/O	P10	P16	P24	P28	L1	K1	215
GND	P11	P17	P25	P29	GND ⁽⁴⁾	GND ⁽⁴⁾	-
VCC	P12	P18	P26	P30	VCC ⁽⁴⁾	K2	-
I/O	P13	P19	P27	P31	L2	K3	218
I/O	P14	P20	P28	P32	L3	K4	221
I/O	P15	P21	P29	P33	L4	K5	224
I/O	-	P22	P30	P34	M1	L1	227
I/O	-	-	P31	P35	M2	L2	230
I/O	-	-	P32	P36	M3	L3	233
I/O	-	-	-	P38	N1	M2	236
I/O	-	-	-	P39	N2	M3	239
VCC	-	-	P33	P40	VCC ⁽⁴⁾	M4	-
I/O	P16	P23	P34	P41	P1	N1	242
I/O	P17	P24	P35	P42	P2	N2	245
I/O	-	P25	P36	P43	R1	N3	248
I/O	-	P26	P37	P44	P3	N4	251
GND	-	P27	P38	P45	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P46	T1	P1	254
I/O	-	-	P39	P47	R3	P2	257
I/O	-	-	P40	P48	T2	P3	260
I/O	-	-	P41	P49	U1	P4	263
I/O	-	-	P42	P50	T3	P5	266
I/O	-	-	P43	P51	U2	R1	269

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	P85	P97	U12	T11	382 ⁽³⁾
I/O	-	-	-	P99	V13	U12	385 ⁽³⁾
I/O	-	-	-	P100	Y14	T12	388 ⁽³⁾
VCC	-	-	P86	P101	VCC ⁽⁴⁾	W13	-
I/O	P43	P60	P87	P102	Y15	V13	391 ⁽³⁾
I/O	P44	P61	P88	P103	V14	U13	394 ⁽³⁾
I/O	-	P62	P89	P104	W15	T13	397 ⁽³⁾
I/O	-	P63	P90	P105	Y16	W14	400 ⁽³⁾
GND	-	P64	P91	P106	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P107	V15	V14	403 ⁽³⁾
I/O	-	-	P92	P108	W16	U14	406 ⁽³⁾
I/O	-	-	P93	P109	Y17	T14	409 ⁽³⁾
I/O	-	-	P94	P110	V16	R14	412 ⁽³⁾
I/O	-	-	P95	P111	W17	W15	415 ⁽³⁾
I/O	-	-	P96	P112	Y18	U15	418 ⁽³⁾
I/O	P45	P65	P97	P113	U16	V16	421 ⁽³⁾
I/O	P46	P66	P98	P114	V17	U16	424 ⁽³⁾
I/O	-	P67	P99	P115	W18	W17	427 ⁽³⁾
I/O	-	P68	P100	P116	Y19	W18	430 ⁽³⁾
I/O	P47	P69	P101	P117	V18	V17	433 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P48	P70	P102	P118	W19	V18	436 ⁽³⁾
GND	P49	P71	P103	P119	GND ⁽⁴⁾	GND ⁽⁴⁾	-
DONE	P50	P72	P104	P120	Y20	W19	-
VCC	P51	P73	P105	P121	VCC ⁽⁴⁾	U17	-
PROGRAM	P52	P74	P106	P122	V19	U18	-
I/O (D7 ⁽²⁾)	P53	P75	P107	P123	U19	V19	439 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P54	P76	P108	P124	U18	U19	442 ⁽³⁾
I/O	-	P77	P109	P125	T17	T16	445 ⁽³⁾
I/O	-	P78	P110	P126	V20	T17	448 ⁽³⁾
I/O	-	-	-	P127	U20	T18	451 ⁽³⁾
I/O	-	-	P111	P128	T18	T19	454 ⁽³⁾
I/O (D6 ⁽²⁾)	P55	P79	P112	P129	T19	R16	457 ⁽³⁾
I/O	P56	P80	P113	P130	T20	R19	460 ⁽³⁾
I/O	-	-	P114	P131	R18	P15	463 ⁽³⁾
I/O	-	-	P115	P132	R19	P17	466 ⁽³⁾
I/O	-	-	P116	P133	R20	P18	469 ⁽³⁾
I/O	-	-	P117	P134	P18	P16	472 ⁽³⁾
GND	-	P81	P118	P135	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P136	P20	P19	475 ⁽³⁾
I/O	-	-	-	P137	N18	N17	478 ⁽³⁾
I/O	-	P82	P119	P138	N19	N18	481 ⁽³⁾
I/O	-	P83	P120	P139	N20	N19	484 ⁽³⁾
VCC	-	-	P121	P140	VCC ⁽⁴⁾	N16	-
I/O (D5 ⁽²⁾)	P57	P84	P122	P141	M17	M19	487 ⁽³⁾
I/O	P58	P85	P123	P142	M18	M17	490 ⁽³⁾

Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: Component Availability Chart for Spartan/XL FPGAs

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84 ⁽³⁾	VQ100 ⁽³⁾	CS144 ⁽³⁾	TQ144	PQ208	PQ240	BG256 ⁽³⁾	CS280 ⁽³⁾
XCS05	-3	C ⁽³⁾	C, I	-	-	-	-	-	-
	-4	C ⁽³⁾	C	-	-	-	-	-	-
XCS10	-3	C ⁽³⁾	C, I	-	C	-	-	-	-
	-4	C ⁽³⁾	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C ⁽³⁾	-	C, I	C, I	C	C ⁽³⁾	-
	-4	-	C ⁽³⁾	-	C	C	C	C ⁽³⁾	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C ⁽³⁾	C, I	-	-	-	-	-	-
	-5	C ⁽³⁾	C	-	-	-	-	-	-
XCS10XL	-4	C ⁽³⁾	C, I	C ⁽³⁾	C	-	-	-	-
	-5	C ⁽³⁾	C	C ⁽³⁾	C	-	-	-	-
XCS20XL	-4	-	C, I	C ⁽³⁾	C, I	C, I	-	-	-
	-5	-	C	C ⁽³⁾	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C ⁽³⁾
	-5	-	C	-	C	C	C	C	C ⁽³⁾
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C ⁽³⁾
	-5	-	-	-	-	C	C	C	C ⁽³⁾

6/25/08

Notes:

1. C = Commercial $T_J = 0^\circ$ to $+85^\circ\text{C}$
2. I = Industrial $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

www.xilinx.com/support/documentation/spartan-xl.htm#19687

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

www.xilinx.com/cgi-bin/thermal/thermal.pl

Table 20: User I/O Chart for Spartan/XL FPGAs

Device	Max I/O	Package Type							
		PC84 ⁽¹⁾	VQ100 ⁽¹⁾	CS144 ⁽¹⁾	TQ144	PQ208	PQ240	BG256 ⁽¹⁾	CS280 ⁽¹⁾
XCS05	80	61 ⁽¹⁾	77	-	-	-	-	-	-
XCS10	112	61 ⁽¹⁾	77	-	112	-	-	-	-
XCS20	160	-	77	-	113	160	-	-	-
XCS30	192	-	77 ⁽¹⁾	-	113	169	192	192 ⁽¹⁾	-
XCS40	224	-	-	-	-	169	192	205	-
XCS05XL	80	61 ⁽¹⁾	77 ⁽²⁾	-	-	-	-	-	-
XCS10XL	112	61 ⁽¹⁾	77 ⁽²⁾	112 ⁽¹⁾	112 ⁽²⁾	-	-	-	-
XCS20XL	160	-	77 ⁽²⁾	113 ⁽¹⁾	113 ⁽²⁾	160 ⁽²⁾	-	-	-
XCS30XL	192	-	77 ⁽²⁾	-	113 ⁽²⁾	169 ⁽²⁾	192 ⁽²⁾	192 ⁽²⁾	192 ⁽¹⁾
XCS40XL	224	-	-	-	-	169 ⁽²⁾	192 ⁽²⁾	205 ⁽²⁾	224 ⁽¹⁾

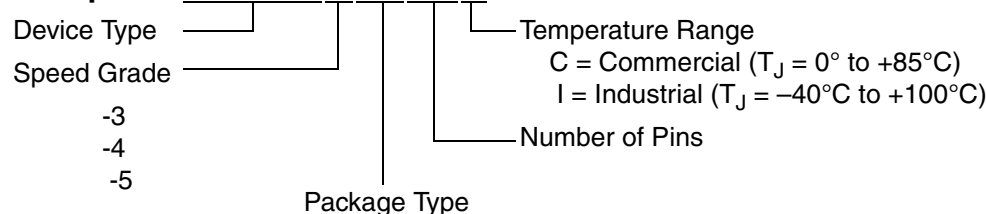
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Notes:

1. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
2. These Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Ordering Information

Example: XCS20XL-4 PQ208C



BG = Ball Grid Array

BGG = Ball Grid Array (Pb-free)

PC = Plastic Lead Chip Carrier

PQ = Plastic Quad Flat Pack

PQG = Plastic Quad Flat Pack (Pb-free)

VQ = Very Thin Quad Flat Pack

VQG = Very Thin Quad Flat Pack (Pb-free)

TQ = Thin Quad Flat Pack

TQG = Thin Quad Flat Pack (Pb-free)

CS = Chip Scale