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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	466
Total RAM Bits	6272
Number of I/O	112
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs10xl-5tq144c

Table 2: **CLB Storage Element Functionality**

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
	⟋	1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (Spartan-XL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X	Don't care
⟋	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
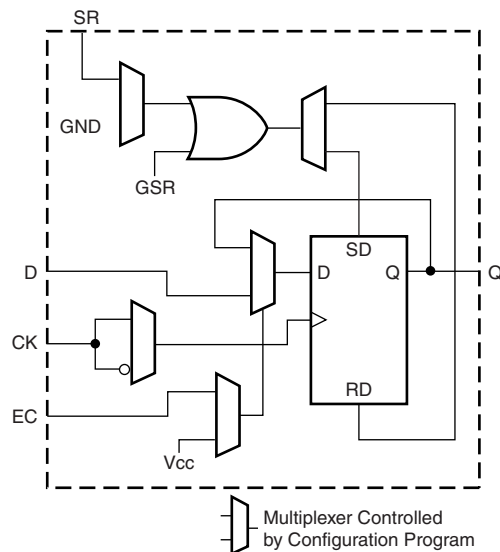
DS060_03_041901

Figure 3: **CLB Flip-Flop Functional Block Diagram**

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

CLB Signal Flow Control

In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2, page 4) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinatorial CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinatorial output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1-C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds,

using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.
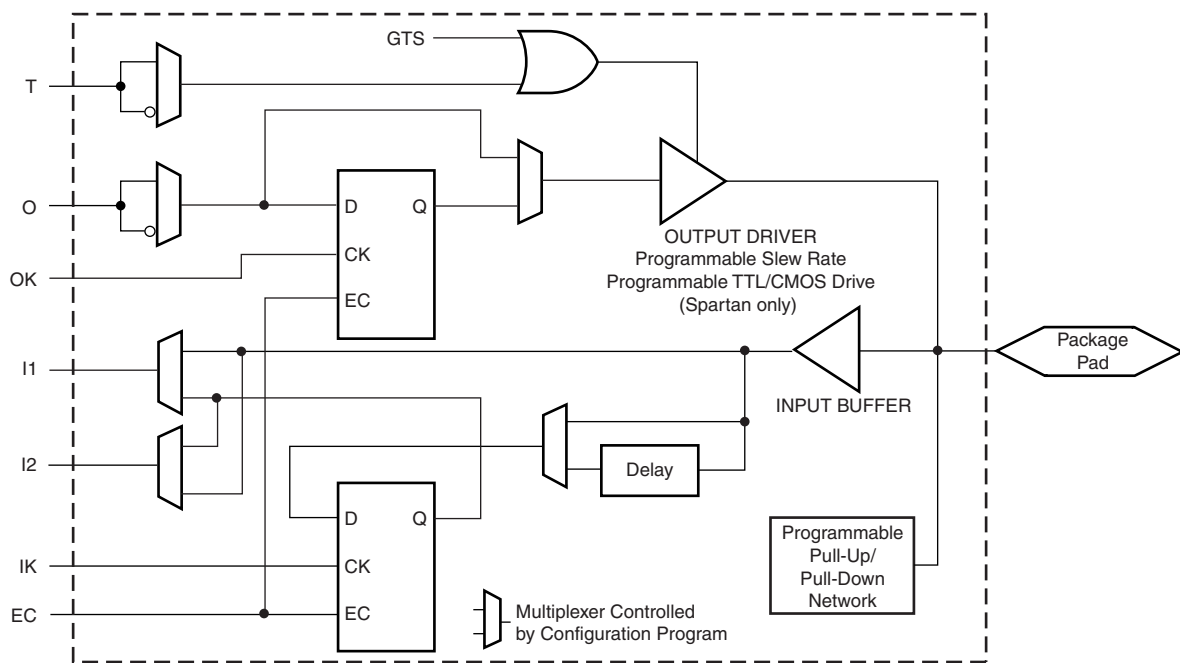
Figure 6: **Simplified Spartan/XL IOB Block Diagram**

Output Multiplexer/2-Input Function Generator (Spartan-XL Family Only)

The output path in the Spartan-XL family IOB contains an additional multiplexer not available in the Spartan family IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass gate, AND gate, OR gate, or XOR gate, with 0, 1, or 2 inverted inputs.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. The select input is the pin used for the output flip-flop clock, OK.

When the multiplexer is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe driven by a global buffer.

The user can specify that the IOB function generator be used by placing special library symbols beginning with the letter "O." For example, a 2-input AND gate in the IOB function generator is called OAND2. Use the symbol input pin labeled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in Figure 7.

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Figure 7: **AND and MUX Symbols in Spartan-XL IOB**

Output Buffer

An active High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (O) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB (see Figure 6, page 7). An output can be configured as open-drain (open-collector) by tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground.

By default, a 5V Spartan device output buffer pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below V_{CC}. Alternatively, the outputs can be globally configured as CMOS drivers, with additional p-channel pull-up transistors pulling to V_{CC}. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable.

All Spartan-XL device outputs are configured as CMOS drivers, therefore driving rail-to-rail. The Spartan-XL family outputs are individually programmable for 12 mA or 24 mA output drive.

Any 5V Spartan device with its outputs configured in TTL mode can drive the inputs of any typical 3.3V device. Supported destinations for Spartan/XL device outputs are shown in Table 7.

Three-State Register (Spartan-XL Family Only)

Spartan-XL devices incorporate an optional register controlling the three-state enable in the IOBs. The use of the three-state control register can significantly improve output enable and disable time.

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

Spartan/XL devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Pull-up and Pull-down Network

Programmable pull-up and pull-down resistors are used for tying unused pins to V_{CC} or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to V_{CC}. The configurable pull-down resistor is an n-channel transistor that pulls to Ground. The value of these resistors is typically 20 KΩ – 100 KΩ (See "Spartan Family DC Characteristics Over Operating Conditions" on page 43.).
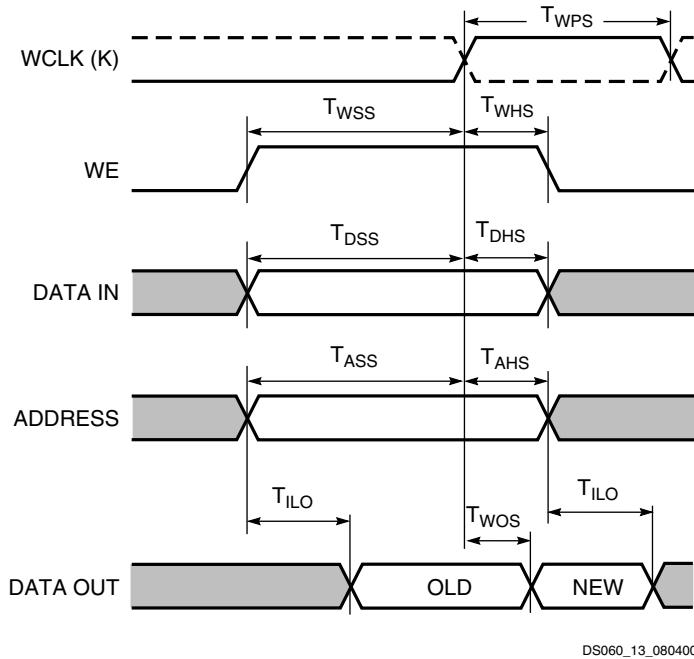
Figure 13: **Data Write and Access Timing for RAM**

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO}, the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS}, the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by A[3:0] while the second provides only for read operations at the address specified independently by DPRA[3:0]. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the
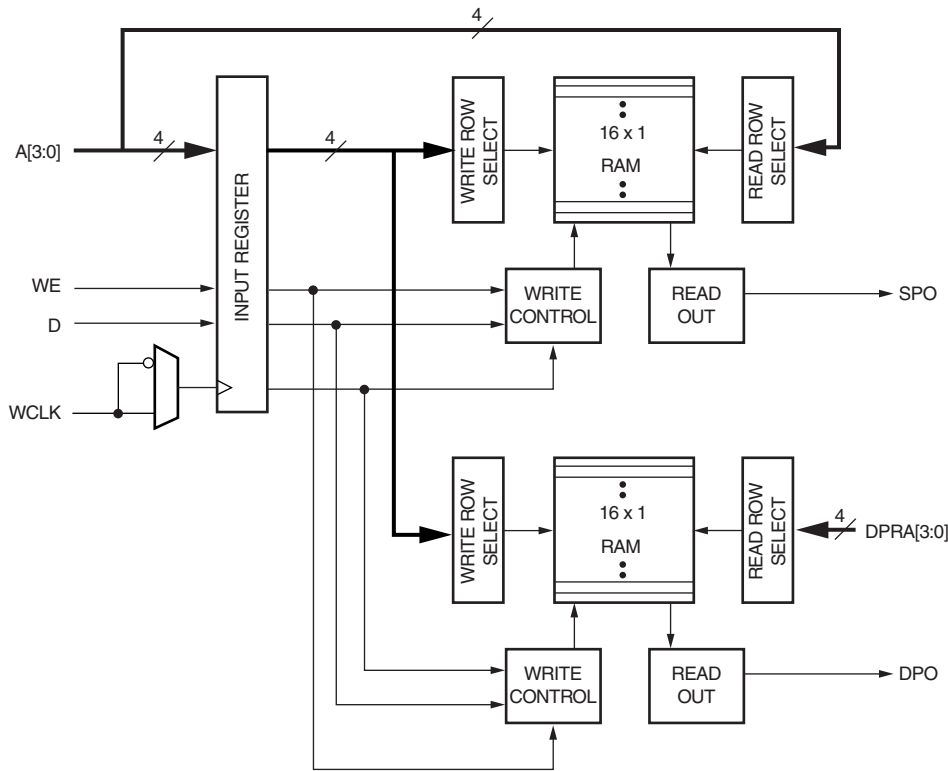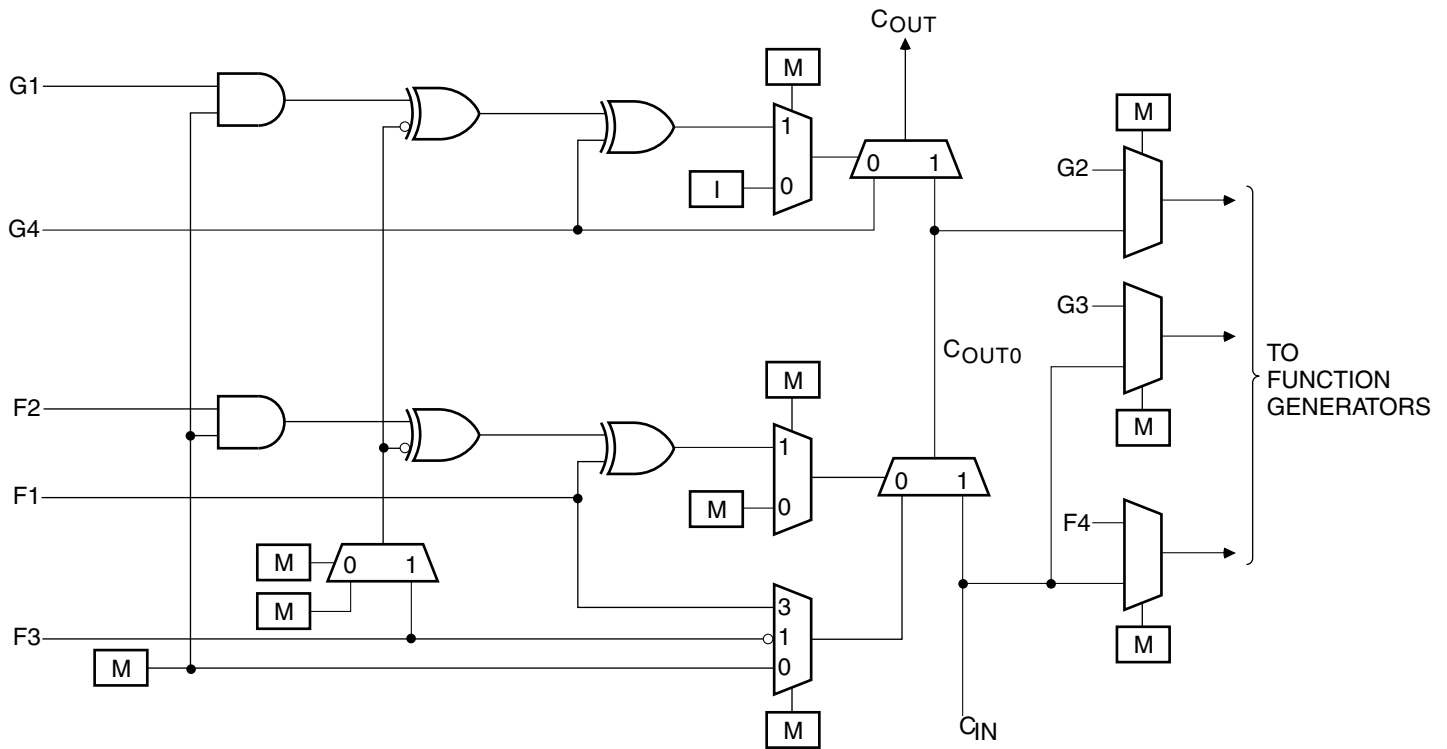

Figure 14: **Logic Diagram for the Dual-Port RAM**

Figure 17: **Detail of Spartan/XL Dedicated Carry Logic**

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal long-lines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

Table 11: **Three-State Buffer Functionality**

IN	T	OUT
X	1	Z
IN	0	IN

$$Z = (D_A \cdot \overline{A}) + (D_B \cdot \overline{B}) + (D_C \cdot \overline{C}) + (D_N \cdot \overline{N})$$
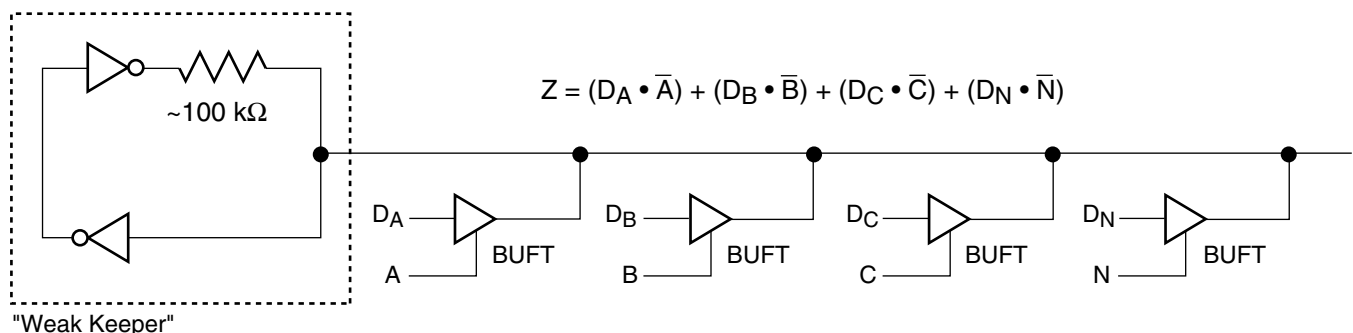
Figure 18: **3-state Buffers Implement a Multiplexer**

On-Chip Oscillator

Spartan/XL devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, V_{CC}, and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8-MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in Figure 3, page 5 for the CLB and Figure 5, page 6 for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 19.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

Global 3-State

A separate Global 3-state line (GTS) as shown in Figure 6, page 7 forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in Figure 19 for GSR except the IBUF would be connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-state signal. Alternatively, GTS can be driven from any internal node.
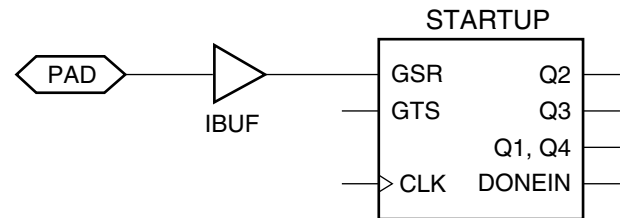
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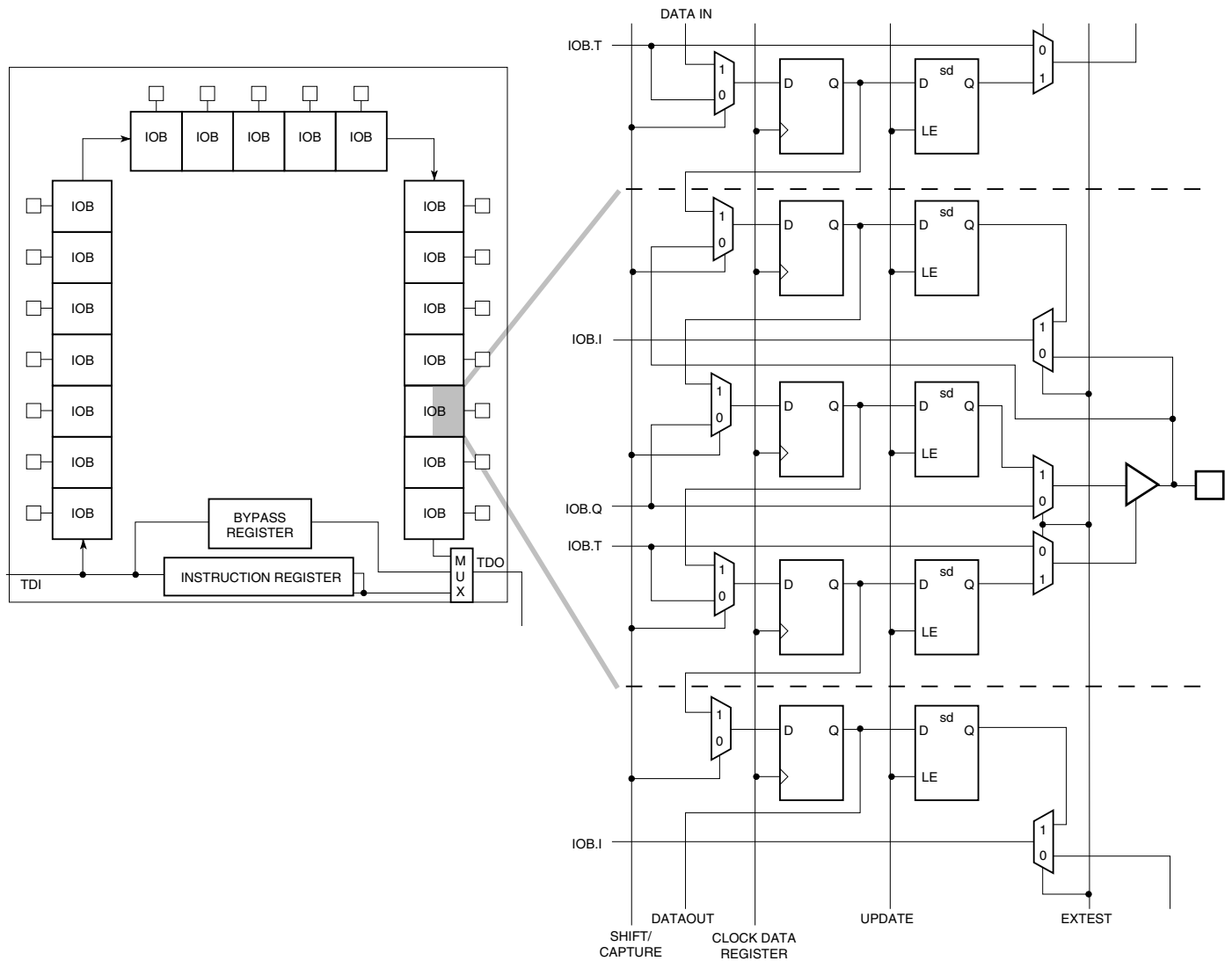*Figure 19:* **Symbols for Global Set/Reset**

Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan compatible device. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan and Spartan-XL families implement IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Spartan/XL devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "*Boundary Scan in FPGA Devices.*"

Figure 20: **Spartan/XL Boundary Scan Logic**

Description	Symbol	Min
Power Down Time	T_{PWD}	50 ns
Power Down Pulse Width	T_{PWDW}	50 ns
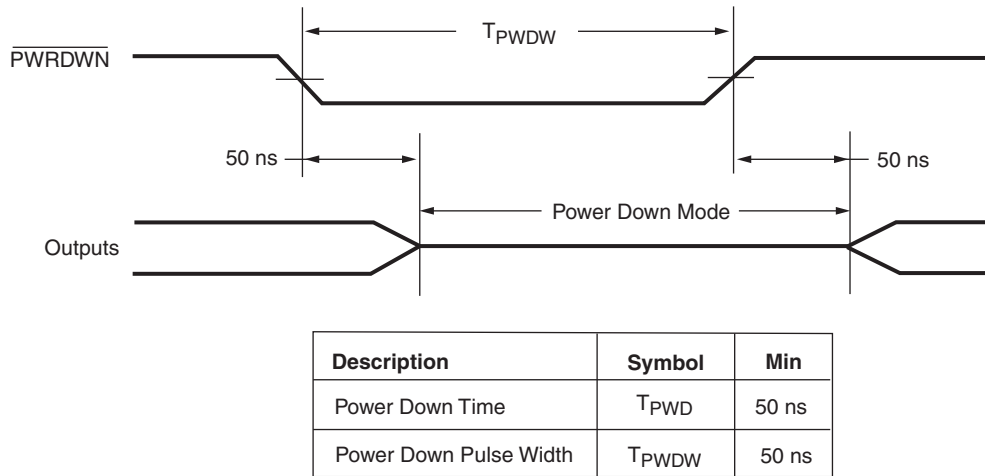
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Figure 23: $\overline{\text{PWRDWN}}$ **Pulse Timing**

Power-down retains the configuration, but loses all data stored in the device flip-flops. All inputs are interpreted as Low, but the internal combinatorial logic is fully functional. Make sure that the combination of all inputs Low and all flip-flops set or reset in your design will not generate internal oscillations, or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line.

During configuration, the $\overline{\text{PWRDWN}}$ pin must be High. If the Power Down state is entered before or during configuration, the device will restart configuration once the $\overline{\text{PWRDWN}}$ signal is removed. Note that the configuration pins are affected by Power Down and may not reflect their normal function. If there is an external pull-up resistor on the DONE pin, it will be High during Power Down even if the device is not yet configured. Similarly, if $\overline{\text{PWRDWN}}$ is asserted before configuration is completed, the $\overline{\text{INIT}}$ pin will not indicate status information.

Note that the $\overline{\text{PWRDWN}}$ pin is not part of the Boundary Scan chain. Therefore, the Spartan-XL family has a separate set of BSDL files than the 5V Spartan family. Boundary scan logic is not usable during Power Down.

Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan/XL devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Configuration Mode Control

5V Spartan devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

3V Spartan-XL devices have three configuration modes.

- M1/M0 = 11 sets Slave Serial mode
- M1/M0 = 10 sets Master Serial mode
- M1/M0 = 0X sets Express mode

In addition to these modes, the device can be configured through the Boundary Scan logic (See "Configuration Through the Boundary Scan Pins" on page 37.).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pin are unused. The Mode pins have a weak pull-up resistor turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the MODE/M0 pin should be connected directly to GND, or through a pull-down resistor of 1 KΩ or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during con-

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through

and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.
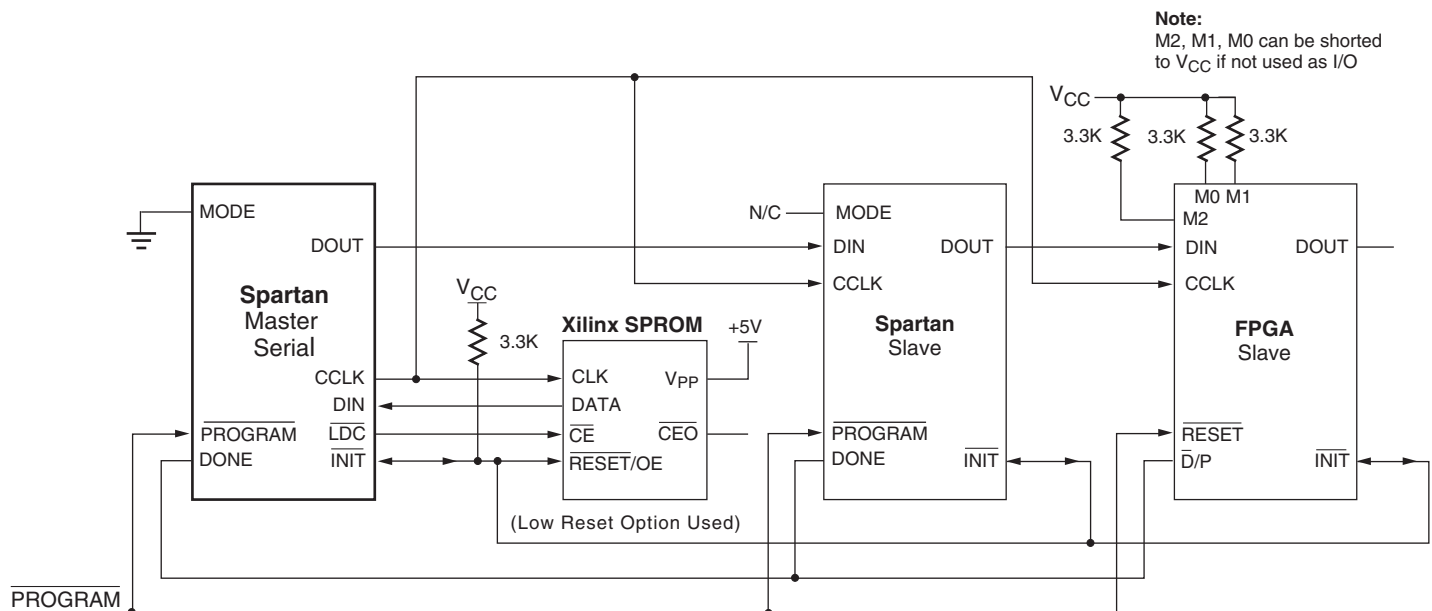
Figure 25: **Master/Slave Serial Mode Circuit Diagram**

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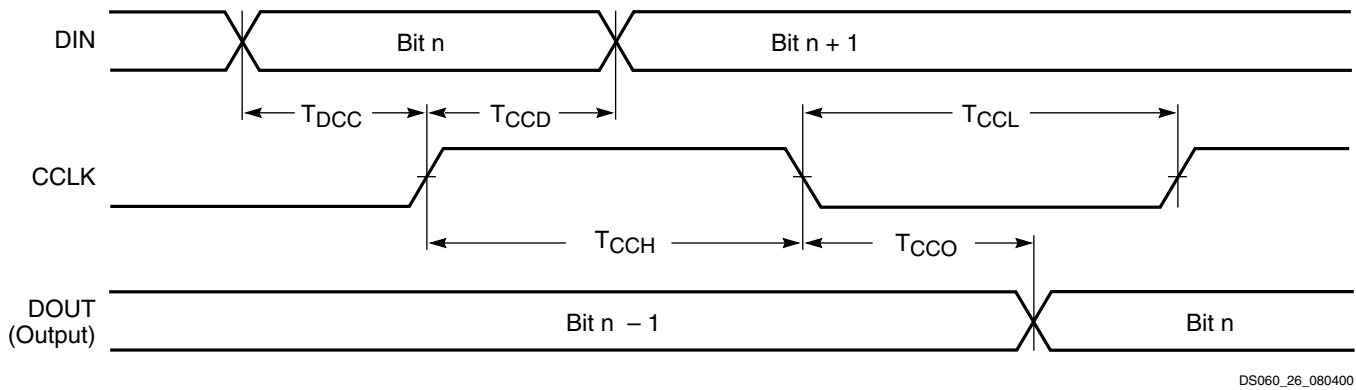
Symbol		Description	Min	Max	Units
T_{DCC}		DIN setup	20	-	ns
T_{CCD}		DIN hold	0	-	ns
T_{CCO}	CCLK	DIN to DOUT	-	30	ns
T_{CCH}		High time	40	-	ns
T_{CCL}		Low time	40	-	ns
F_{CC}		Frequency	-	12.5	MHz

Notes:
1. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 26: **Slave Serial Mode Programming Switching Characteristics**

Express Mode (Spartan-XL Family Only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

Pseudo Daisy Chain

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized

Table 16: **Spartan/XL Data Stream Formats**

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0][1]
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	11111110b[2]
Data Frame	DATA[n–1:0]	DATA[n–1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes[3]	FFh	FFFFFFFFFFFFFFFFh

Legend:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Notes:
1. Not used by configuration logic.
2. 11111111b for XCS40XL only.
3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the INIT pin. In Master serial mode, CCLK continues to operate externally. The user must detect INIT and initialize a new configuration by pulsing the PROGRAM pin Low or cycling V_CC.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the INIT pin Low and goes into a Wait state.

Polynomial: X16 + X15 + X2 + 1

Readback Data Stream
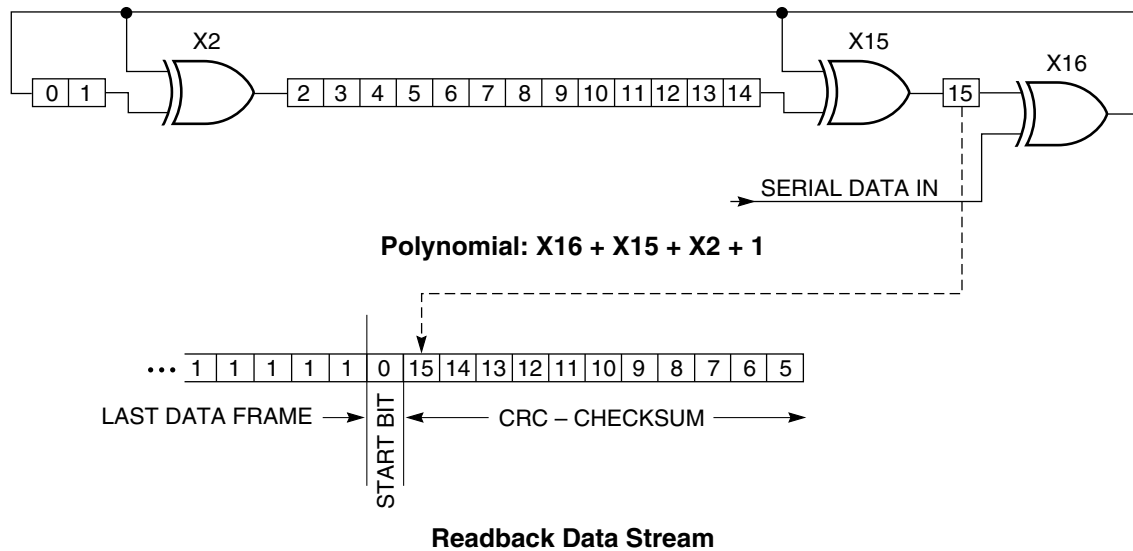
DS060_29_080400

Figure 29: **Circuit for Generating CRC-16**

Configuration Sequence

There are four major steps in the Spartan/XL FPGA power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC}. When all $\overline{INIT}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin

Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{INIT}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{LDC}$, $\overline{INIT}$ and DONE provide status outputs for the system interface. The outputs $\overline{LDC}$, $\overline{INIT}$ and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain $\overline{INIT}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive $\overline{INIT}$. Two internal clocks after the $\overline{INIT}$ pin is recognized as High, the device samples the MODE pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Configuration Switching Characteristics
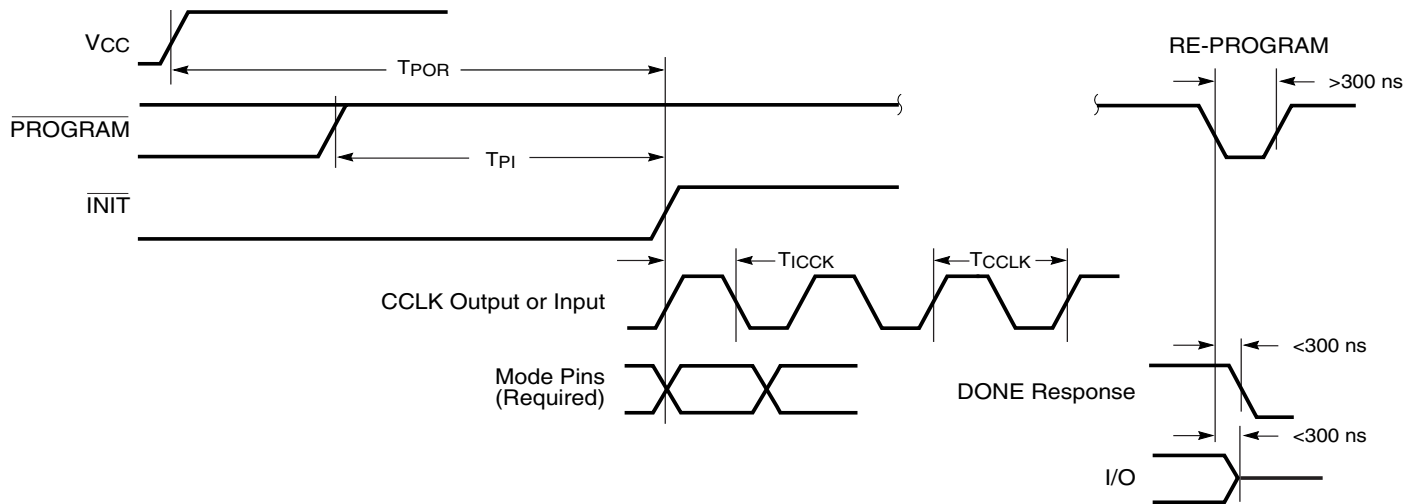
DS060_33_080400

Master Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	40	130	ms
T_{PI}	Program Latency	30	200	µs per CLB column
T_{ICCK}	CCLK (output) delay	40	250	µs
T_{CCLK}	CCLK (output) period, slow	640	2000	ns
T_{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	10	33	ms
T_{PI}	Program latency	30	200	µs per CLB column
T_{ICCK}	CCLK (input) delay (required)	4	-	µs
T_{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage @ I_{OH} = –1.0 mA, V_{CC} min	CMOS outputs	V_{CC} – 0.5	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min[1]	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		3.0	-	V
I_{CCO}	Quiescent FPGA supply current[2]	Commercial	-	3.0	mA
		Industrial	-	6.0	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)		-	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 5V (sample tested)		0.02	-	mA

Notes:
1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a Tie option.

Spartan Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

			Speed Grade		
			-4	-3	
Symbol	Description	Device	Max	Max	Units
T_{PG}	From pad through Primary buffer, to any clock K	XCS05	2.0	4.0	ns
		XCS10	2.4	4.3	ns
		XCS20	2.8	5.4	ns
		XCS30	3.2	5.8	ns
		XCS40	3.5	6.4	ns
T_{SG}	From pad through Secondary buffer, to any clock K	XCS05	2.5	4.4	ns
		XCS10	2.9	4.7	ns
		XCS20	3.3	5.8	ns
		XCS30	3.6	6.2	ns
		XCS40	3.9	6.7	ns

Spartan Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Spartan Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade -4 Max	Speed Grade -3 Max	Units
Global Primary Clock to TTL Output using OFF					
T_{ICKOF}	Fast	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
T_{ICKO}	Slew-rate limited	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
T_{ICKSOF}	Fast	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
T_{ICKSO}	Slew-rate limited	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
T_{CMOSOF}	Fast	All devices	0.8	1.0	ns
T_{CMOSO}	Slew-rate limited	All devices	1.5	2.0	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 34.
3. OFF = Output Flip-Flop

Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade -4 Min	Speed Grade -3 Min	Units
Input Setup/Hold Times Using Primary Clock and IFF					
T_{PSUF}/T_{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T_{PSU}/T_{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T_{SSUF}/T_{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T_{SSU}/T_{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:
1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

			Speed Grade				
			-4		**-3**		
Symbol	**Description**	**Device**	**Min**	**Max**	**Min**	**Max**	**Units**
Setup Times - TTL Inputs[1]							
T_{ECIK}	Clock Enable (EC) to Clock (IK), no delay	All devices	1.6	-	2.1	-	ns
T_{PICK}	Pad to Clock (IK), no delay	All devices	1.5	-	2.0	-	ns
Hold Times							
T_{IKEC}	Clock Enable (EC) to Clock (IK), no delay	All devices	0.0	-	0.9	-	ns
	All Other Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays - TTL Inputs[1]							
T_{PID}	Pad to I1, I2	All devices	-	1.5	-	2.0	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.8	-	3.6	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	2.7	-	2.8	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	3.2	-	3.9	ns
Delay Adder for Input with Delay Option							
T_{Delay}	$T_{ECIKD} = T_{ECIK} + T_{Delay}$ $T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	XCS05	3.6	-	4.0	-	ns
		XCS10	3.7	-	4.1	-	ns
		XCS20	3.8	-	4.2	-	ns
		XCS30	4.5	-	5.0	-	ns
		XCS40	5.5	-	5.5	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	11.5	-	13.5	-	ns
T_{RRI}	Delay from GSR input to any Q	XCS05	-	9.0	-	11.3	ns
		XCS10	-	9.5	-	11.9	ns
		XCS20	-	10.0	-	12.5	ns
		XCS30	-	10.5	-	13.1	ns
		XCS40	-	11.0	-	13.8	ns

Notes:
1. Delay adder for CMOS Inputs option: for -3 speed grade, add 0.4 ns; for -4 speed grade, add 0.2 ns.
2. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
3. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade		Units
			-5	**-4**	
			Max	Max	
T_{GLS}	From pad through buffer, to any clock K	XCS05XL	1.4	1.5	ns
		XCS10XL	1.7	1.8	ns
		XCS20XL	2.0	2.1	ns
		XCS30XL	2.3	2.5	ns
		XCS40XL	2.6	2.8	ns

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

			Speed Grade				
			-5		-4		
Symbol	Single Port RAM	Size[1]	Min	Max	Min	Max	Units
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	7.7	-	8.4	-	ns
T_{WCTS}		32x1	7.7	-	8.4	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	3.1	-	3.6	-	ns
T_{WPTS}		32x1	3.1	-	3.6	-	ns
T_{ASS}	Address setup time before clock K	16x2	1.3	-	1.5	-	ns
T_{ASTS}		32x1	1.5	-	1.7	-	ns
T_{DSS}	DIN setup time before clock K	16x2	1.5	-	1.7	-	ns
T_{DSTS}		32x1	1.8	-	2.1	-	ns
T_{WSS}	WE setup time before clock K	16x2	1.4	-	1.6	-	ns
T_{WSTS}		32x1	1.3	-	1.5	-	ns
	All hold times after clock K	16x2	0.0	-	0.0	-	ns
T_{WOS}	Data valid after clock K	32x1	-	4.5	-	5.3	ns
T_{WOTS}		16x2	-	5.4	-	6.3	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	2.6	-	3.1	-	ns
T_{RCT}		32x1	3.8	-	5.5	-	ns
T_{ILO}	Data Valid after address change (no Write Enable)	16x2	-	1.0	-	1.1	ns
T_{IHO}		32x1	-	1.7	-	2.0	ns
T_{ICK}	Address setup time before clock K	16x2	0.6	-	0.7	-	ns
T_{IHCK}		32x1	1.3	-	1.6	-	ns

Notes:
1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7[2])	P53	L12	P75	P107	367 [3]
I/O, PGCK3[1], GCK5[2]	P54	L13	P76	P108	370 [3]
I/O	-	K10	P77	P109	373 [3]
I/O	-	K11	P78	P110	376 [3]
I/O (D6[2])	P55	K12	P79	P112	379 [3]
I/O	P56	K13	P80	P113	382 [3]
I/O	-	-	-	P114	385 [3]
I/O	-	-	-	P115	388 [3]
I/O	-	-	-	P116	391 [3]
I/O	-	-	-	P117	394 [3]
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 [3]
I/O	-	J12	P83	P120	400 [3]
VCC[2]	-	-	-	P121	-
I/O (D5[2])	P57	J13	P84	P122	403 [3]
I/O	P58	H10	P85	P123	406 [3]
I/O	-	-	-	P124	409 [3]
I/O	-	-	-	P125	412 [3]
I/O	P59	H11	P86	P126	415 [3]
I/O	P60	H12	P87	P127	418 [3]
I/O (D4[2])	P61	H13	P88	P128	421 [3]
I/O	P62	G12	P89	P129	424 [3]
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3[2])	P65	G10	P92	P132	427 [3]
I/O	P66	F13	P93	P133	430 [3]
I/O	P67	F12	P94	P134	433 [3]
I/O	-	F11	P95	P135	436 [3]
I/O	-	-	-	P136	439 [3]
I/O	-	-	-	P137	442 [3]
I/O (D2[2])	P68	F10	P96	P138	445 [3]
I/O	P69	E13	P97	P139	448 [3]
VCC[2]	-	-	-	P140	-
I/O	-	E12	P98	P141	451 [3]
I/O	-	E11	P99	P142	454 [3]
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 [3]
I/O	-	-	-	P146	460 [3]
I/O	-	-	-	P147	463 [3]
I/O	-	-	-	P148	466 [3]
I/O (D1[2])	P70	D13	P101	P149	469 [3]
I/O	P71	D12	P102	P150	472 [3]
I/O	-	D11	P103	P151	475 [3]

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 [3]
I/O (D0[2], DIN)	P72	C12	P105	P153	481 [3]
I/O, SGCK4[1], GCK6[2] (DOUT)	P73	C11	P106	P154	484 [3]
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4[1], GCK7[2]	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1[2])	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC[2]	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

2/8/00