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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	950
Total RAM Bits	12800
Number of I/O	160
Number of Gates	20000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcs20-3pq208c">https://www.e-xfl.com/product-detail/xilinx/xcs20-3pq208c</a>

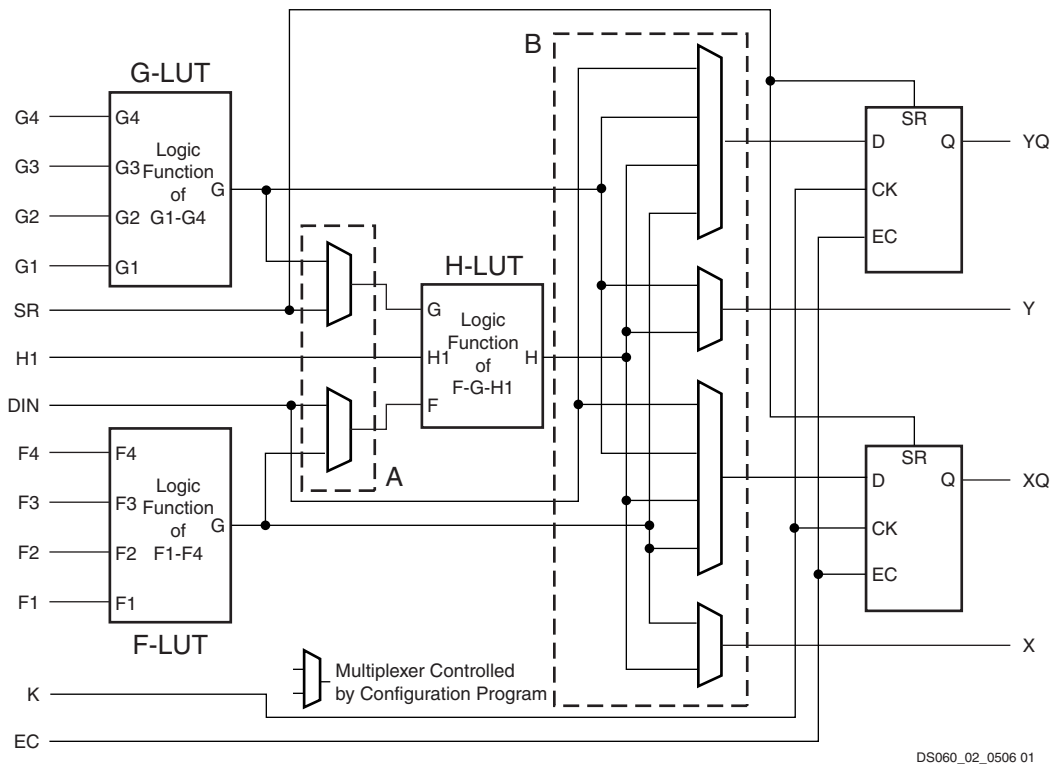


Figure 2: Spartan/XL Simplified CLB Logic Diagram (some features not shown)

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

**Note:** When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

### Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.

### Latches (Spartan-XL Family Only)

The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.

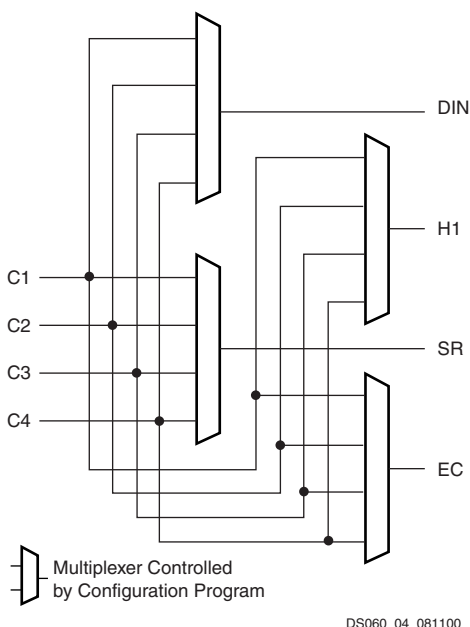


Figure 4: CLB Control Signal Interface

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

## Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

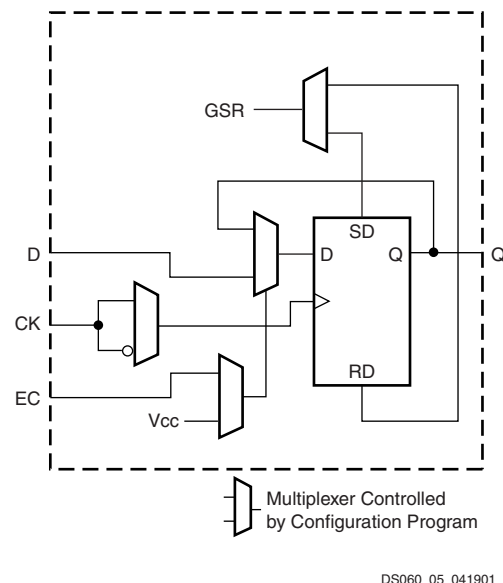


Figure 5: IOB Flip-Flop/Latch Functional Block Diagram

## IOB Input Signal Path

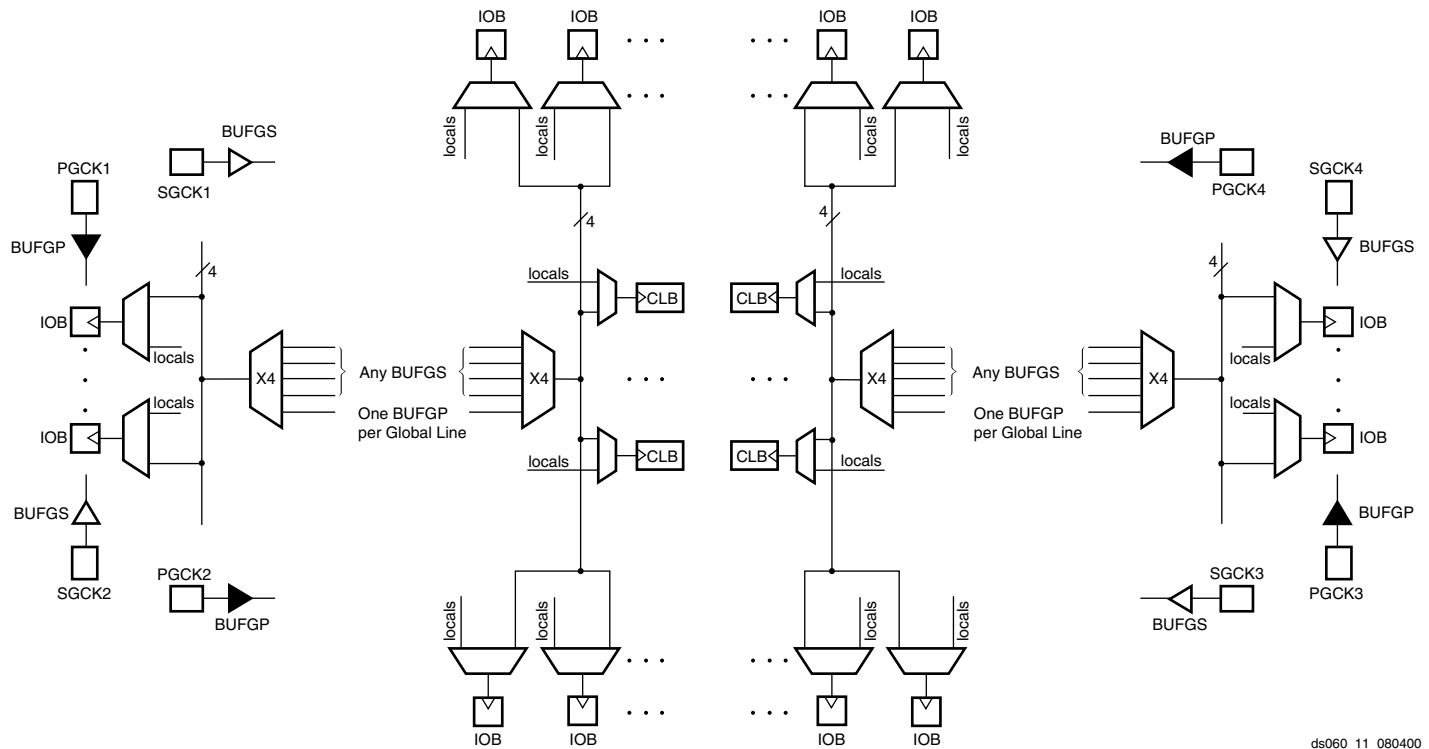
The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: Input Register Functionality

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop		1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

### Legend:

- X Don't care.
- Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0\* Input is Low or unconnected (default value)
- 1\* Input is High or unconnected (default value)



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Figure 11: 5V Spartan Family Global Net Distribution

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

## Advanced Features Description

### Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

### Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 8. Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 8: CLB Memory Configurations

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√	—	—

CLB signals from which they are originally derived are shown in Table 10.

Table 10: Dual-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F <sub>OUT</sub>
DPO	Dual Port Out (addressed by DPRA[3:0])	G <sub>OUT</sub>

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

### Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

### More Information on Using RAM Inside CLBs

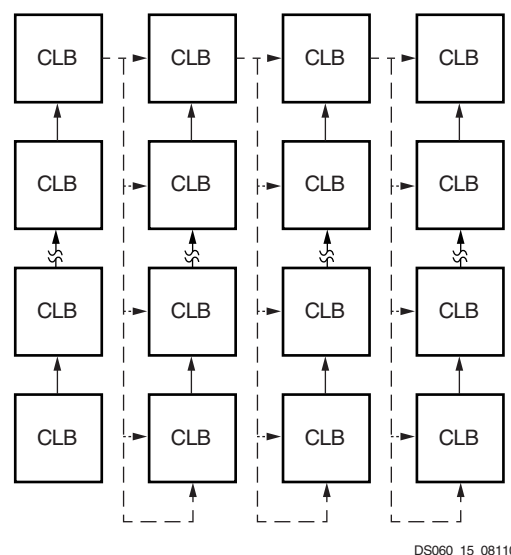
Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both the Spartan and the Spartan-XL families.

### Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in micro-processor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan



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Figure 15: Available Spartan/XL Carry Propagation Paths

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

### Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

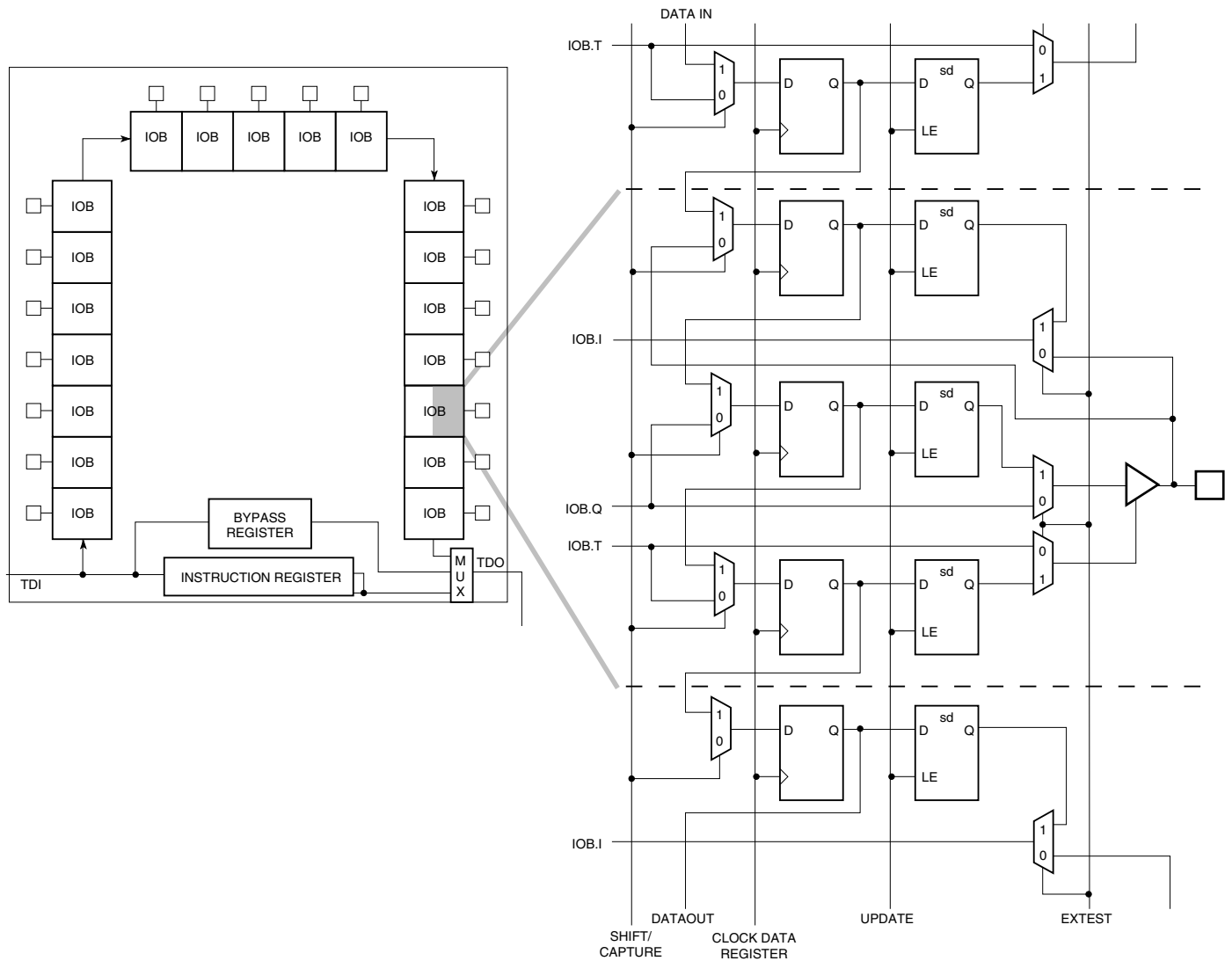
The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

### Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.



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Figure 20: Spartan/XL Boundary Scan Logic

figuration are shown in Table 14 and Table 15.

**Table 14: Pin Functions During Configuration (Spartan Family Only)**

Configuration Mode (MODE Pin)		User Operation
Slave Serial (High)	Master Serial (Low)	
MODE (I)	MODE (I)	MODE
HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

**Notes:**

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3.  $\overline{\text{INIT}}$  is an open-drain output during configuration.

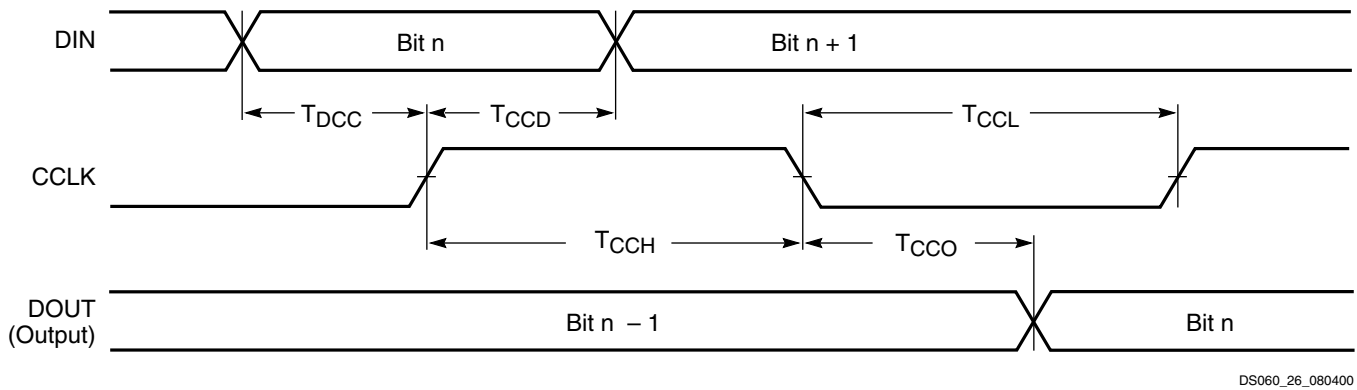
**Table 15: Pin Functions During Configuration (Spartan-XL Family Only)**

CONFIGURATION MODE <M1:M0>			User Operation
Slave Serial [1:1]	Master Serial [1:0]	Express [0:X]	
M1 (High) (I)	M1 (High) (I)	M1(Low) (I)	M1
M0 (High) (I)	M0 (Low) (I)	M0 (I)	M0
HDC (High)	HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

**Notes:**

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3.  $\overline{\text{INIT}}$  is an open-drain output during configuration.





Symbol		Description	Min	Max	Units
$T_{DCC}$	CCLK	DIN setup	20	-	ns
$T_{CCD}$		DIN hold	0	-	ns
$T_{CCO}$		DIN to DOUT	-	30	ns
$T_{CCH}$		High time	40	-	ns
$T_{CCL}$		Low time	40	-	ns
$F_{CC}$		Frequency	-	12.5	MHz

**Notes:**

1. Configuration must be delayed until the  $\overline{INIT}$  pins of all daisy-chained FPGAs are High.

Figure 26: Slave Serial Mode Programming Switching Characteristics

## Express Mode (Spartan-XL Family Only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

### Pseudo Daisy Chain

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices

are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized

Table 16: Spartan/XL Data Stream Formats

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0] <sup>(1)</sup>
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	11111110b <sup>(2)</sup>
Data Frame	DATA[n-1:0]	DATA[n-1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes <sup>(3)</sup>	FFh	FFFFFFFFFFFFFFh

**Legend:**

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

**Notes:**

1. Not used by configuration logic.
2. 11111111b for XCS40XL only.
3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the  $\overline{\text{INIT}}$  pin. In Master serial mode, CCLK continues to operate externally. The user must detect  $\overline{\text{INIT}}$  and initialize a new configuration by pulsing the PROGRAM pin Low or cycling VCC.

**Cyclic Redundancy Check (CRC) for Configuration and Readback**

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the  $\overline{\text{INIT}}$  pin Low and goes into a Wait state.

## Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in [Figure 32](#).

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low)

of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

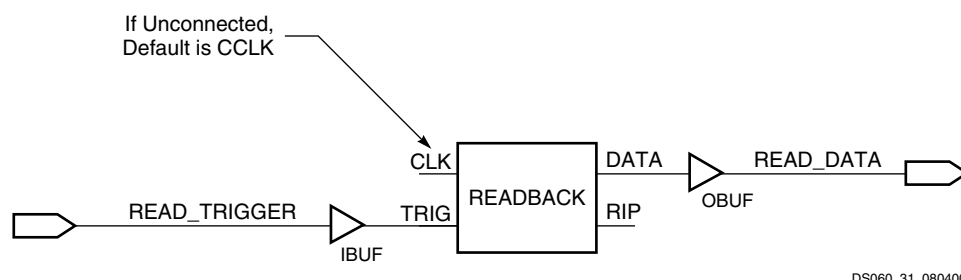
### Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

### Readback Capture

When the Readback Capture option is selected, the data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.



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Figure 32: Readback Example

### Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

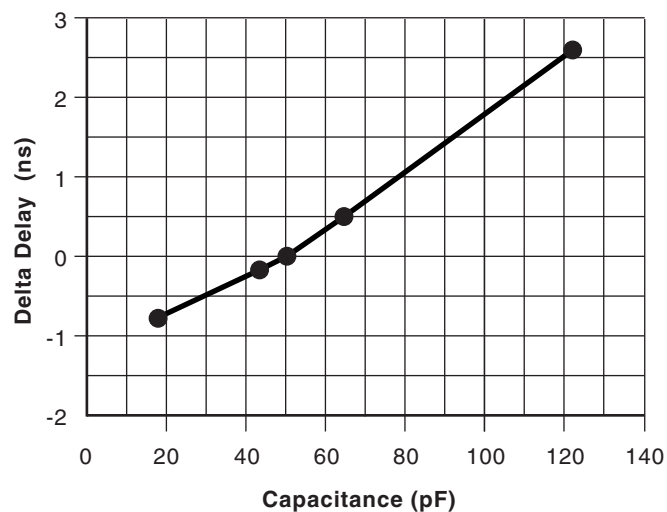
Symbol	Single Port RAM	Size <sup>(1)</sup>	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Write Operation							
T <sub>WCS</sub>	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T <sub>WCTS</sub>		32x1	8.0	-	11.6	-	ns
T <sub>WPS</sub>	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T <sub>WPTS</sub>		32x1	4.0	-	5.8	-	ns
T <sub>ASS</sub>	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T <sub>ASTS</sub>		32x1	1.5	-	2.0	-	ns
T <sub>AHS</sub>	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T <sub>AHTS</sub>		32x1	0.0	-	0.0	-	ns
T <sub>DSS</sub>	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T <sub>DSTS</sub>		32x1	1.5	-	1.7	-	ns
T <sub>DHS</sub>	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T <sub>DHTS</sub>		32x1	0.0	-	0.0	-	ns
T <sub>WSS</sub>	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T <sub>WSTS</sub>		32x1	1.5	-	1.6	-	ns
T <sub>WHS</sub>	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T <sub>WHTS</sub>		32x1	0.0	-	0.0	-	ns
T <sub>WOS</sub>	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T <sub>WOTS</sub>		32x1	-	7.0	-	9.3	ns
Read Operation							
T <sub>RC</sub>	Address read cycle time	16x2	2.6	-	2.6	-	ns
T <sub>RCT</sub>		32x1	3.8	-	3.8	-	ns
T <sub>ILO</sub>	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T <sub>IHO</sub>		32x1	-	2.0	-	2.7	ns
T <sub>ICK</sub>	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T <sub>IHCK</sub>		32x1	2.9	-	3.9	-	ns

#### Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

### Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



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Figure 34: Delay Factor at Various Capacitive Loads

### Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Typ.	Max	Units
V <sub>OH</sub>	High-level output voltage @ I <sub>OH</sub> = −4.0 mA, V <sub>CC</sub> min (LVTTL)		2.4	-	-	V
	High-level output voltage @ I <sub>OH</sub> = −500 μA, (LVCMOS)		90% V <sub>CC</sub>	-	-	V
V <sub>OL</sub>	Low-level output voltage @ I <sub>OL</sub> = 12.0 mA, V <sub>CC</sub> min (LVTTL) <sup>(1)</sup>		-	-	0.4	V
	Low-level output voltage @ I <sub>OL</sub> = 24.0 mA, V <sub>CC</sub> min (LVTTL) <sup>(2)</sup>		-	-	0.4	V
	Low-level output voltage @ I <sub>OL</sub> = 1500 μA, (LVCMOS)		-	-	10% V <sub>CC</sub>	V
V <sub>DR</sub>	Data retention supply voltage (below which configuration data may be lost)		2.5	-	-	V
I <sub>CCO</sub>	Quiescent FPGA supply current <sup>(3,4)</sup>	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I <sub>CCPD</sub>	Power Down FPGA supply current <sup>(3,5)</sup>	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I <sub>L</sub>	Input or output leakage current		−10	-	10	μA
C <sub>IN</sub>	Input capacitance (sample tested)		-	-	10	pF
I <sub>RPU</sub>	Pad pull-up (when selected) @ V <sub>IN</sub> = 0V (sample tested)		0.02	-	0.25	mA
I <sub>RPD</sub>	Pad pull-down (when selected) @ V <sub>IN</sub> = 3.3V (sample tested)		0.02	-	-	mA

#### Notes:

1. With up to 64 pins simultaneously sinking 12 mA (default mode).
2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
4. With no output current loads, no active input resistors, and all package pins at  $V_{CC}$  or GND.
5. With  $\overline{PWRDWN}$  active.

### Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current  $I_{CCPO}$  be provided to the  $V_{CC}$  lines for a successful power on. If more current is available, the FPGA can consume more than  $I_{CCPO}$  min., though this cannot adversely affect reliability.

A maximum limit for  $I_{CCPO}$  is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of  $I_{CCPO}$  by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Max	Units
$I_{CCPO}$	Total $V_{CC}$ supply current required during power-on	100	-	mA
$T_{CCPO}$	$V_{CC}$ ramp time <sup>(2,3)</sup>	-	50	ms

#### Notes:

1. The  $I_{CCPO}$  requirement applies for a brief time (commonly only a few milliseconds) when  $V_{CC}$  ramps from 0 to 3.3V.
2. The ramp time is measured from GND to  $V_{CC}$  max on a fully loaded board.
3.  $V_{CC}$  must not dip in the negative direction during power on.

## Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size <sup>(1)</sup>	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Write Operation							
T <sub>WCS</sub>	Address write cycle time (clock K period)	16x2	7.7	-	8.4	-	ns
T <sub>WCTS</sub>		32x1	7.7	-	8.4	-	ns
T <sub>WPS</sub>	Clock K pulse width (active edge)	16x2	3.1	-	3.6	-	ns
T <sub>WPTS</sub>		32x1	3.1	-	3.6	-	ns
T <sub>ASS</sub>	Address setup time before clock K	16x2	1.3	-	1.5	-	ns
T <sub>ASTS</sub>		32x1	1.5	-	1.7	-	ns
T <sub>DSS</sub>	DIN setup time before clock K	16x2	1.5	-	1.7	-	ns
T <sub>DSTS</sub>		32x1	1.8	-	2.1	-	ns
T <sub>WSS</sub>	WE setup time before clock K	16x2	1.4	-	1.6	-	ns
T <sub>WSTS</sub>		32x1	1.3	-	1.5	-	ns
	All hold times after clock K	16x2	0.0	-	0.0	-	ns
T <sub>WOS</sub>	Data valid after clock K	32x1	-	4.5	-	5.3	ns
T <sub>WOTS</sub>		16x2	-	5.4	-	6.3	ns
Read Operation							
T <sub>RC</sub>	Address read cycle time	16x2	2.6	-	3.1	-	ns
T <sub>RCT</sub>		32x1	3.8	-	5.5	-	ns
T <sub>ILO</sub>	Data Valid after address change (no Write Enable)	16x2	-	1.0	-	1.1	ns
T <sub>IHO</sub>		32x1	-	1.7	-	2.0	ns
T <sub>ICK</sub>	Address setup time before clock K	16x2	0.6	-	0.7	-	ns
T <sub>IHCK</sub>		32x1	1.3	-	1.6	-	ns

### Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

### Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to

the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Propagation Delays							
T <sub>OKPOF</sub>	Clock (OK) to Pad, fast	All devices	-	3.2	-	3.7	ns
T <sub>OPF</sub>	Output (O) to Pad, fast	All devices	-	2.5	-	2.9	ns
T <sub>TSHZ</sub>	3-state to Pad High-Z (slew-rate independent)	All devices	-	2.8	-	3.3	ns
T <sub>TSONF</sub>	3-state to Pad active and valid, fast	All devices	-	2.6	-	3.0	ns
T <sub>OFFPF</sub>	Output (O) to Pad via Output MUX, fast	All devices	-	3.7	-	4.4	ns
T <sub>OKFPF</sub>	Select (OK) to Pad via Output MUX, fast	All devices	-	3.3	-	3.9	ns
T <sub>SLOW</sub>	For Output SLOW option add	All devices	-	1.5	-	1.7	ns
Setup and Hold Times							
T <sub>OOK</sub>	Output (O) to clock (OK) setup time	All devices	0.5	-	0.5	-	ns
T <sub>OKO</sub>	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T <sub>ECOK</sub>	Clock Enable (EC) to clock (OK) setup time	All devices	0.0	-	0.0	-	ns
T <sub>OKEC</sub>	Clock Enable (EC) to clock (OK) hold time	All devices	0.1	-	0.2	-	ns
Global Set/Reset							
T <sub>MRW</sub>	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T <sub>RPO</sub>	Delay from GSR input to any Pad	XCS05XL	-	11.9	-	14.0	ns
		XCS10XL	-	12.4	-	14.5	ns
		XCS20XL	-	12.9	-	15.0	ns
		XCS30XL	-	13.9	-	16.0	ns
		XCS40XL	-	14.9	-	17.0	ns

#### Notes:

- Output timing is measured at ~50%  $V_{CC}$  threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
- Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.



### Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 <sup>(1)</sup>	P33 <sup>(1)</sup>	P39	P65	P71 <sup>(1)</sup>
P86 <sup>(1)</sup>	P92	P111	P121 <sup>(1)</sup>	P140 <sup>(1)</sup>	P144
P165	P173 <sup>(1)</sup>	P192 <sup>(1)</sup>	P202	P203	-
9/16/98					

#### Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by [PDN2004-01](#)

### XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100 <sup>(5)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(5)</sup>	CS280 <sup>(2,5)</sup>	Bndry Scan
VCC	P89	P128	P183	P212	VCC <sup>(4)</sup>	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC <sup>(4)</sup>	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1 <sup>(1)</sup> , GCK8 <sup>(2)</sup>	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC <sup>(4)</sup>	A1	-
GND	P1	P1	P1	P1	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O, PGCK1 <sup>(1)</sup> , GCK1 <sup>(2)</sup>	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

### XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 <sup>(5)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(5)</sup>	CS280 <sup>(2,5)</sup>	Bndry Scan
I/O	-	-	P124	P144	M20	L19	493 <sup>(3)</sup>
I/O	-	-	P125	P145	L19	L18	496 <sup>(3)</sup>
I/O	P59	P86	P126	P146	L18	L17	499 <sup>(3)</sup>
I/O	P60	P87	P127	P147	L20	L16	502 <sup>(3)</sup>
I/O (D4 <sup>(2)</sup> )	P61	P88	P128	P148	K20	K19	505 <sup>(3)</sup>
I/O	P62	P89	P129	P149	K19	K18	508 <sup>(3)</sup>
VCC	P63	P90	P130	P150	VCC <sup>(4)</sup>	K17	-
GND	P64	P91	P131	P151	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O (D3 <sup>(2)</sup> )	P65	P92	P132	P152	K18	K16	511 <sup>(3)</sup>
I/O	P66	P93	P133	P153	K17	K15	514 <sup>(3)</sup>
I/O	P67	P94	P134	P154	J20	J19	517 <sup>(3)</sup>
I/O	-	P95	P135	P155	J19	J18	520 <sup>(3)</sup>
I/O	-	-	P136	P156	J18	J17	523 <sup>(3)</sup>
I/O	-	-	P137	P157	J17	J16	526 <sup>(3)</sup>
I/O (D2 <sup>(2)</sup> )	P68	P96	P138	P159	H19	H17	529 <sup>(3)</sup>
I/O	P69	P97	P139	P160	H18	H16	532 <sup>(3)</sup>
VCC	-	-	P140	P161	VCC <sup>(4)</sup>	G19	-
I/O	-	P98	P141	P162	G19	G18	535 <sup>(3)</sup>
I/O	-	P99	P142	P163	F20	G17	538 <sup>(3)</sup>
I/O	-	-	-	P164	G18	G16	541 <sup>(3)</sup>
I/O	-	-	-	P165	F19	F19	544 <sup>(3)</sup>
GND	-	P100	P143	P166	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	-	-	-	P167	F18	F18	547 <sup>(3)</sup>
I/O	-	-	P144	P168	E19	F17	550 <sup>(3)</sup>
I/O	-	-	P145	P169	D20	F16	553 <sup>(3)</sup>
I/O	-	-	P146	P170	E18	F15	556 <sup>(3)</sup>
I/O	-	-	P147	P171	D19	E19	559 <sup>(3)</sup>
I/O	-	-	P148	P172	C20	E17	562 <sup>(3)</sup>
I/O (D1 <sup>(2)</sup> )	P70	P101	P149	P173	E17	E16	565 <sup>(3)</sup>
I/O	P71	P102	P150	P174	D18	D19	568 <sup>(3)</sup>
I/O	-	P103	P151	P175	C19	C19	571 <sup>(3)</sup>
I/O	-	P104	P152	P176	B20	B19	574 <sup>(3)</sup>
I/O (D0 <sup>(2)</sup> , DIN)	P72	P105	P153	P177	C18	C18	577 <sup>(3)</sup>
I/O, SGCK4 <sup>(1)</sup> , GCK6 <sup>(2)</sup> (DOUT)	P73	P106	P154	P178	B19	B18	580 <sup>(3)</sup>
CCLK	P74	P107	P155	P179	A20	A19	-
VCC	P75	P108	P156	P180	VCC <sup>(4)</sup>	C17	-
O, TDO	P76	P109	P157	P181	A19	B17	0
GND	P77	P110	P158	P182	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P78	P111	P159	P183	B18	A18	2
I/O, PGCK4 <sup>(1)</sup> , GCK7 <sup>(2)</sup>	P79	P112	P160	P184	B17	A17	5
I/O	-	P113	P161	P185	C17	D16	8
I/O	-	P114	P162	P186	D16	C16	11
I/O (CS1) <sup>(2)</sup>	P80	P115	P163	P187	A18	B16	14
I/O	P81	P116	P164	P188	A17	A16	17
I/O	-	-	P165	P189	C16	D15	20

### CS280

VCC Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-
Not Connected Pins					
A4	A12	C8	C12	C15	D1
D2	D5	D8	D17	D18	E15
H2	H3	H18	H19	L4	M1
M16	M18	R2	R4	R5	R15
R17	T8	T15	U5	V8	V12
W12	W16	-	-	-	-
Not Connected Pins (VCC in XCS40XL)					
B5	B15	E3	E18	R3	R18
V5	V15	-	-	-	-

5/21/02

### XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 <sup>(2,5)</sup>	Bndry Scan
VCC	P183	P212	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	P184	P213	C10	D10	86
I/O	P185	P214	D10	E10	89
I/O	P186	P215	A9	A9	92
I/O	P187	P216	B9	B9	95
I/O	P188	P217	C9	C9	98
I/O	P189	P218	D9	D9	101
I/O	P190	P220	A8	A8	104
I/O	P191	P221	B8	B8	107
I/O	-	-	C8	C8	110
I/O	-	-	A7	D8	113
VCC	P192	P222	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	-	P223	A6	B7	116
I/O	-	P224	C7	C7	119
I/O	P193	P225	B6	D7	122
I/O	P194	P226	A5	A6	125
GND	P195	P227	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P196	P228	C6	B6	128
I/O	P197	P229	B5	C6	131
I/O	P198	P230	A4	D6	134
I/O	P199	P231	C5	E6	137

### XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 <sup>(2,5)</sup>	Bndry Scan
I/O	P200	P232	B4	A5	140
I/O	P201	P233	A3	C5	143
I/O	-	-	-	D5	146
I/O	-	-	-	A4	149
I/O	P202	P234	D5	B4	152
I/O	P203	P235	C4	C4	155
I/O	P204	P236	B3	A3	158
I/O	P205	P237	B2	A2	161
I/O	P206	P238	A2	B3	164
I/O, SGCK1 <sup>(1)</sup> , GCK8 <sup>(2)</sup>	P207	P239	C3	B2	167
VCC	P208	P240	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
GND	P1	P1	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O, PGCK1 <sup>(1)</sup> , GCK1 <sup>(2)</sup>	P2	P2	B1	C3	170
I/O	P3	P3	C2	C2	173
I/O	P4	P4	D2	B1	176
I/O	P5	P5	D3	C1	179
I/O, TDI	P6	P6	E4	D4	182
I/O, TCK	P7	P7	C1	D3	185
I/O	-	-	-	D2	188
I/O	-	-	-	D1	191
I/O	P8	P8	D1	E2	194
I/O	P9	P9	E3	E4	197
I/O	P10	P10	E2	E1	200
I/O	P11	P11	E1	F5	203
I/O	P12	P12	F3	F3	206
I/O	-	P13	F2	F2	209
GND	P13	P14	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P14	P15	G3	F4	212
I/O	P15	P16	G2	F1	215
I/O, TMS	P16	P17	G1	G3	218
I/O	P17	P18	H3	G2	221
VCC	P18	P19	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	-	P20	H2	G4	224
I/O	-	P21	H1	H1	227
I/O	-	-	J4	H3	230
I/O	-	-	J3	H2	233
I/O	P19	P23	J2	H4	236
I/O	P20	P24	J1	J1	239
I/O	P21	P25	K2	J2	242
I/O	P22	P26	K3	J3	245
I/O	P23	P27	K1	J4	248
I/O	P24	P28	L1	K1	251

### Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: Component Availability Chart for Spartan/XL FPGAs

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84 <sup>(3)</sup>	VQ100 <sup>(3)</sup>	CS144 <sup>(3)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(3)</sup>	CS280 <sup>(3)</sup>
XCS05	-3	C <sup>(3)</sup>	C, I	-	-	-	-	-	-
	-4	C <sup>(3)</sup>	C	-	-	-	-	-	-
XCS10	-3	C <sup>(3)</sup>	C, I	-	C	-	-	-	-
	-4	C <sup>(3)</sup>	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C <sup>(3)</sup>	-	C, I	C, I	C	C <sup>(3)</sup>	-
	-4	-	C <sup>(3)</sup>	-	C	C	C	C <sup>(3)</sup>	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C <sup>(3)</sup>	C, I	-	-	-	-	-	-
	-5	C <sup>(3)</sup>	C	-	-	-	-	-	-
XCS10XL	-4	C <sup>(3)</sup>	C, I	C <sup>(3)</sup>	C	-	-	-	-
	-5	C <sup>(3)</sup>	C	C <sup>(3)</sup>	C	-	-	-	-
XCS20XL	-4	-	C, I	C <sup>(3)</sup>	C, I	C, I	-	-	-
	-5	-	C	C <sup>(3)</sup>	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C <sup>(3)</sup>
	-5	-	C	-	C	C	C	C	C <sup>(3)</sup>
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C <sup>(3)</sup>
	-5	-	-	-	-	C	C	C	C <sup>(3)</sup>

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#### Notes:

1. C = Commercial  $T_J = 0^\circ$  to  $+85^\circ\text{C}$
2. I = Industrial  $T_J = -40^\circ\text{C}$  to  $+100^\circ\text{C}$
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

### Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

[www.xilinx.com/support/documentation/spartan-xl.htm#19687](http://www.xilinx.com/support/documentation/spartan-xl.htm#19687)

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

[www.xilinx.com/cgi-bin/thermal/thermal.pl](http://www.xilinx.com/cgi-bin/thermal/thermal.pl)

Table 20: User I/O Chart for Spartan/XL FPGAs

Device	Max I/O	Package Type							
		PC84 <sup>(1)</sup>	VQ100 <sup>(1)</sup>	CS144 <sup>(1)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(1)</sup>	CS280 <sup>(1)</sup>
XCS05	80	61 <sup>(1)</sup>	77	-	-	-	-	-	-
XCS10	112	61 <sup>(1)</sup>	77	-	112	-	-	-	-
XCS20	160	-	77	-	113	160	-	-	-
XCS30	192	-	77 <sup>(1)</sup>	-	113	169	192	192 <sup>(1)</sup>	-
XCS40	224	-	-	-	-	169	192	205	-
XCS05XL	80	61 <sup>(1)</sup>	77 <sup>(2)</sup>	-	-	-	-	-	-
XCS10XL	112	61 <sup>(1)</sup>	77 <sup>(2)</sup>	112 <sup>(1)</sup>	112 <sup>(2)</sup>	-	-	-	-
XCS20XL	160	-	77 <sup>(2)</sup>	113 <sup>(1)</sup>	113 <sup>(2)</sup>	160 <sup>(2)</sup>	-	-	-
XCS30XL	192	-	77 <sup>(2)</sup>	-	113 <sup>(2)</sup>	169 <sup>(2)</sup>	192 <sup>(2)</sup>	192 <sup>(2)</sup>	192 <sup>(1)</sup>
XCS40XL	224	-	-	-	-	169 <sup>(2)</sup>	192 <sup>(2)</sup>	205 <sup>(2)</sup>	224 <sup>(1)</sup>

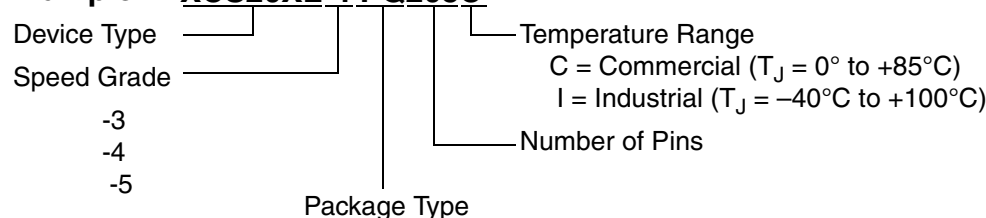
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**Notes:**

1. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
2. These Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

## Ordering Information

**Example: XCS20XL-4 PQ208C**



BG = Ball Grid Array

BGG = Ball Grid Array (Pb-free)

PC = Plastic Lead Chip Carrier

PQ = Plastic Quad Flat Pack

PQG = Plastic Quad Flat Pack (Pb-free)

VQ = Very Thin Quad Flat Pack

VQG = Very Thin Quad Flat Pack (Pb-free)

TQ = Thin Quad Flat Pack

TQG = Thin Quad Flat Pack (Pb-free)

CS = Chip Scale