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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	950
Total RAM Bits	12800
Number of I/O	113
Number of Gates	20000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs20xl-4tqg144c

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in [Figure 5](#) on the CK line.

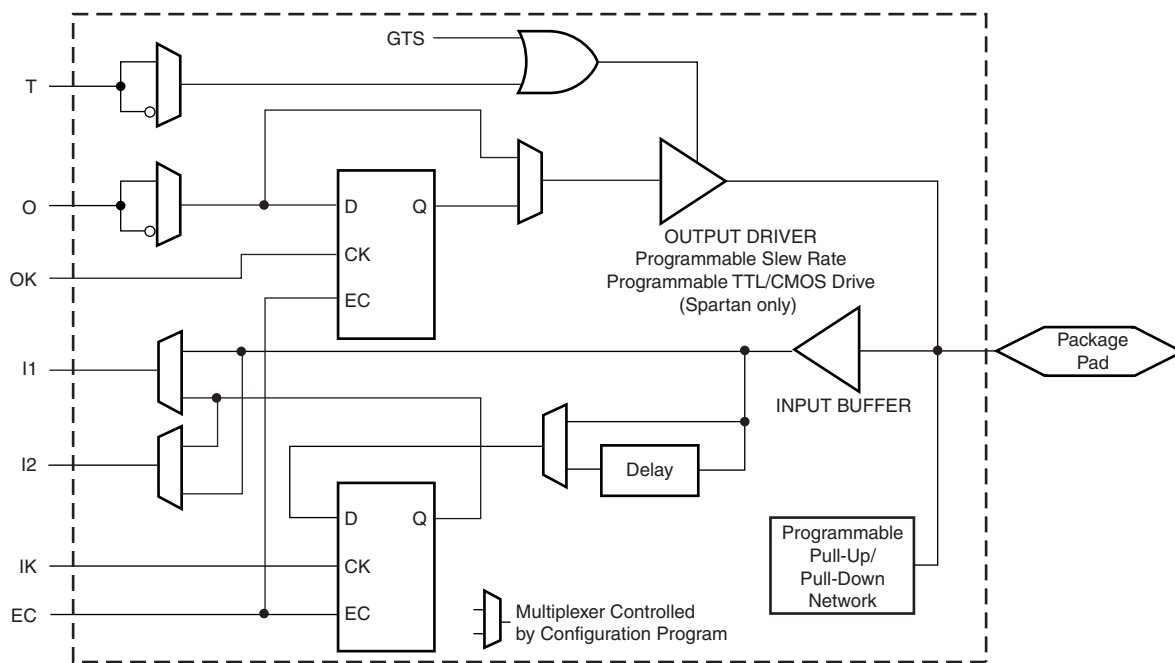
The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See [Global Nets and Buffers](#), page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop. The output of the input register goes to the routing channels (via I1 and I2 in [Figure 6](#)). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds,

using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

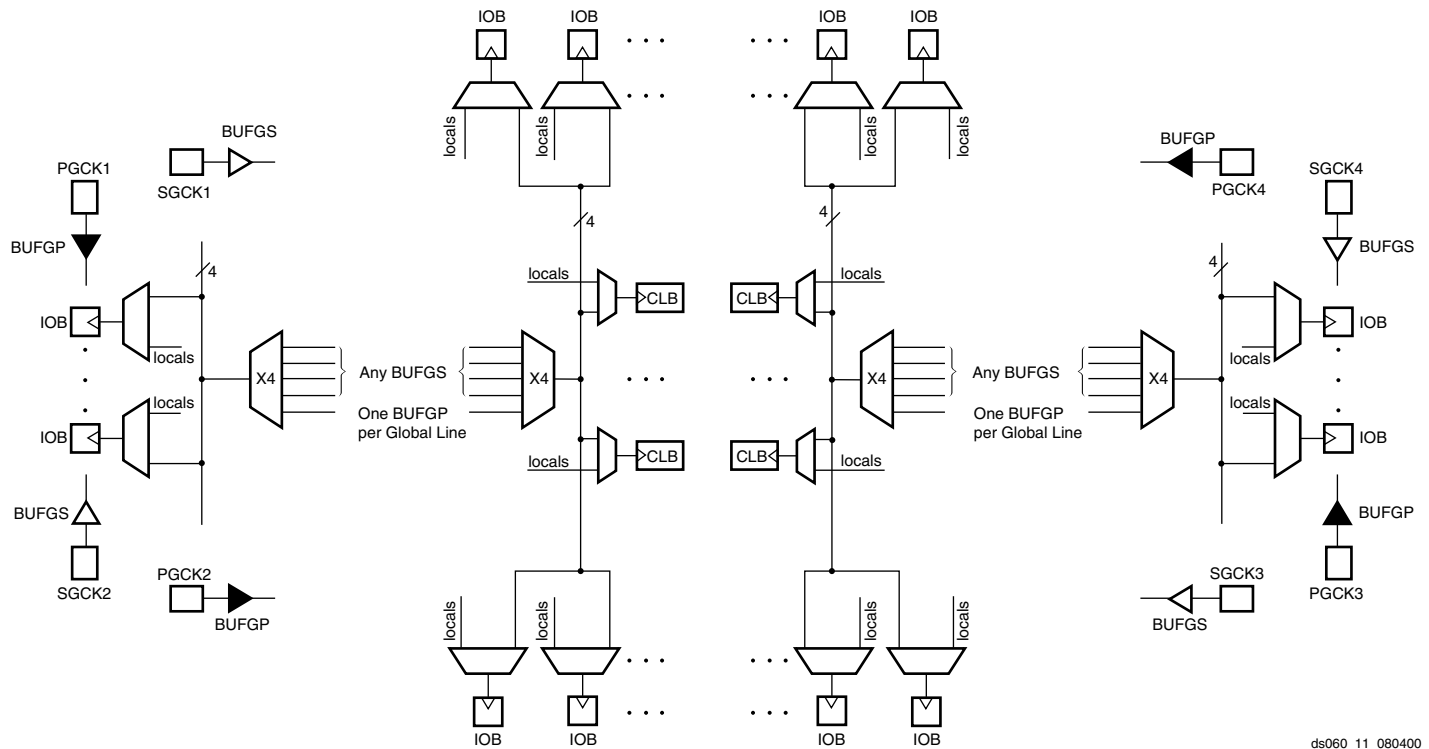
Supported sources for Spartan/XL device inputs are shown in [Table 4](#).

Spartan-XL family I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in [Table 4](#). In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.



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Figure 6: Simplified Spartan/XL IOB Block Diagram



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Figure 11: 5V Spartan Family Global Net Distribution

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 8. Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 8: CLB Memory Configurations

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√	—	—

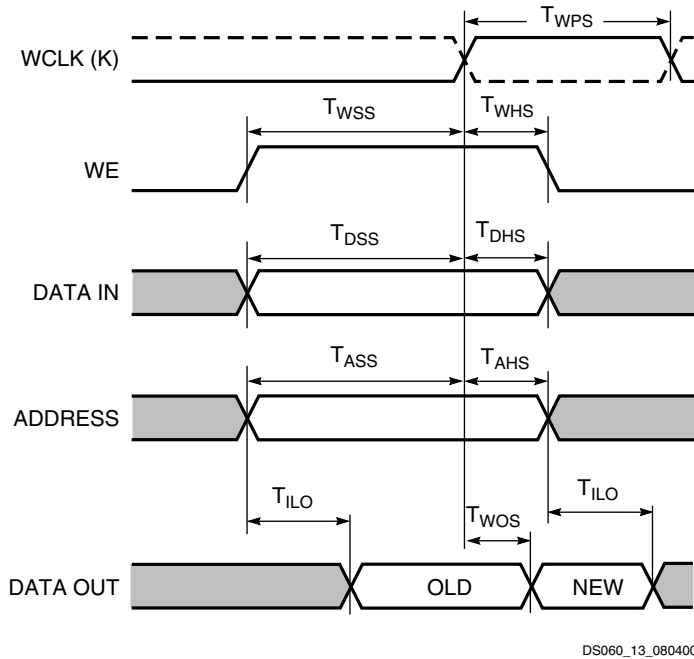


Figure 13: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be

inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO} , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS} , the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by $A[3:0]$ while the second provides only for read operations at the address specified independently by $DPRA[3:0]$. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the

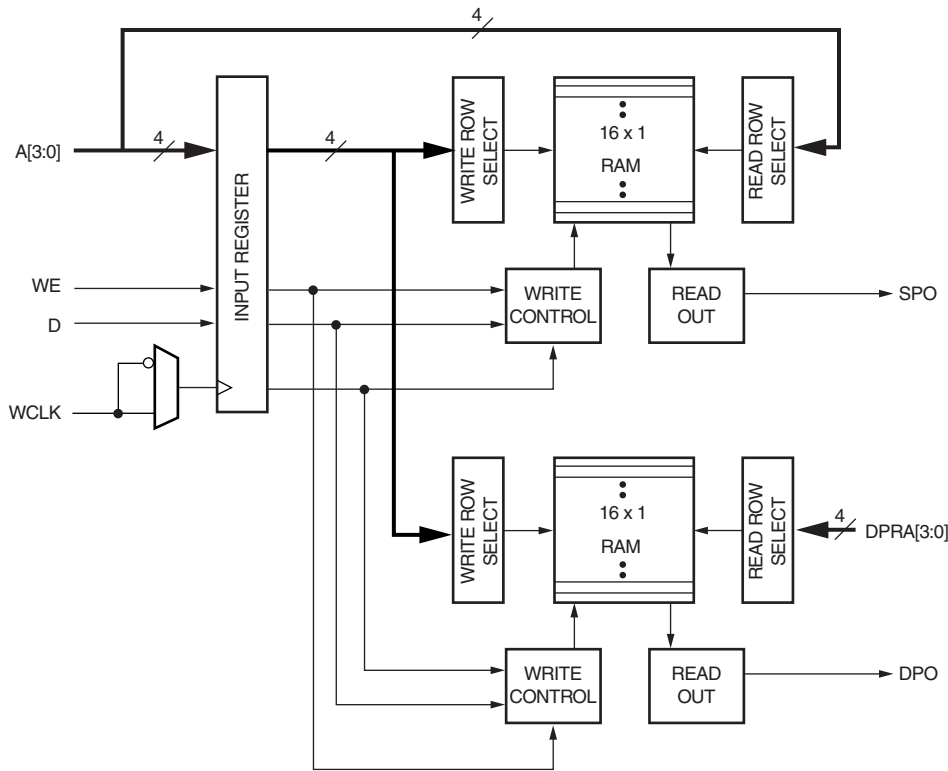


Figure 14: Logic Diagram for the Dual-Port RAM

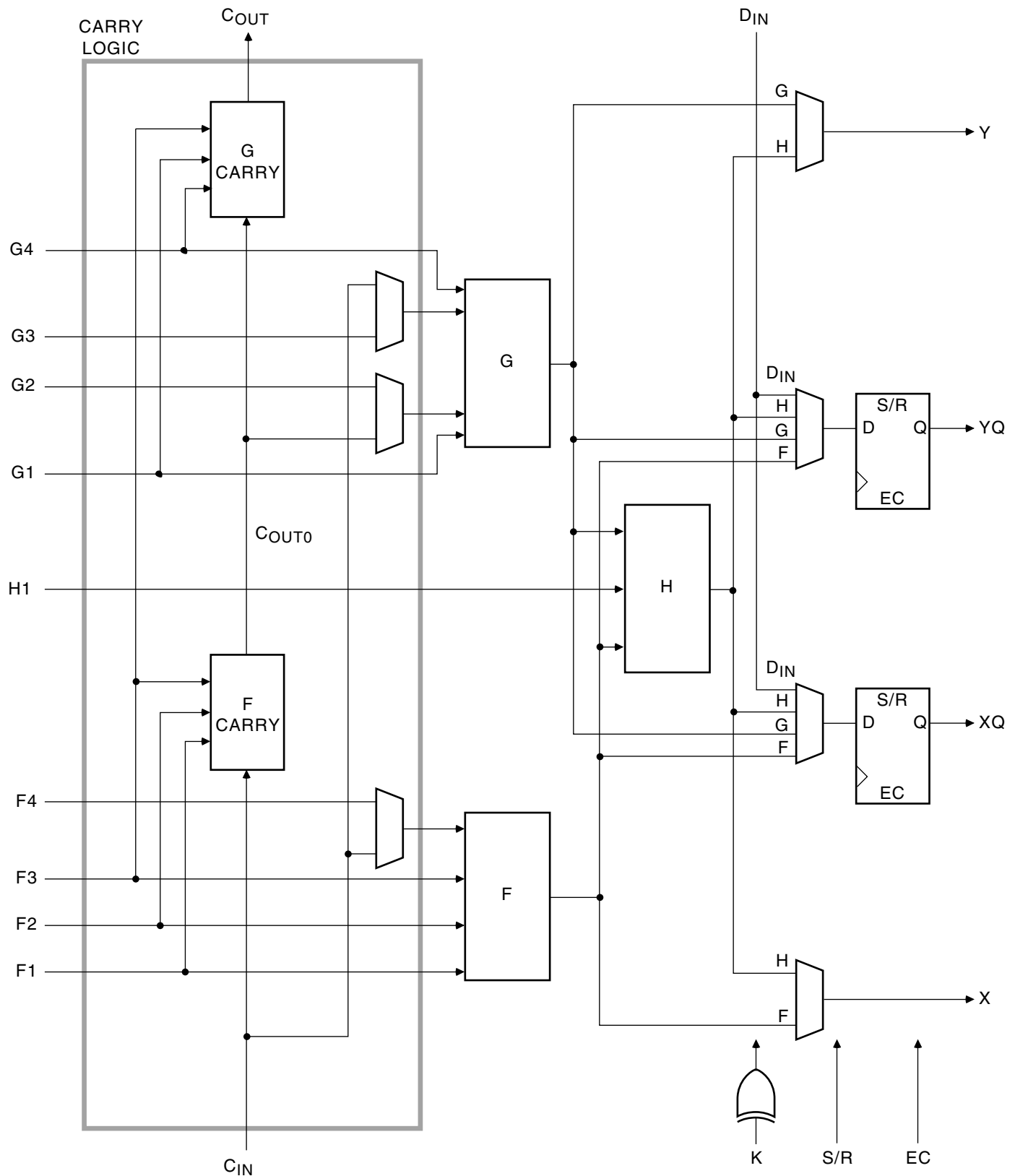
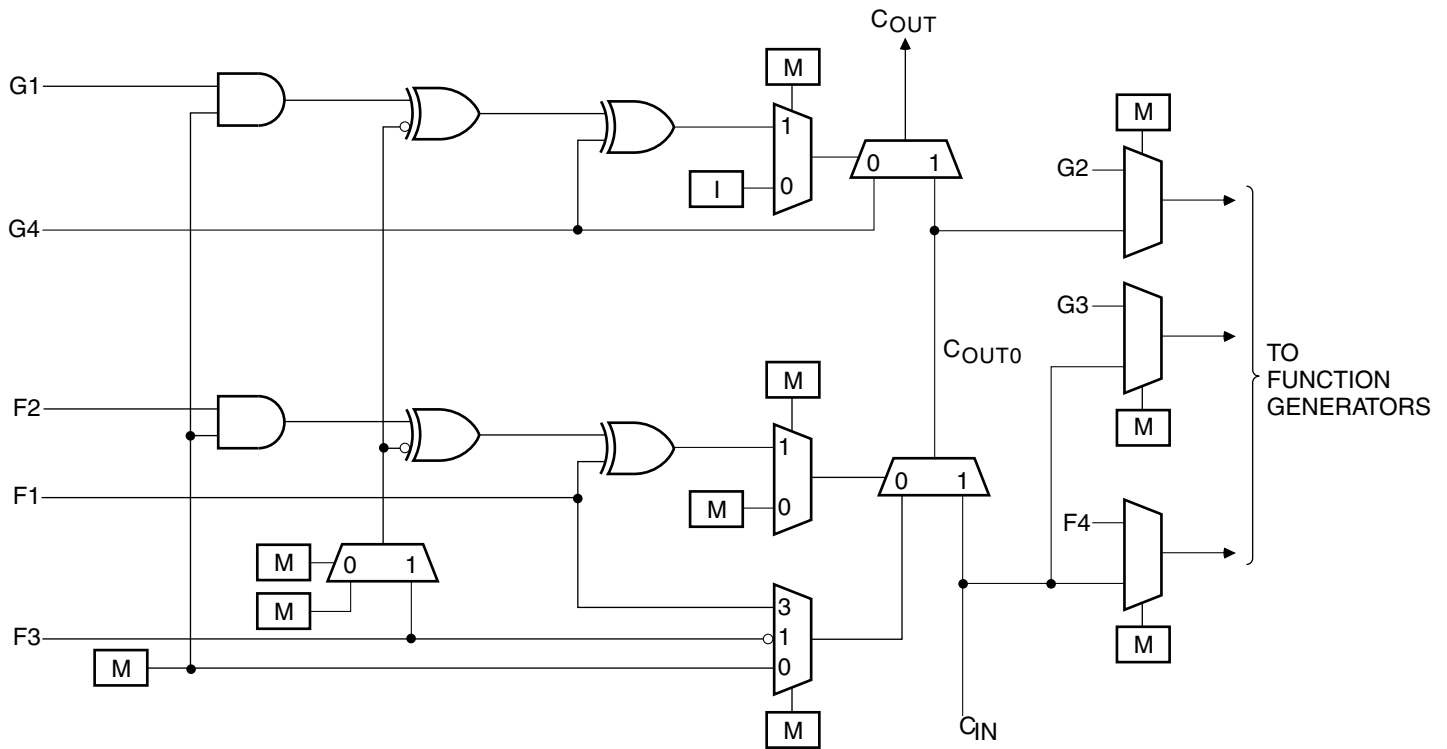


Figure 16: Fast Carry Logic in Spartan/XL CLB

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Figure 17: Detail of Spartan/XL Dedicated Carry Logic

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

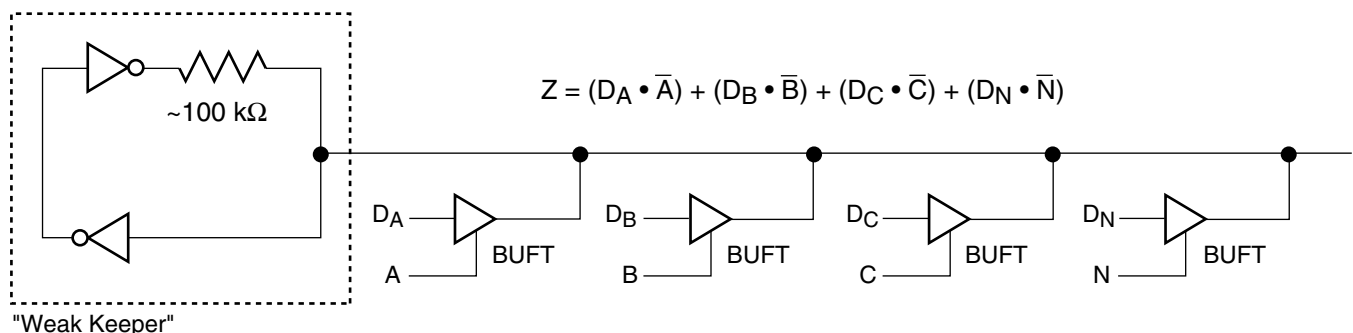
Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

Table 11: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN



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Figure 18: 3-state Buffers Implement a Multiplexer

Table 12: Boundary Scan Instructions

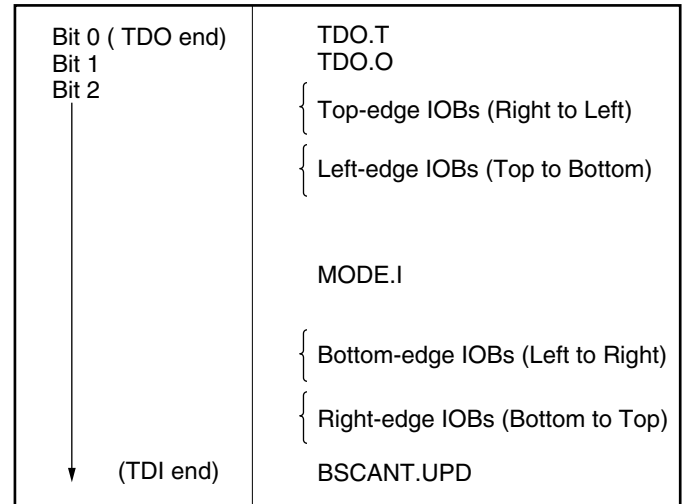
Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	IDCODE (Spartan-XL only)	IDCODE Register	-
1	1	1	BYPASS	Bypass Register	-

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-state. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contribute all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 21. The device-specific pinout tables for the Spartan/XL devices include the boundary scan locations for each IOB pin.



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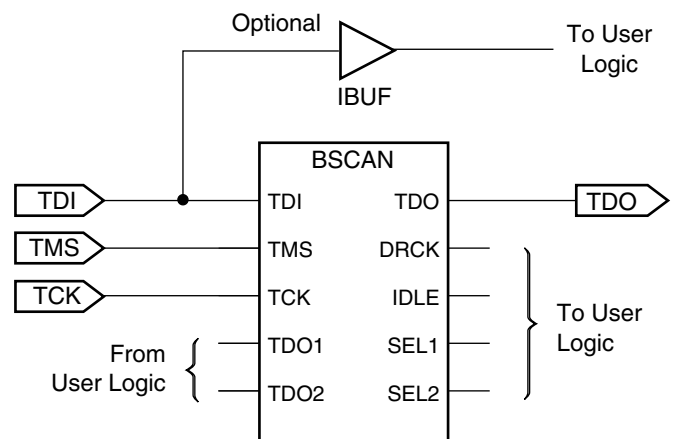
Figure 21: Boundary Scan Bit Sequence

BSDL (Boundary Scan Description Language) files for Spartan/XL devices are available on the Xilinx website in the File Download area. Note that the 5V Spartan devices and 3V Spartan-XL devices have different BSDL files.

Including Boundary Scan in a Design

If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 22.



DS060_22_080400

Figure 22: Boundary Scan Example

Even if the boundary scan symbol is used in a design, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state.
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "Boundary Scan in FPGA Devices."

Boundary Scan Enhancements (Spartan-XL Family Only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

IDCODE: The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

c = the company code (49h for Xilinx)

a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)

f = the family code (02h for Spartan-XL family)

v = the die version number

Table 13: IDCODEs Assigned to Spartan-XL FPGAs

FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

Configuration State: The configuration state is available to JTAG controllers.

Configuration Disable: The JTAG port can be prevented from configuring the FPGA.

TCK Startup: TCK can now be used to clock the start-up block in addition to other user clocks.

CCLK Holdoff: Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

Reissue Configure: The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

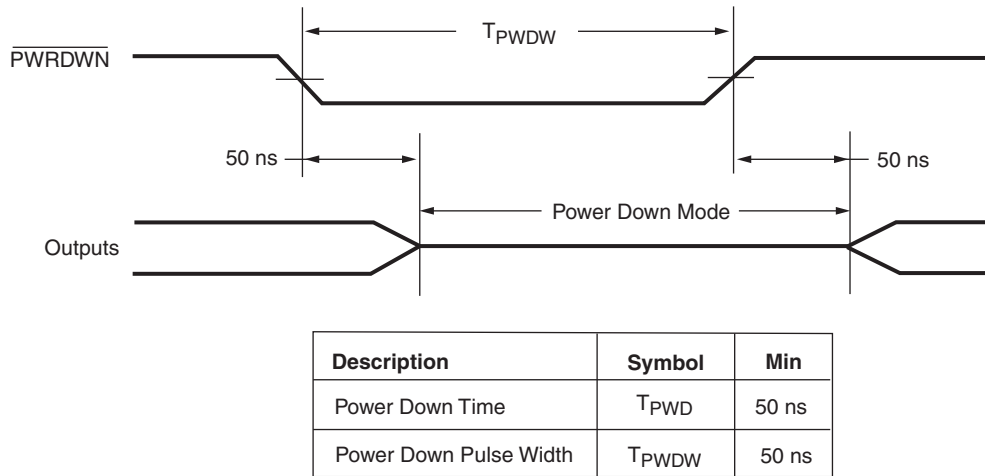
Bypass FF: Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

Power-Down (Spartan-XL Family Only)

All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low power-down pin (PWRDWN) to reduce supply current to 100 μ A typical. The PWRDWN pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The PWRDWN pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

V_{CC} must continue to be supplied during Power-down, and configuration data is maintained. When the PWRDWN pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The PROGRAM pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

PWRDWN has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before PWRDWN to affect the order of events. When the PWRDWN signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of PWRDWN before using the device.



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Figure 23: **PWRDWN Pulse Timing**

Power-down retains the configuration, but loses all data stored in the device flip-flops. All inputs are interpreted as Low, but the internal combinatorial logic is fully functional. Make sure that the combination of all inputs Low and all flip-flops set or reset in your design will not generate internal oscillations, or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line.

During configuration, the \overline{PWRDWN} pin must be High. If the Power Down state is entered before or during configuration, the device will restart configuration once the \overline{PWRDWN} signal is removed. Note that the configuration pins are affected by Power Down and may not reflect their normal function. If there is an external pull-up resistor on the DONE pin, it will be High during Power Down even if the device is not yet configured. Similarly, if \overline{PWRDWN} is asserted before configuration is completed, the \overline{INIT} pin will not indicate status information.

Note that the \overline{PWRDWN} pin is not part of the Boundary Scan chain. Therefore, the Spartan-XL family has a separate set of BSDL files than the 5V Spartan family. Boundary scan logic is not usable during Power Down.

Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan/XL devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell

that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Configuration Mode Control

5V Spartan devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

3V Spartan-XL devices have three configuration modes.

- M1/M0 = 11 sets Slave Serial mode
- M1/M0 = 10 sets Master Serial mode
- M1/M0 = 0X sets Express mode

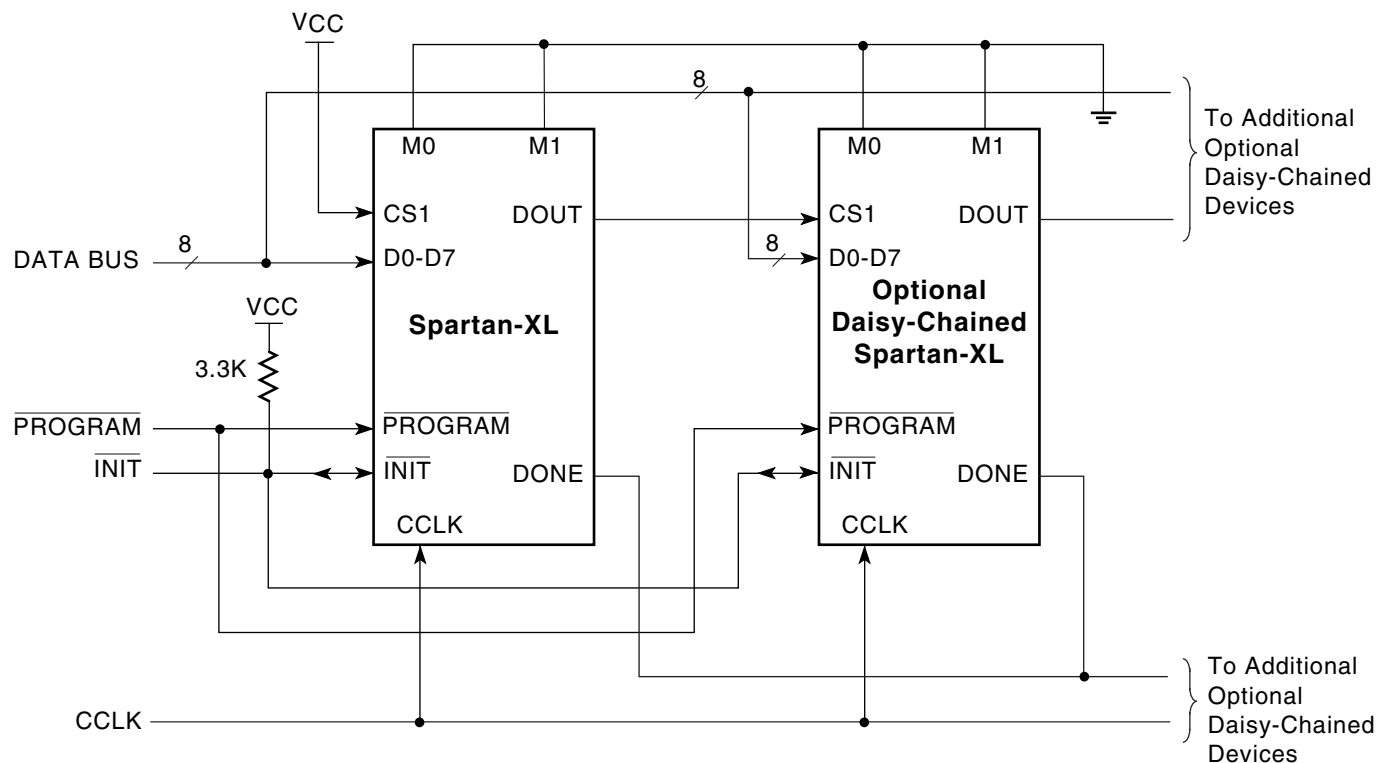
In addition to these modes, the device can be configured through the Boundary Scan logic (See "Configuration Through the Boundary Scan Pins" on page 37.).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pins are unused. The Mode pins have a weak pull-up resistor turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the MODE/M0 pin should be connected directly to GND, or through a pull-down resistor of 1 K Ω or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during con-

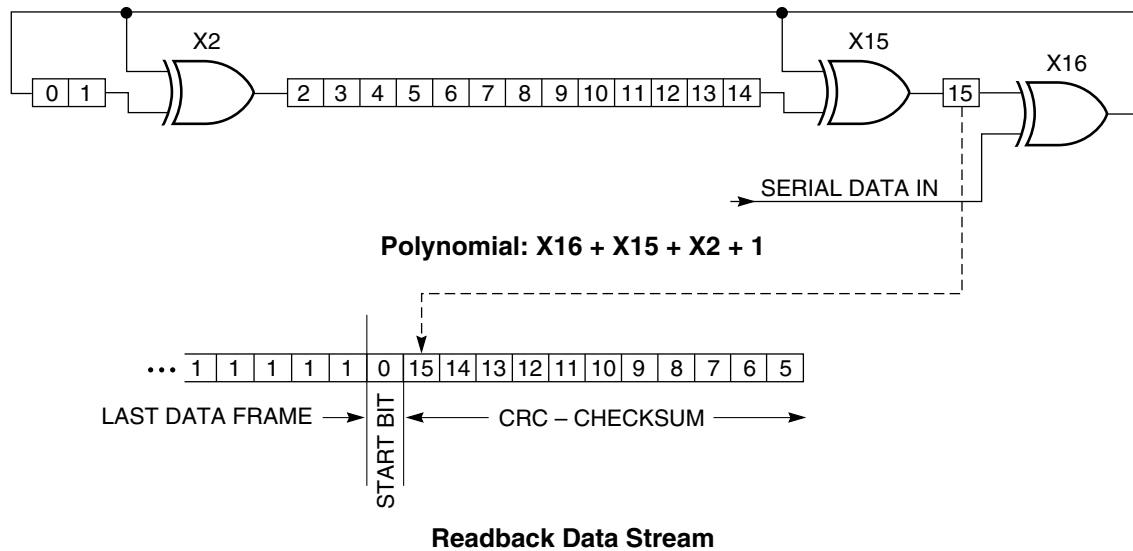
to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device

in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.



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Figure 27: Express Mode Circuit Diagram



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Figure 29: Circuit for Generating CRC-16

Configuration Sequence

There are four major steps in the Spartan/XL FPGA power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC} . When all \overline{INIT} pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin

Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the \overline{INIT} input.

Initialization

During initialization and configuration, user pins \overline{HDC} , \overline{LDC} , \overline{INIT} and \overline{DONE} provide status outputs for the system interface. The outputs \overline{LDC} , \overline{INIT} and \overline{DONE} are held Low and \overline{HDC} is held High starting at the initial application of power.

The open drain \overline{INIT} pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive \overline{INIT} . Two internal clocks after the \overline{INIT} pin is recognized as High, the device samples the \overline{MODE} pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in [Figure 32](#).

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low)

of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

Readback Capture

When the Readback Capture option is selected, the data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.

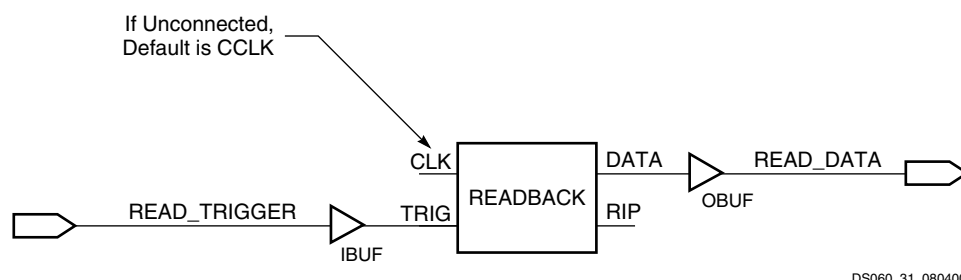


Figure 32: Readback Example

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be

met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

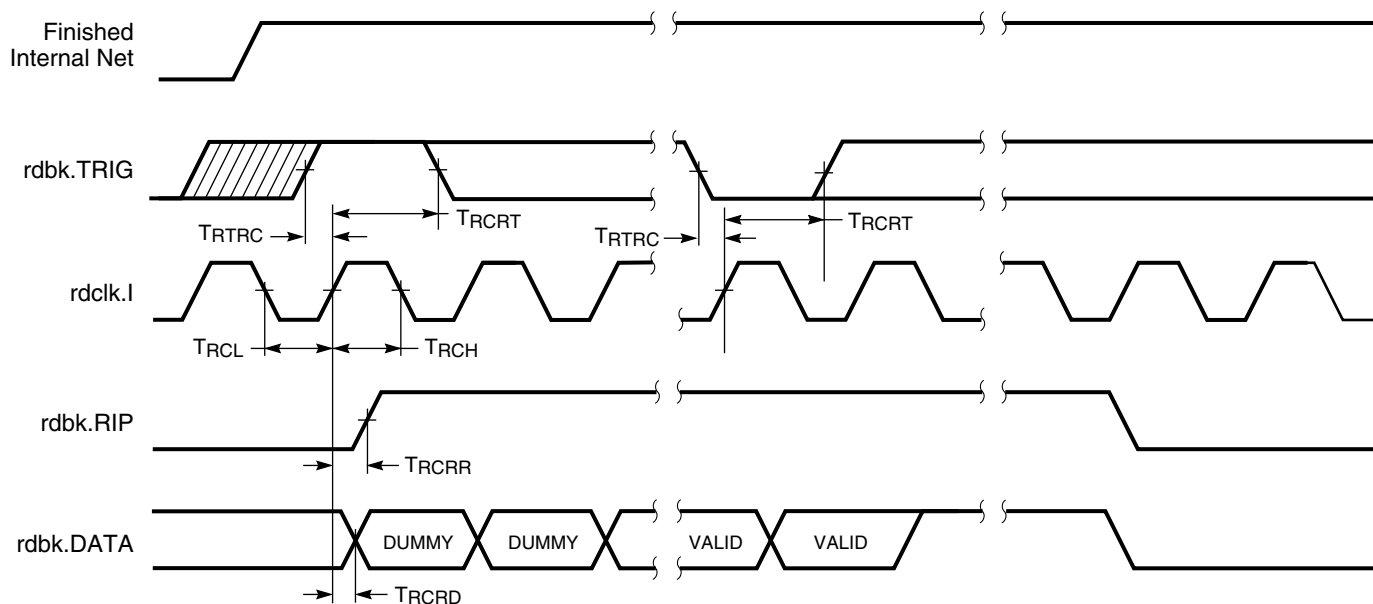
The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in [Table 16](#) and [Table 17](#).

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.



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Figure 33: Spartan and Spartan-XL Readback Timing Diagram

Spartan and Spartan-XL Readback Switching Characteristics

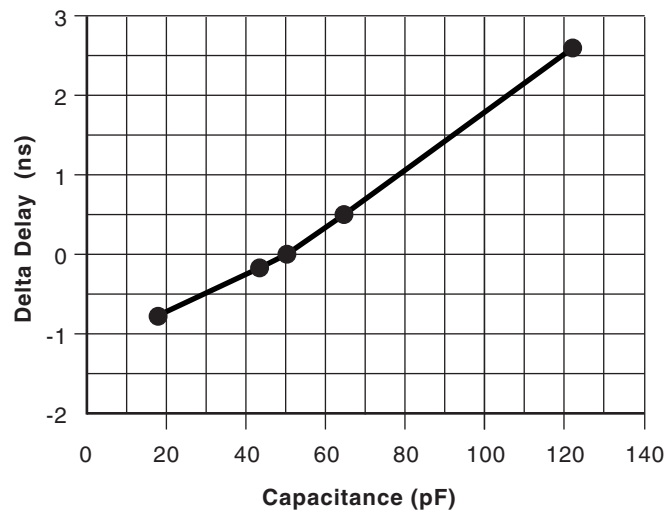
Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:

1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



DS060_35_080400

Figure 34: Delay Factor at Various Capacitive Loads

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size ⁽¹⁾	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Write Operation							
T _{WCS}	Address write cycle time (clock K period)	16x2	7.7	-	8.4	-	ns
T _{WCTS}		32x1	7.7	-	8.4	-	ns
T _{WPS}	Clock K pulse width (active edge)	16x2	3.1	-	3.6	-	ns
T _{WPTS}		32x1	3.1	-	3.6	-	ns
T _{ASS}	Address setup time before clock K	16x2	1.3	-	1.5	-	ns
T _{ASTS}		32x1	1.5	-	1.7	-	ns
T _{DSS}	DIN setup time before clock K	16x2	1.5	-	1.7	-	ns
T _{DSTS}		32x1	1.8	-	2.1	-	ns
T _{WSS}	WE setup time before clock K	16x2	1.4	-	1.6	-	ns
T _{WSTS}		32x1	1.3	-	1.5	-	ns
	All hold times after clock K	16x2	0.0	-	0.0	-	ns
T _{WOS}	Data valid after clock K	32x1	-	4.5	-	5.3	ns
T _{WOTS}		16x2	-	5.4	-	6.3	ns
Read Operation							
T _{RC}	Address read cycle time	16x2	2.6	-	3.1	-	ns
T _{RCT}		32x1	3.8	-	5.5	-	ns
T _{ILO}	Data Valid after address change (no Write Enable)	16x2	-	1.0	-	1.1	ns
T _{IHO}		32x1	-	1.7	-	2.0	ns
T _{ICK}	Address setup time before clock K	16x2	0.6	-	0.7	-	ns
T _{IHCK}		32x1	1.3	-	1.6	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan-XL Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case oper-

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Global Clock to Output using OFF					
T _{ICKOF}	Fast	XCS05XL	4.6	5.2	ns
		XCS10XL	4.9	5.5	ns
		XCS20XL	5.2	5.8	ns
		XCS30XL	5.5	6.2	ns
		XCS40XL	5.8	6.5	ns
Slew Rate Adjustment					
T _{SLOW}	For Output SLOW option add	All Devices	1.5	1.7	ns

Notes:

1. Output delays are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.
3. OFF = Output Flip Flop

Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to

the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Propagation Delays							
T _{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.2	-	3.7	ns
T _{OPF}	Output (O) to Pad, fast	All devices	-	2.5	-	2.9	ns
T _{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	2.8	-	3.3	ns
T _{TSONF}	3-state to Pad active and valid, fast	All devices	-	2.6	-	3.0	ns
T _{OFFPF}	Output (O) to Pad via Output MUX, fast	All devices	-	3.7	-	4.4	ns
T _{OKFPF}	Select (OK) to Pad via Output MUX, fast	All devices	-	3.3	-	3.9	ns
T _{SLOW}	For Output SLOW option add	All devices	-	1.5	-	1.7	ns
Setup and Hold Times							
T _{OOK}	Output (O) to clock (OK) setup time	All devices	0.5	-	0.5	-	ns
T _{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T _{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	0.0	-	0.0	-	ns
T _{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.1	-	0.2	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T _{RPO}	Delay from GSR input to any Pad	XCS05XL	-	11.9	-	14.0	ns
		XCS10XL	-	12.4	-	14.5	ns
		XCS20XL	-	12.9	-	15.0	ns
		XCS30XL	-	13.9	-	16.0	ns
		XCS40XL	-	14.9	-	17.0	ns

Notes:

- Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
- Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
$\overline{\text{PWRDWN}}$	I	I	$\overline{\text{PWRDWN}}$ is an active Low input that forces the FPGA into the Power Down state and reduces power consumption. When $\overline{\text{PWRDWN}}$ is Low, the FPGA disables all I/O and initializes all flip-flops. All inputs are interpreted as Low independent of their actual level. VCC must be maintained, and the configuration data is maintained. $\overline{\text{PWRDWN}}$ halts configuration if asserted before or during configuration, and re-starts configuration when removed. When $\overline{\text{PWRDWN}}$ returns High, the FPGA becomes operational by first enabling the inputs and flip-flops and then enabling the outputs. $\overline{\text{PWRDWN}}$ has a default internal pull-up resistor.
User I/O Pins That Can Have Special Functions			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 k Ω to 10 k Ω external pull-up resistor is recommended. As an active Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 μs after INIT has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGRP symbol is automatically placed on one of these pins.

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	P85	P97	U12	T11	382 ⁽³⁾
I/O	-	-	-	P99	V13	U12	385 ⁽³⁾
I/O	-	-	-	P100	Y14	T12	388 ⁽³⁾
VCC	-	-	P86	P101	VCC ⁽⁴⁾	W13	-
I/O	P43	P60	P87	P102	Y15	V13	391 ⁽³⁾
I/O	P44	P61	P88	P103	V14	U13	394 ⁽³⁾
I/O	-	P62	P89	P104	W15	T13	397 ⁽³⁾
I/O	-	P63	P90	P105	Y16	W14	400 ⁽³⁾
GND	-	P64	P91	P106	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P107	V15	V14	403 ⁽³⁾
I/O	-	-	P92	P108	W16	U14	406 ⁽³⁾
I/O	-	-	P93	P109	Y17	T14	409 ⁽³⁾
I/O	-	-	P94	P110	V16	R14	412 ⁽³⁾
I/O	-	-	P95	P111	W17	W15	415 ⁽³⁾
I/O	-	-	P96	P112	Y18	U15	418 ⁽³⁾
I/O	P45	P65	P97	P113	U16	V16	421 ⁽³⁾
I/O	P46	P66	P98	P114	V17	U16	424 ⁽³⁾
I/O	-	P67	P99	P115	W18	W17	427 ⁽³⁾
I/O	-	P68	P100	P116	Y19	W18	430 ⁽³⁾
I/O	P47	P69	P101	P117	V18	V17	433 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P48	P70	P102	P118	W19	V18	436 ⁽³⁾
GND	P49	P71	P103	P119	GND ⁽⁴⁾	GND ⁽⁴⁾	-
DONE	P50	P72	P104	P120	Y20	W19	-
VCC	P51	P73	P105	P121	VCC ⁽⁴⁾	U17	-
PROGRAM	P52	P74	P106	P122	V19	U18	-
I/O (D7 ⁽²⁾)	P53	P75	P107	P123	U19	V19	439 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P54	P76	P108	P124	U18	U19	442 ⁽³⁾
I/O	-	P77	P109	P125	T17	T16	445 ⁽³⁾
I/O	-	P78	P110	P126	V20	T17	448 ⁽³⁾
I/O	-	-	-	P127	U20	T18	451 ⁽³⁾
I/O	-	-	P111	P128	T18	T19	454 ⁽³⁾
I/O (D6 ⁽²⁾)	P55	P79	P112	P129	T19	R16	457 ⁽³⁾
I/O	P56	P80	P113	P130	T20	R19	460 ⁽³⁾
I/O	-	-	P114	P131	R18	P15	463 ⁽³⁾
I/O	-	-	P115	P132	R19	P17	466 ⁽³⁾
I/O	-	-	P116	P133	R20	P18	469 ⁽³⁾
I/O	-	-	P117	P134	P18	P16	472 ⁽³⁾
GND	-	P81	P118	P135	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P136	P20	P19	475 ⁽³⁾
I/O	-	-	-	P137	N18	N17	478 ⁽³⁾
I/O	-	P82	P119	P138	N19	N18	481 ⁽³⁾
I/O	-	P83	P120	P139	N20	N19	484 ⁽³⁾
VCC	-	-	P121	P140	VCC ⁽⁴⁾	N16	-
I/O (D5 ⁽²⁾)	P57	P84	P122	P141	M17	M19	487 ⁽³⁾
I/O	P58	P85	P123	P142	M18	M17	490 ⁽³⁾

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	P124	P144	M20	L19	493 ⁽³⁾
I/O	-	-	P125	P145	L19	L18	496 ⁽³⁾
I/O	P59	P86	P126	P146	L18	L17	499 ⁽³⁾
I/O	P60	P87	P127	P147	L20	L16	502 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	P88	P128	P148	K20	K19	505 ⁽³⁾
I/O	P62	P89	P129	P149	K19	K18	508 ⁽³⁾
VCC	P63	P90	P130	P150	VCC ⁽⁴⁾	K17	-
GND	P64	P91	P131	P151	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O (D3 ⁽²⁾)	P65	P92	P132	P152	K18	K16	511 ⁽³⁾
I/O	P66	P93	P133	P153	K17	K15	514 ⁽³⁾
I/O	P67	P94	P134	P154	J20	J19	517 ⁽³⁾
I/O	-	P95	P135	P155	J19	J18	520 ⁽³⁾
I/O	-	-	P136	P156	J18	J17	523 ⁽³⁾
I/O	-	-	P137	P157	J17	J16	526 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	P96	P138	P159	H19	H17	529 ⁽³⁾
I/O	P69	P97	P139	P160	H18	H16	532 ⁽³⁾
VCC	-	-	P140	P161	VCC ⁽⁴⁾	G19	-
I/O	-	P98	P141	P162	G19	G18	535 ⁽³⁾
I/O	-	P99	P142	P163	F20	G17	538 ⁽³⁾
I/O	-	-	-	P164	G18	G16	541 ⁽³⁾
I/O	-	-	-	P165	F19	F19	544 ⁽³⁾
GND	-	P100	P143	P166	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P167	F18	F18	547 ⁽³⁾
I/O	-	-	P144	P168	E19	F17	550 ⁽³⁾
I/O	-	-	P145	P169	D20	F16	553 ⁽³⁾
I/O	-	-	P146	P170	E18	F15	556 ⁽³⁾
I/O	-	-	P147	P171	D19	E19	559 ⁽³⁾
I/O	-	-	P148	P172	C20	E17	562 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	P101	P149	P173	E17	E16	565 ⁽³⁾
I/O	P71	P102	P150	P174	D18	D19	568 ⁽³⁾
I/O	-	P103	P151	P175	C19	C19	571 ⁽³⁾
I/O	-	P104	P152	P176	B20	B19	574 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	P105	P153	P177	C18	C18	577 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	P106	P154	P178	B19	B18	580 ⁽³⁾
CCLK	P74	P107	P155	P179	A20	A19	-
VCC	P75	P108	P156	P180	VCC ⁽⁴⁾	C17	-
O, TDO	P76	P109	P157	P181	A19	B17	0
GND	P77	P110	P158	P182	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P78	P111	P159	P183	B18	A18	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	P112	P160	P184	B17	A17	5
I/O	-	P113	P161	P185	C17	D16	8
I/O	-	P114	P162	P186	D16	C16	11
I/O (CS1) ⁽²⁾	P80	P115	P163	P187	A18	B16	14
I/O	P81	P116	P164	P188	A17	A16	17
I/O	-	-	P165	P189	C16	D15	20