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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	950
Total RAM Bits	12800
Number of I/O	113
Number of Gates	20000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs20xl-4tqg144i

Spartan and Spartan-XL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In addition to the conventional benefit of high volume programmable logic solutions, Spartan series FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan/XL families leverage the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA process developments.

Logic Functional Description

The Spartan series uses a standard FPGA structure as shown in Figure 1, page 2. The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.

- IOBs provide the interface between the package pins and internal signal lines.

- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in Figure 2. There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the **Advanced Features Description**, page 13.

Function Generators

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.
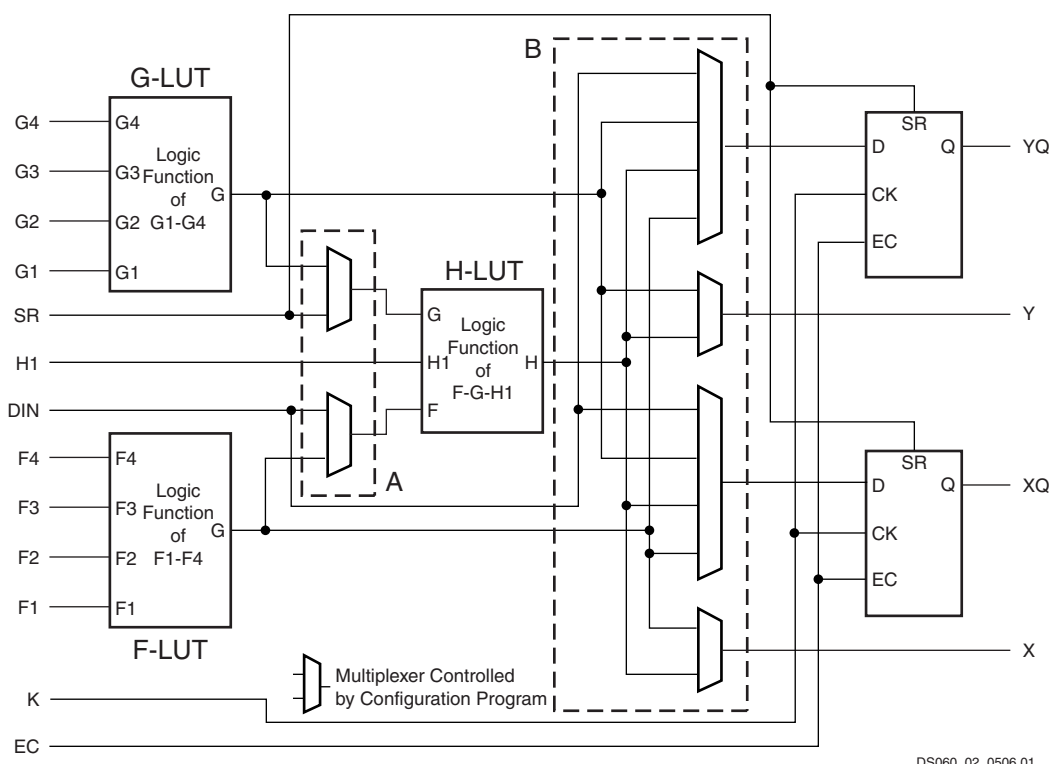
Figure 2: **Spartan/XL Simplified CLB Logic Diagram (some features not shown)**

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

  Note: When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.

Latches (Spartan-XL Family Only)

The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.
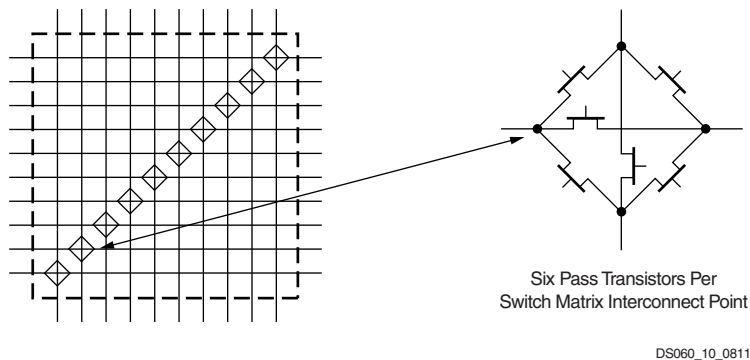
DS060_10_081100

Figure 10: **Programmable Switch Matrix**

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 8).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 8. The longlines also interface to some 3-state buffers which is described later in **3-State Long Line Drivers**, page 19.

I/O Routing

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four long-lines.

Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 11. In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.
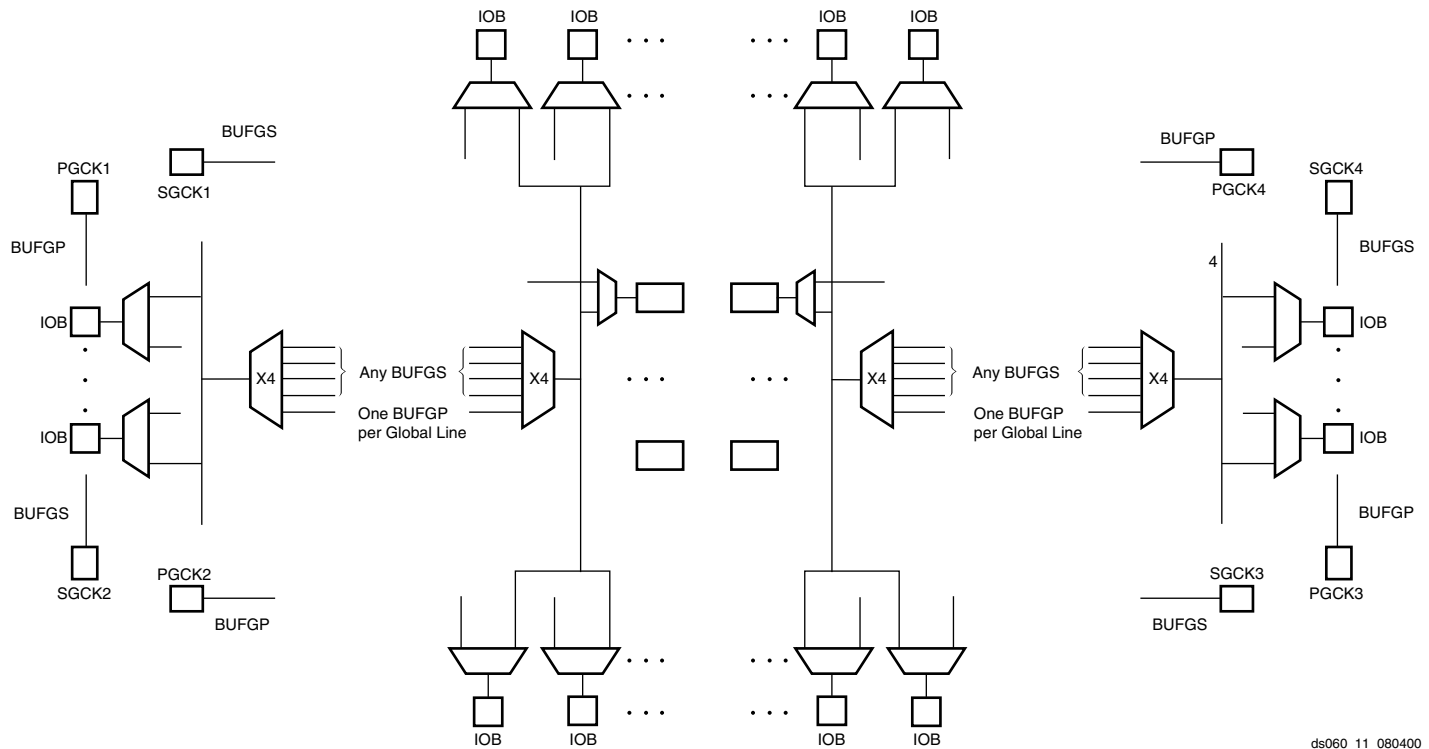
Figure 11: **5V Spartan Family Global Net Distribution**

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 8. Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 16: **Spartan/XL Data Stream Formats**

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0][1]
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	11111110b[2]
Data Frame	DATA[n–1:0]	DATA[n–1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes[3]	FFh	FFFFFFFFFFFFFFh

Legend:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Notes:
1. Not used by configuration logic.
2. 11111111b for XCS40XL only.
3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the $\overline{INIT}$ pin. In Master serial mode, CCLK continues to operate externally. The user must detect $\overline{INIT}$ and initialize a new configuration by pulsing the $\overline{PROGRAM}$ pin Low or cycling V_{CC}.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{INIT}$ pin Low and goes into a Wait state.
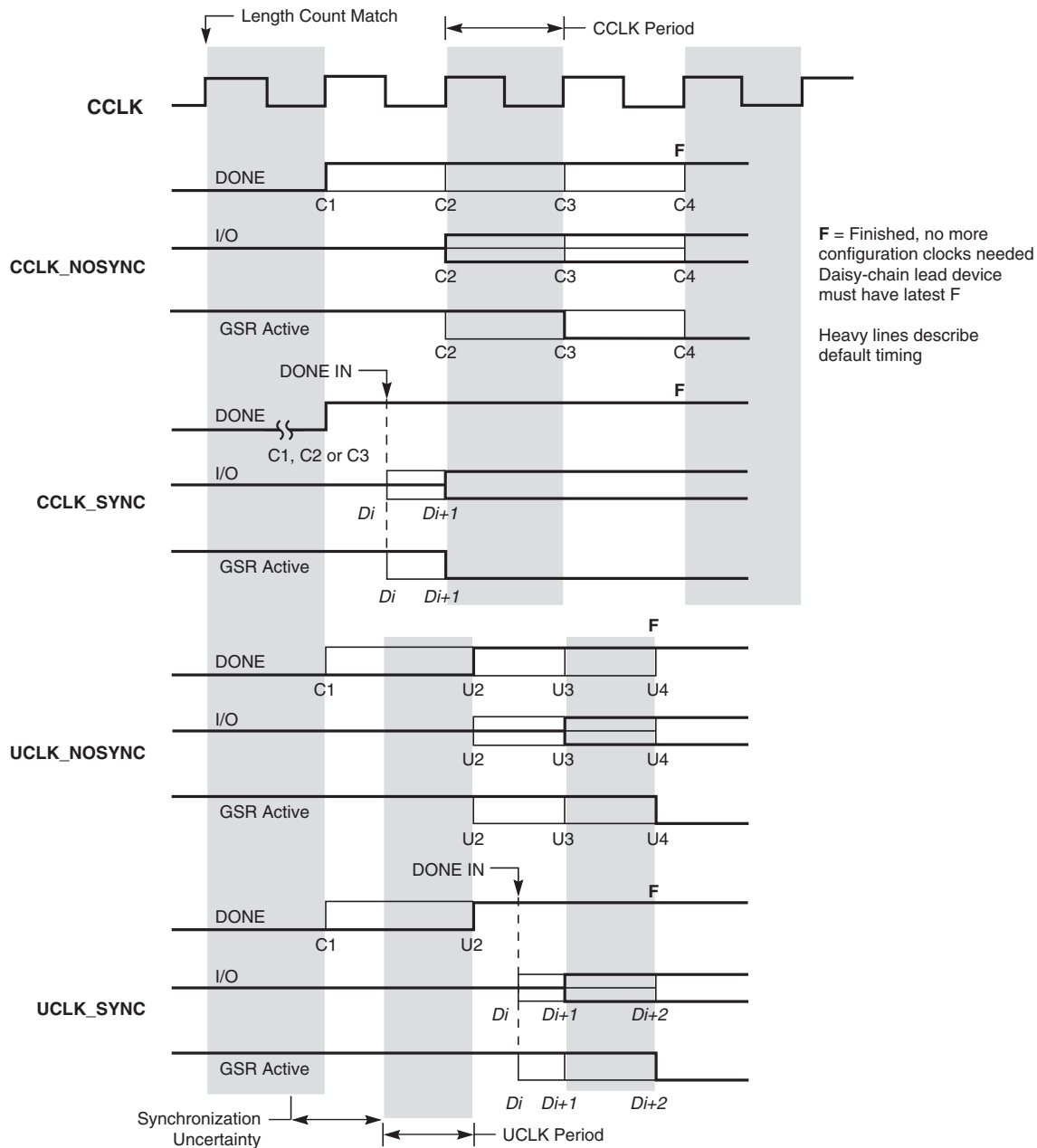
Figure 31: **Start-up Timing**

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with INIT held Low (or drive the PROGRAM pin Low for more than 300 ns followed by a High while holding INIT Low). Holding INIT Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold INIT Low.

- Issue the CONFIG command to the TMS input.

- Wait for INIT to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices.*" This application note applies to Spartan and Spartan-XL devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 32.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low)

of the first frame. The first two data bits of the first frame are always High.

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 16 and Table 17.

Spartan Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan Family Absolute Maximum Ratings[1]

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		−0.5 to +7.0	V
V_{IN}	Input voltage relative to GND[2,3]		−0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output[2,3]		−0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		−65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot (above V_{CC}) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to −2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = −40°C to +100°C[1]	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage[2]	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage[2]	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Spartan Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage @ I_{OH} = –1.0 mA, V_{CC} min	CMOS outputs	V_{CC} – 0.5	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min[1]	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		3.0	-	V
I_{CCO}	Quiescent FPGA supply current[2]	Commercial	-	3.0	mA
		Industrial	-	6.0	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)		-	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 5V (sample tested)		0.02	-	mA

Notes:
1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a Tie option.

Spartan Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

			Speed Grade		
			-4	-3	
Symbol	Description	Device	Max	Max	Units
T_{PG}	From pad through Primary buffer, to any clock K	XCS05	2.0	4.0	ns
		XCS10	2.4	4.3	ns
		XCS20	2.8	5.4	ns
		XCS30	3.2	5.8	ns
		XCS40	3.5	6.4	ns
T_{SG}	From pad through Secondary buffer, to any clock K	XCS05	2.5	4.4	ns
		XCS10	2.9	4.7	ns
		XCS20	3.3	5.8	ns
		XCS30	3.6	6.2	ns
		XCS40	3.9	6.7	ns

Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

| Symbol | Description | Speed Grade | | | | Units |
| | | -4 | | -3 | | |
		Min	Max	Min	Max	
Clocks						
T_{CH}	Clock High time	3.0	-	4.0	-	ns
T_{CL}	Clock Low time	3.0	-	4.0	-	ns
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	1.2	-	1.6	ns
T_{IHO}	F/G inputs via H to X/Y outputs	-	2.0	-	2.7	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.7	-	2.2	ns
CLB Fast Carry Logic						
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	1.7	-	2.1	ns
T_{ASCY}	Add/Subtract input (F3) to C_{OUT}	-	2.8	-	3.7	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	1.2	-	1.4	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	2.0	-	2.6	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.5	-	0.6	ns
Sequential Delays						
T_{CKO}	Clock K to Flip-Flop outputs Q	-	2.1	-	2.8	ns
Setup Time before Clock K						
T_{ICK}	F/G inputs	1.8	-	2.4	-	ns
T_{IHCK}	F/G inputs via H	2.9	-	3.9	-	ns
T_{HH1CK}	C inputs via H1 through H	2.3	-	3.3	-	ns
T_{DICK}	C inputs via DIN	1.3	-	2.0	-	ns
T_{ECCK}	C inputs via EC	2.0	-	2.6	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	2.5	-	4.0	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	3.0	-	4.0	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	3.0	-	4.0	ns
Global Set/Reset						
T_{MRW}	Minimum GSR pulse width	11.5	-	13.5	-	ns
T_{MRQ}	Delay from GSR input to any Q	See page 50 for T_{RRI} values per device.				
F_{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	166	-	125	MHz

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

DS060_35_080400

Figure 34: **Delay Factor at Various Capacitive Loads**

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)
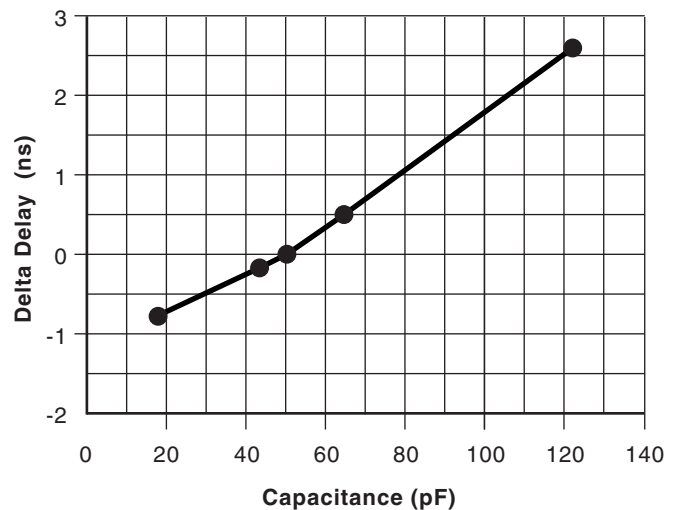
All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation[1]							
T_{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T_{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

Notes:
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port
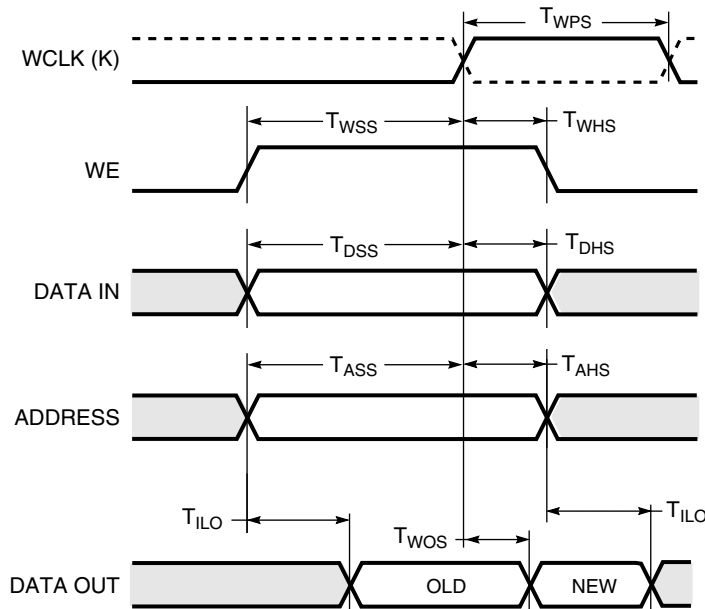
Dual Port
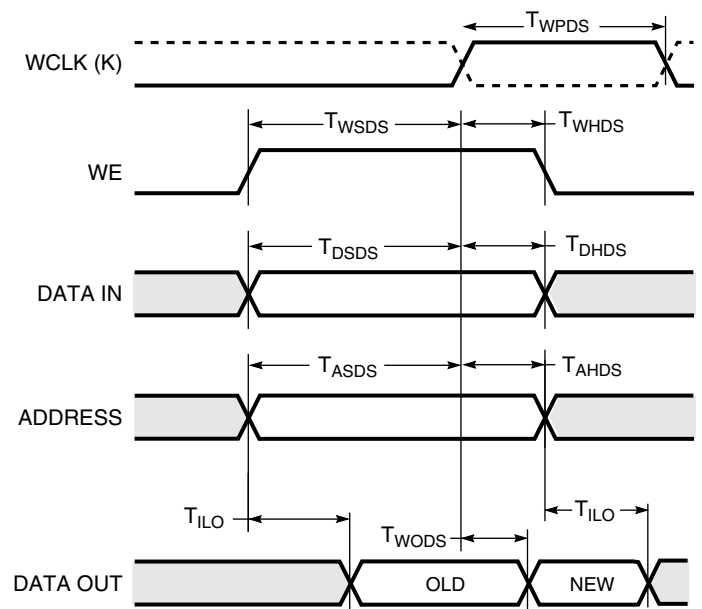
DS060_34_011300

Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

| Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Setup Times							
T_{ECIK}	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T_{PICK}	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T_{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T_{PID}	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T_{Delay}	$T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T_{RRI}	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

Notes:
1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Table 18: **Pin Descriptions** *(Continued)*

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84[4]	VQ100	Bndry Scan
I/O	P70	P71	238[3]
I/O (D0[2], DIN)	P71	P72	241[3]
I/O, SGCK4[1], GCK6[2] (DOUT)	P72	P73	244[3]
CCLK	P73	P74	-
VCC	P74	P75	-
O, TDO	P75	P76	0
GND	P76	P77	-
I/O	P77	P78	2
I/O, PGCK4[1], GCK7[2]	P78	P79	5
I/O (CS1[2])	P79	P80	8
I/O	P80	P81	11
I/O	P81	P82	14
I/O	P82	P83	17
I/O	-	P84	20
I/O	-	P85	23
I/O	P83	P86	26
I/O	P84	P87	29
GND	P1	P88	-

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS05XL is not part of the Boundary Scan chain. For the XCS05XL, subtract 1 from all Boundary Scan numbers from GCK3 on (127 and higher).
4. PC84 package discontinued by **PDN2004-01**

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
VCC	P2	P89	D7	P128	-
I/O	P3	P90	A6	P129	44
I/O	P4	P91	B6	P130	47
I/O	-	P92	C6	P131	50
I/O	-	P93	D6	P132	53
I/O	P5	P94	A5	P133	56
I/O	P6	P95	B5	P134	59
I/O	-	-	C5	P135	62
I/O	-	-	D5	P136	65
GND	-	-	A4	P137	-
I/O	P7	P96	B4	P138	68
I/O	P8	P97	C4	P139	71
I/O	-	-	A3	P140	74
I/O	-	-	B3	P141	77
I/O	P9	P98	C3	P142	80

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O, SGCK1[1] GCK8[2]	P10	P99	A2	P143	83
VCC	P11	P100	B2	P144	-
GND	P12	P1	A1	P1	-
I/O, PGCK1[1] GCK1[2]	P13	P2	B1	P2	86
I/O	P14	P3	C2	P3	89
I/O	-	-	C1	P4	92
I/O	-	-	D4	P5	95
I/O, TDI	P15	P4	D3	P6	98
I/O, TCK	P16	P5	D2	P7	101
GND	-	-	D1	P8	-
I/O	-	-	E4	P9	104
I/O	-	-	E3	P10	107
I/O, TMS	P17	P6	E2	P11	110
I/O	P18	P7	E1	P12	113
I/O	-	-	F4	P13	116
I/O	-	P8	F3	P14	119
I/O	P19	P9	F2	P15	122
I/O	P20	P10	F1	P16	125
GND	P21	P11	G2	P17	-
VCC	P22	P12	G1	P18	-
I/O	P23	P13	G3	P19	128
I/O	P24	P14	G4	P20	131
I/O	-	P15	H1	P21	134
I/O	-	-	H2	P22	137
I/O	P25	P16	H3	P23	140
I/O	P26	P17	H4	P24	143
I/O	-	-	J1	P25	146
I/O	-	-	J2	P26	149
GND	-	-	J3	P27	-
I/O	P27	P18	J4	P28	152
I/O	-	P19	K1	P29	155
I/O	-	-	K2	P30	158
I/O	-	-	K3	P31	161
I/O	P28	P20	L1	P32	164
I/O, SGCK2[1] GCK2[2]	P29	P21	L2	P33	167
Not Connected[1] M1[2]	P30	P22	L3	P34	170
GND	P31	P23	M1	P35	-
MODE[1], M0[2]	P32	P24	M2	P36	173

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O	P80	P81	A10	P116	17
GND	-	-	C9	P118	-
I/O	-	-	B9	P119	20
I/O	-	-	A9	P120	23
I/O	P81	P82	D8	P121	26
I/O	P82	P83	C8	P122	29
I/O	-	P84	B8	P123	32
I/O	-	P85	A8	P124	35
I/O	P83	P86	B7	P125	38
I/O	P84	P87	A7	P126	41
GND	P1	P88	C7	P127	-

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS10XL is not part of the Boundary Scan chain. For the XCS10XL, subtract 1 from all Boundary Scan numbers from GCK3 on (175 and higher).
4. PC84 and CS144 packages discontinued by **PDN2004-01**

Additional XCS10/XL Package Pins

TQ144					
Not Connected Pins					
P117	-	-	-	-	-
5/5/97					

CS144					
Not Connected Pins					
D9	-	-	-	-	-
4/28/99					

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
VCC	P89	D7	P128	P183	-
I/O	P90	A6	P129	P184	62
I/O	P91	B6	P130	P185	65
I/O	P92	C6	P131	P186	68
I/O	P93	D6	P132	P187	71
I/O	-	-	-	P188	74
I/O	-	-	-	P189	77
I/O	P94	A5	P133	P190	80
I/O	P95	B5	P134	P191	83
VCC[2]	-	-	-	P192	-
I/O	-	C5	P135	P193	86
I/O	-	D5	P136	P194	89
GND	-	A4	P137	P195	-
I/O	-	-	-	P196	92
I/O	-	-	-	P197	95
I/O	-	-	-	P198	98
I/O	-	-	-	P199	101
I/O	P96	B4	P138	P200	104
I/O	P97	C4	P139	P201	107
I/O	-	A3	P140	P204	110
I/O	-	B3	P141	P205	113
I/O	P98	C3	P142	P206	116

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O, SGCK1[1], GCK8[2]	P99	A2	P143	P207	119
VCC	P100	B2	P144	P208	-
GND	P1	A1	P1	P1	-
I/O, PGCK1[1], GCK1[2]	P2	B1	P2	P2	122
I/O	P3	C2	P3	P3	125
I/O	-	C1	P4	P4	128
I/O	-	D4	P5	P5	131
I/O, TDI	P4	D3	P6	P6	134
I/O, TCK	P5	D2	P7	P7	137
I/O	-	-	-	P8	140
I/O	-	-	-	P9	143
I/O	-	-	-	P10	146
I/O	-	-	-	P11	149
GND	-	D1	P8	P13	-
I/O	-	E4	P9	P14	152
I/O	-	E3	P10	P15	155
I/O, TMS	P6	E2	P11	P16	158
I/O	P7	E1	P12	P17	161
VCC[2]	-	-	-	P18	-
I/O	-	-	-	P19	164
I/O	-	-	-	P20	167

Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 [1]	P33 [1]	P39	P65	P71 [1]
P86 [1]	P92	P111	P121[1]	P140[1]	P144
P165	P173[1]	P192[1]	P202	P203	-
9/16/98					

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by **PDN2004-01**

XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
VCC	P89	P128	P183	P212	VCC[4]	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC[4]	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND[4]	GND[4]	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1[1], GCK8[2]	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC[4]	A1	-
GND	P1	P1	P1	P1	GND[4]	GND[4]	-
I/O, PGCK1[1], GCK1[2]	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	-	-	P190	B16	A15	23
I/O	-	P117	P166	P191	A16	E14	26
I/O	-	-	P167	P192	C15	C14	29
I/O	-	-	P168	P193	B15	B14	32
I/O	-	-	P169	P194	A15	D14	35
GND	-	P118	P170	P196	GND[4]	GND[4]	-
I/O	-	P119	P171	P197	B14	A14	38
I/O	-	P120	P172	P198	A14	C13	41
I/O	-	-	-	P199	C13	B13	44
I/O	-	-	-	P200	B13	A13	47
VCC	-	-	P173	P201	VCC[4]	D13	-
I/O	P82	P121	P174	P202	C12	B12	50
I/O	P83	P122	P175	P203	B12	D12	53
I/O	-	-	P176	P205	A12	A11	56
I/O	-	-	P177	P206	B11	B11	59
I/O	P84	P123	P178	P207	C11	C11	62
I/O	P85	P124	P179	P208	A11	D11	65
I/O	P86	P125	P180	P209	A10	A10	68
I/O	P87	P126	P181	P210	B10	B10	71
GND	P88	P127	P182	P211	GND[4]	GND[4]	-

2/8/00

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND[4] or V_{CC}[4] are internally bonded to Ground or V_{CC} planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by **PDN2004-01**

Additional XCS30/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

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CS280

VCC Pins					
A1	A7	C10	C17	D13	G1
G1	G19	K2	K17	M4	N16
T7	U3	U10	U17	W13	-
GND Pins					

Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: **Component Availability Chart for Spartan/XL FPGAs**

Device	Pins Type Code	84 Plastic PLCC PC84[3]	100 Plastic VQFP VQ100[3]	144 Chip Scale CS144[3]	144 Plastic TQFP TQ144	208 Plastic PQFP PQ208	240 Plastic PQFP PQ240	256 Plastic BGA BG256[3]	280 Chip Scale CS280[3]
XCS05	-3	C[3]	C, I	-	-	-	-	-	-
	-4	C[3]	C	-	-	-	-	-	-
XCS10	-3	C[3]	C, I	-	C	-	-	-	-
	-4	C[3]	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C[3]	-	C, I	C, I	C	C[3]	-
	-4	-	C[3]	-	C	C	C	C[3]	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C[3]	C, I	-	-	-	-	-	-
	-5	C[3]	C	-	-	-	-	-	-
XCS10XL	-4	C[3]	C, I	C[3]	C	-	-	-	-
	-5	C[3]	C	C[3]	C	-	-	-	-
XCS20XL	-4	-	C, I	C[3]	C, I	C, I	-	-	-
	-5	-	C	C[3]	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C[3]
	-5	-	C	-	C	C	C	C	C[3]
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C[3]
	-5	-	-	-	-	C	C	C	C[3]

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Notes:
1. C = Commercial T_J = 0° to +85°C
2. I = Industrial T_J = –40°C to +100°C
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by **PDN2004-01**
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

www.xilinx.com/support/documentation/spartan-xl.htm#19687

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

www.xilinx.com/cgi-bin/thermal/thermal.pl