AMD Xilinx - XCS20XL-4VQG100C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	950
Total RAM Bits	12800
Number of I/O	77
Number of Gates	20000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs20xl-4vqg100c

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds, using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.

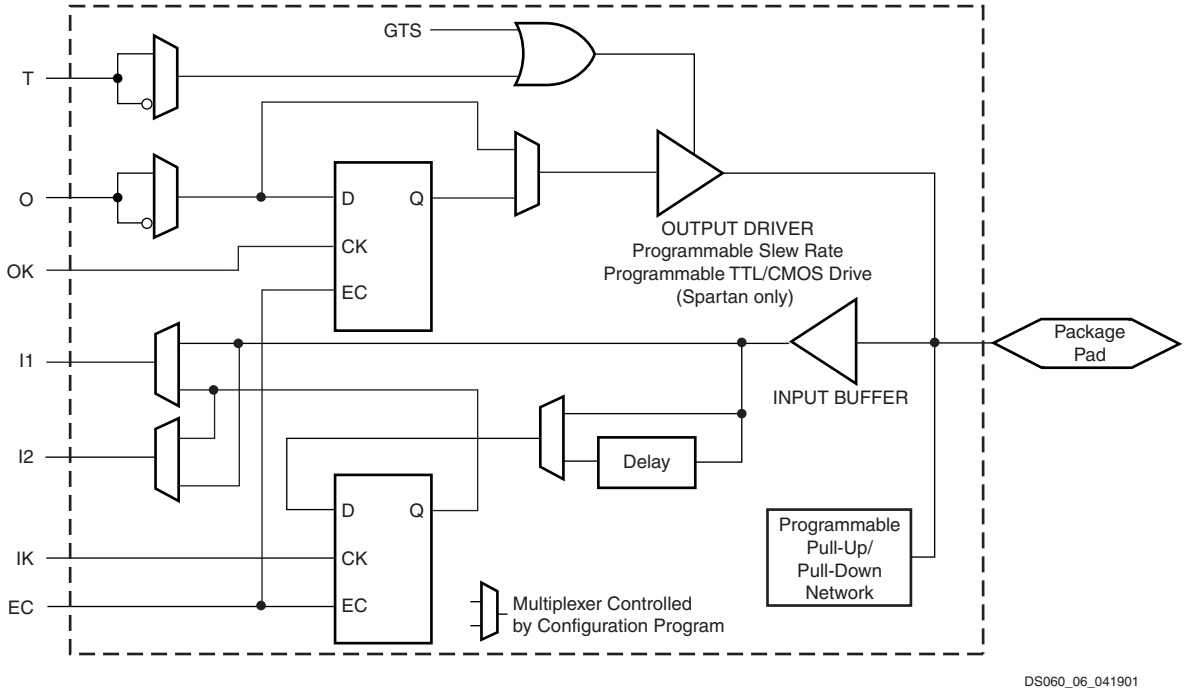


Figure 6: **Simplified Spartan/XL IOB Block Diagram**

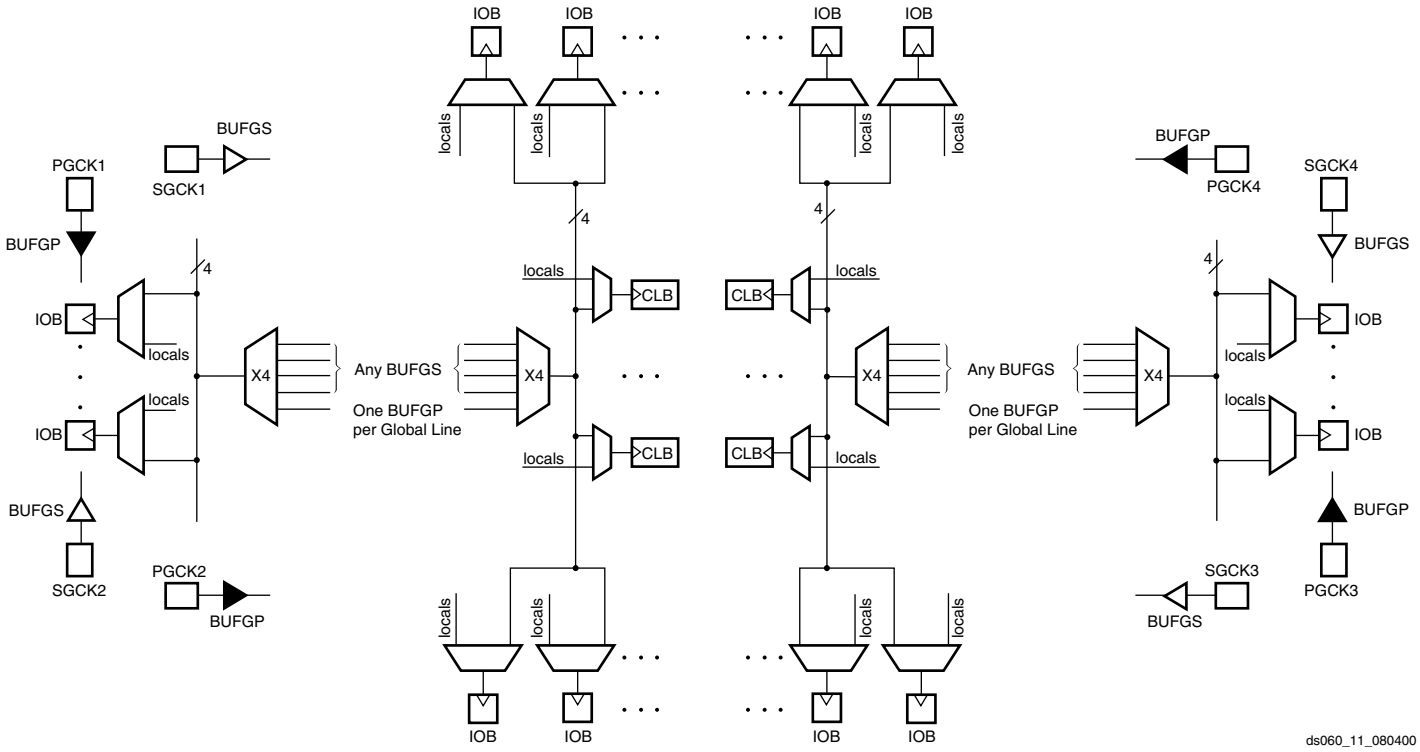


Figure 11: **5V Spartan Family Global Net Distribution**

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 8. Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 8: **CLB Memory Configurations**

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√	–	–

CLB signals from which they are originally derived are shown in Table 10.

Table 10: **Dual-Port RAM Signals**

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F_{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G_{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: *"Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM,"* and *"Synchronous and Asynchronous FIFO Designs."* All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan

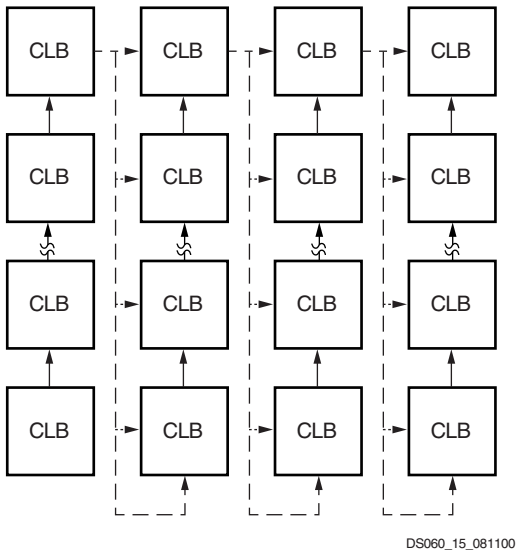


Figure 15: **Available Spartan/XL Carry Propagation Paths**

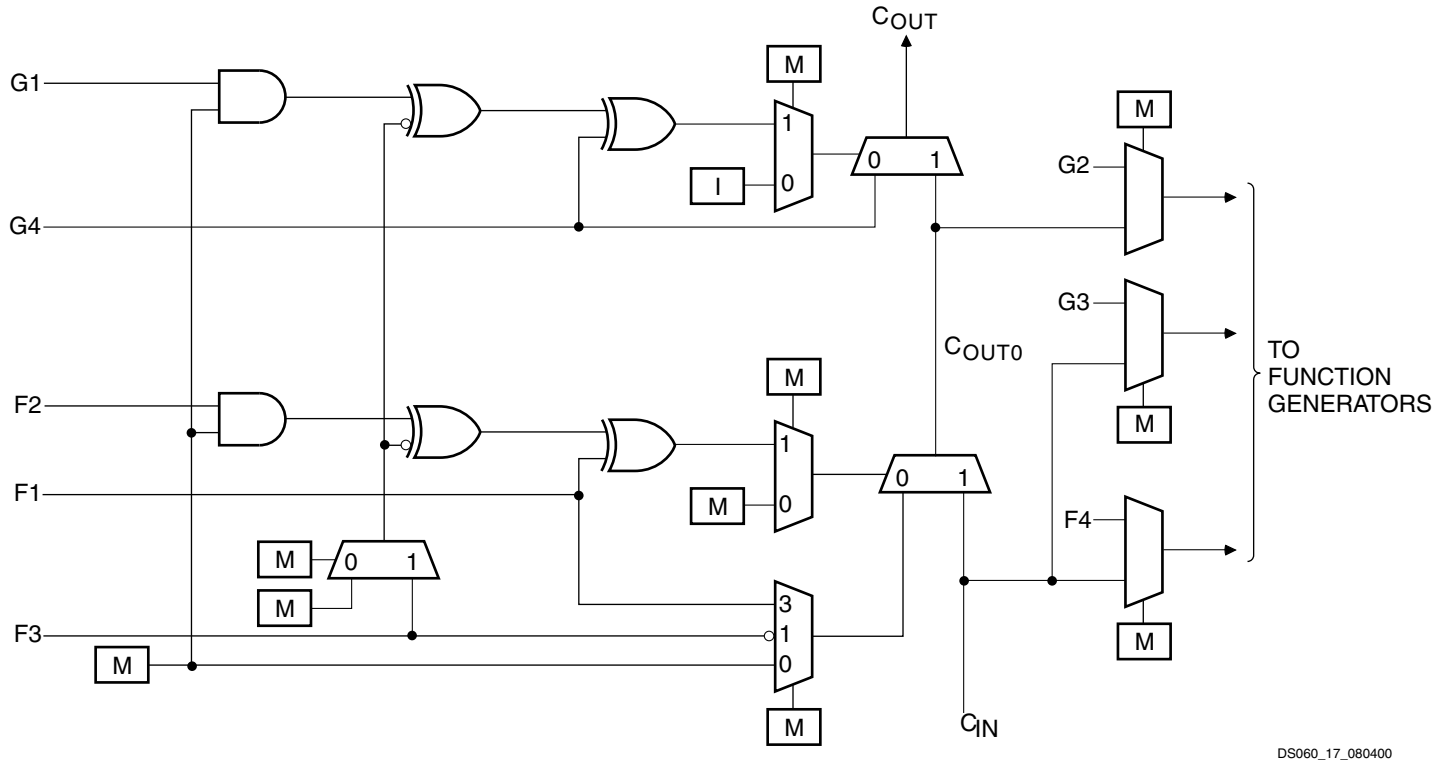


Figure 17: **Detail of Spartan/XL Dedicated Carry Logic**

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

Table 11: **Three-State Buffer Functionality**

IN	T	OUT
X	1	Z
IN	0	IN

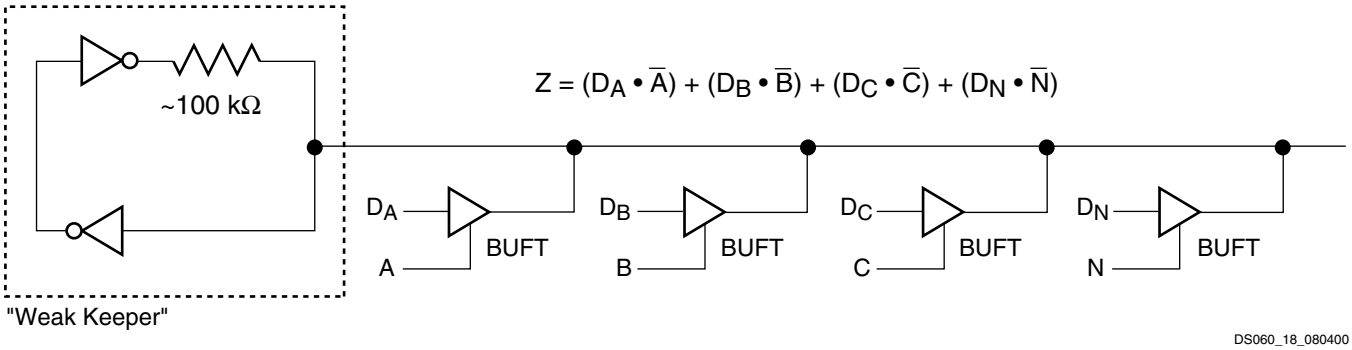
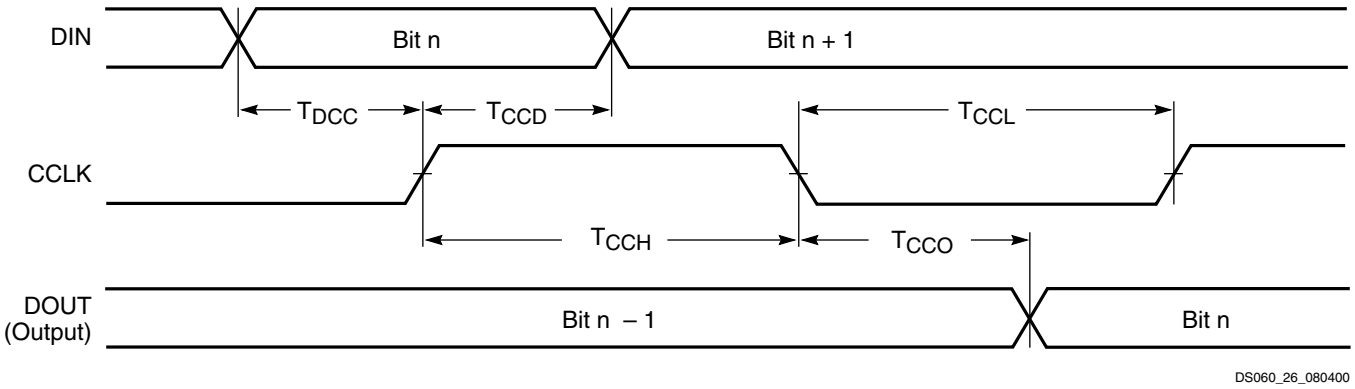


Figure 18: **3-state Buffers Implement a Multiplexer**



Symbol		Description	Min	Max	Units
T_{DCC}	CCLK	DIN setup	20	-	ns
T_{CCD}		DIN hold	0	-	ns
T_{CCO}		DIN to DOUT	-	30	ns
T_{CCH}		High time	40	-	ns
T_{CCL}		Low time	40	-	ns
F_{CC}		Frequency	-	12.5	MHz

Notes:
1. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 26: **Slave Serial Mode Programming Switching Characteristics**

Express Mode (Spartan-XL Family Only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

Pseudo Daisy Chain

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized

to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.

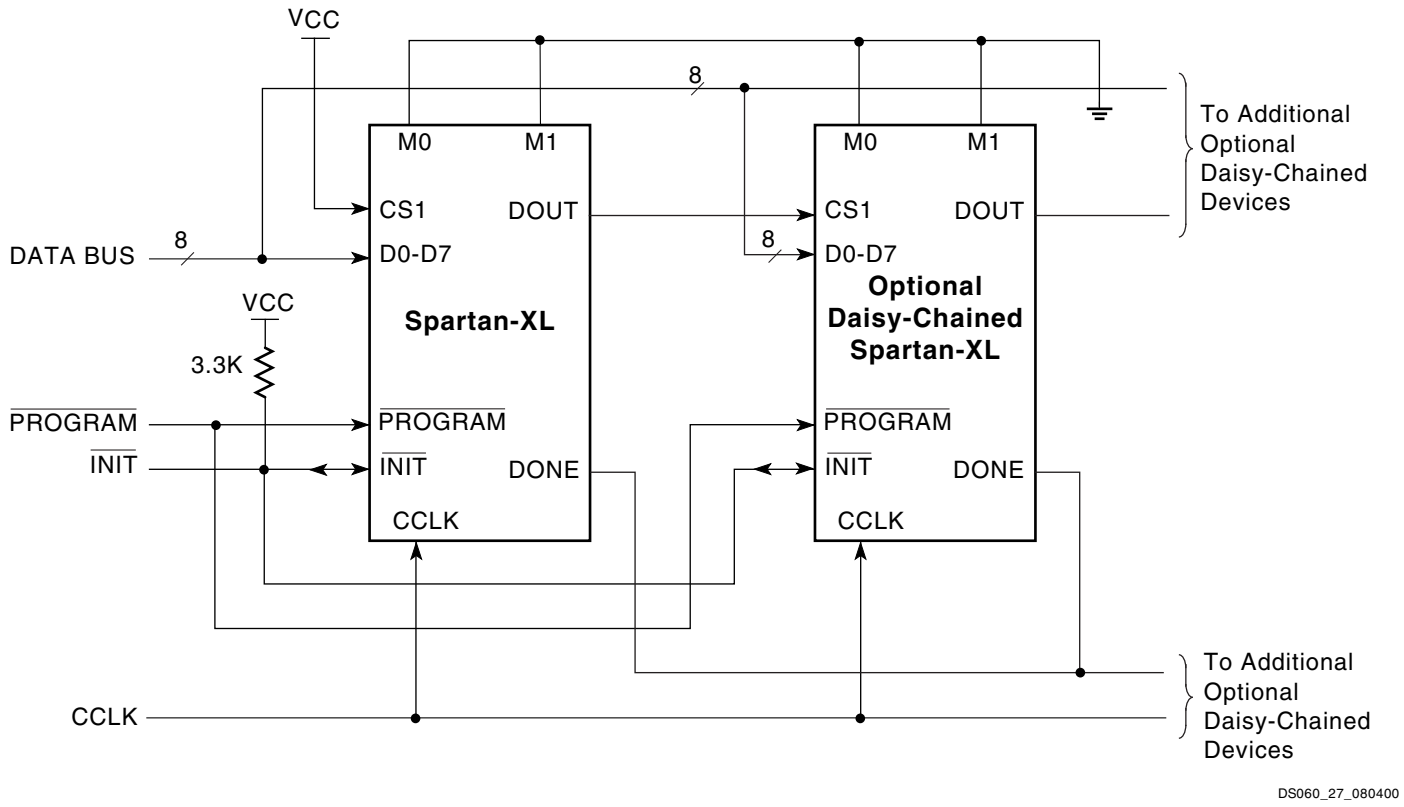


Figure 27: **Express Mode Circuit Diagram**

Table 16: **Spartan/XL Data Stream Formats**

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0](1)
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	11111110b(2)
Data Frame	DATA[n–1:0]	DATA[n–1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes(3)	FFh	FFFFFFFFFFFFFFh

Legend:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Notes:
1. Not used by configuration logic.
2. 11111111b for XCS40XL only.
3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the $\overline{\text{INIT}}$ pin. In Master serial mode, CCLK continues to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling V_{CC}.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

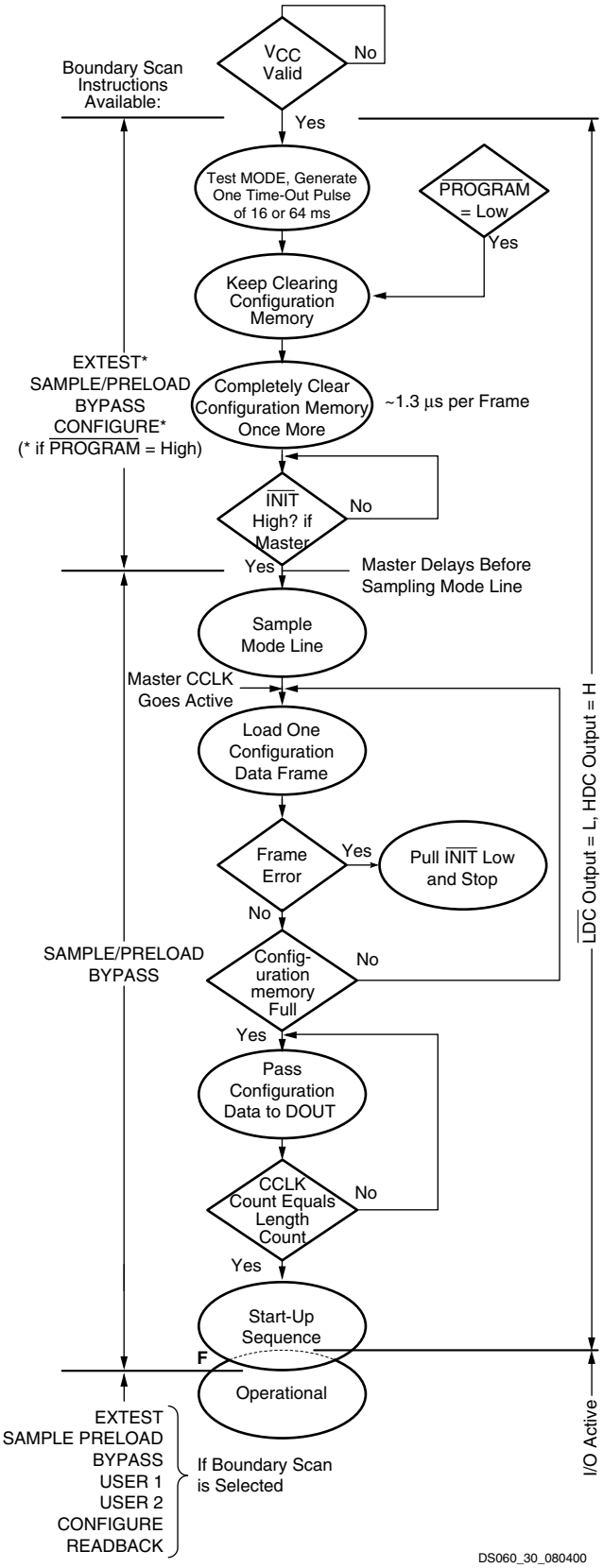


Figure 30: **Power-up Configuration Sequence**

Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count for serial modes. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Spartan-XL family Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{\text{INIT}}$ pin Low. After all configuration frames have been loaded into an FPGA using a serial mode, DOUT again follows the input data so that the remaining data is passed on to the next device. In Spartan-XL family Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See Figure 30.)

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the FPGA keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the $\overline{\text{INIT}}$ input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output. The Spartan/XL FPGA $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up.

Avoid holding $\overline{\text{PROGRAM}}$ Low for more than 500 µs. The 500 µs maximum limit is only a recommendation, not a requirement. The only effect of holding $\overline{\text{PROGRAM}}$ Low for more than 500 µs is an increase in current, measured at about 40 mA in the XCS40XL. This increased current cannot damage the device. This applies only during reconfiguration, not during power-up. The $\overline{\text{INIT}}$ pin can also be held Low to delay reconfiguration, and the same characteristics apply as for the $\overline{\text{PROGRAM}}$ pin.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration causes the FPGA

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 32.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

Readback Capture

When the Readback Capture option is selected, the data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.

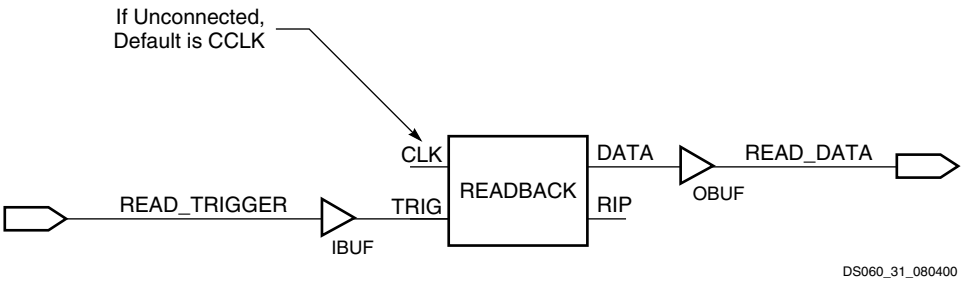


Figure 32: **Readback Example**

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size[1]	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T_{WCTS}		32x1	8.0	-	11.6	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T_{WPTS}		32x1	4.0	-	5.8	-	ns
T_{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T_{ASTS}		32x1	1.5	-	2.0	-	ns
T_{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{AHTS}		32x1	0.0	-	0.0	-	ns
T_{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T_{DSTS}		32x1	1.5	-	1.7	-	ns
T_{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{DHTS}		32x1	0.0	-	0.0	-	ns
T_{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T_{WSTS}		32x1	1.5	-	1.6	-	ns
T_{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{WHTS}		32x1	0.0	-	0.0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T_{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T_{RCT}		32x1	3.8	-	3.8	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T_{IHO}		32x1	-	2.0	-	2.7	ns
T_{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T_{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:
1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Typ.	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min (LVTTL)		2.4	-	-	V
	High-level output voltage @ I_{OH} = –500 µA, (LVCMOS)		90% V_{CC}	-	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (LVTTL)(1)		-	-	0.4	V
	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL)(2)		-	-	0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)		-	-	10% V_{CC}	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		2.5	-	-	V
I_{CCO}	Quiescent FPGA supply current(3,4)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I_{CCPD}	Power Down FPGA supply current(3,5)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I_L	Input or output leakage current		–10	-	10	µA
C_{IN}	Input capacitance (sample tested)		-	-	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V (sample tested)		0.02	-	-	mA

Notes:
1. With up to 64 pins simultaneously sinking 12 mA (default mode).
2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
4. With no output current loads, no active input resistors, and all package pins at V_{CC} or GND.
5. With $\overline{PWRDWN}$ active.

Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CC} lines for a successful power on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Max	Units
I_{CCPO}	Total V_{CC} supply current required during power-on	100	-	mA
T_{CCPO}	V_{CC} ramp time(2,3)	-	50	ms

Notes:
1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CC} ramps from 0 to 3.3V.
2. The ramp time is measured from GND to V_{CC} max on a fully loaded board.
3. V_{CC} must not dip in the negative direction during power on.

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

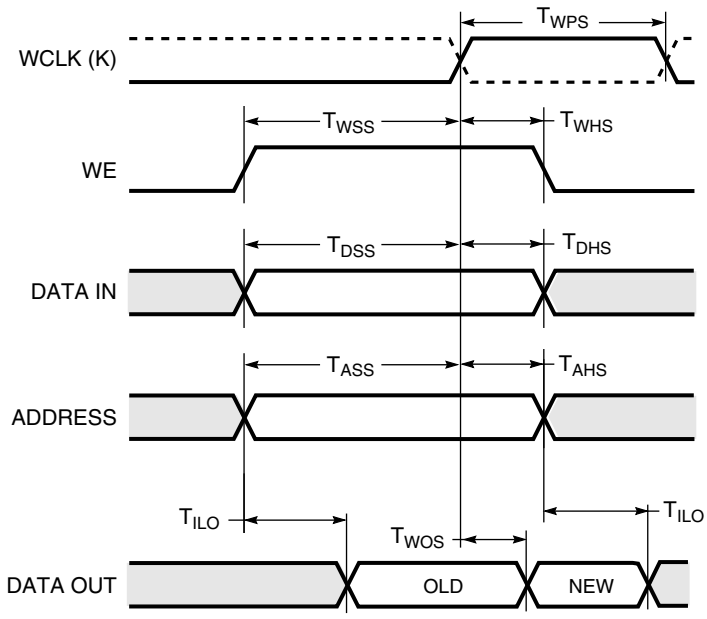
All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation(1)							
T_{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T_{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

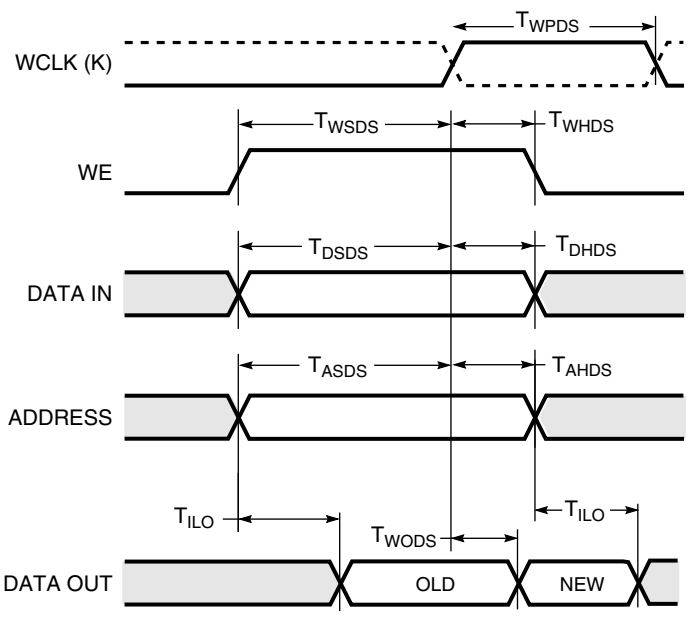
Notes:
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



DS060_34_011300

Table 18: **Pin Descriptions *(Continued)***

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
VCC	P33	P25	N1	P37	-
Not Connect-ed[1] PWRDWN[2]	P34	P26	N2	P38	174 [1]
I/O, PGCK2[1] GCK3[2]	P35	P27	M3	P39	175[3]
I/O (HDC)	P36	P28	N3	P40	178 [3]
I/O	-	-	K4	P41	181 [3]
I/O	-	-	L4	P42	184 [3]
I/O	-	P29	M4	P43	187 [3]
I/O ($\overline{LDC}$)	P37	P30	N4	P44	190 [3]
GND	-	-	K5	P45	-
I/O	-	-	L5	P46	193 [3]
I/O	-	-	M5	P47	196 [3]
I/O	P38	P31	N5	P48	199 [3]
I/O	P39	P32	K6	P49	202 [3]
I/O	-	P33	L6	P50	205 [3]
I/O	-	P34	M6	P51	208 [3]
I/O	P40	P35	N6	P52	211 [3]
I/O ($\overline{INIT}$)	P41	P36	M7	P53	214 [3]
VCC	P42	P37	N7	P54	-
GND	P43	P38	L7	P55	-
I/O	P44	P39	K7	P56	217 [3]
I/O	P45	P40	N8	P57	220 [3]
I/O	-	P41	M8	P58	223 [3]
I/O	-	P42	L8	P59	226 [3]
I/O	P46	P43	K8	P60	229 [3]
I/O	P47	P44	N9	P61	232 [3]
I/O	-	-	M9	P62	235 [3]
I/O	-	-	L9	P63	238 [3]
GND	-	-	K9	P64	-
I/O	P48	P45	N10	P65	241 [3]
I/O	P49	P46	M10	P66	244 [3]
I/O	-	-	L10	P67	247 [3]
I/O	-	-	N11	P68	250 [3]
I/O	P50	P47	M11	P69	253 [3]
I/O, SGCK3[1] GCK4[2]	P51	P48	L11	P70	256 [3]
GND	P52	P49	N12	P71	-
DONE	P53	P50	M12	P72	-
VCC	P54	P51	N13	P73	-
$\overline{PROGRAM}$	P55	P52	M13	P74	-
I/O (D7[2])	P56	P53	L12	P75	259 [3]

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O, PGCK3[1] GCK5[2]	P57	P54	L13	P76	262 [3]
I/O	-	-	K10	P77	265 [3]
I/O	-	-	K11	P78	268 [3]
I/O (D6[2])	P58	P55	K12	P79	271 [3]
I/O	-	P56	K13	P80	274 [3]
GND	-	-	J10	P81	-
I/O	-	-	J11	P82	277 [3]
I/O	-	-	J12	P83	280 [3]
I/O (D5[2])	P59	P57	J13	P84	283 [3]
I/O	P60	P58	H10	P85	286 [3]
I/O	-	P59	H11	P86	289 [3]
I/O	-	P60	H12	P87	292 [3]
I/O (D4[2])	P61	P61	H13	P88	295 [3]
I/O	P62	P62	G12	P89	298 [3]
VCC	P63	P63	G13	P90	-
GND	P64	P64	G11	P91	-
I/O (D3[2])	P65	P65	G10	P92	301 [3]
I/O	P66	P66	F13	P93	304 [3]
I/O	-	P67	F12	P94	307 [3]
I/O	-	-	F11	P95	310 [3]
I/O (D2[2])	P67	P68	F10	P96	313 [3]
I/O	P68	P69	E13	P97	316 [3]
I/O	-	-	E12	P98	319 [3]
I/O	-	-	E11	P99	322 [3]
GND	-	-	E10	P100	-
I/O (D1[2])	P69	P70	D13	P101	325 [3]
I/O	P70	P71	D12	P102	328 [3]
I/O	-	-	D11	P103	331 [3]
I/O	-	-	C13	P104	334 [3]
I/O (D0[2], DIN)	P71	P72	C12	P105	337 [3]
I/O, SGCK4[1] GCK6[2] (DOUT)	P72	P73	C11	P106	340 [3]
CCLK	P73	P74	B13	P107	-
VCC	P74	P75	B12	P108	-
O, TDO	P75	P76	A13	P109	0
GND	P76	P77	A12	P110	-
I/O	P77	P78	B11	P111	2
I/O, PGCK4[1] GCK7[2]	P78	P79	A11	P112	5
I/O	-	-	D10	P113	8
I/O	-	-	C10	P114	11
I/O (CS1[2])	P79	P80	B10	P115	14

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7[2])	P53	L12	P75	P107	367 [3]
I/O, PGCK3[1], GCK5[2]	P54	L13	P76	P108	370 [3]
I/O	-	K10	P77	P109	373 [3]
I/O	-	K11	P78	P110	376 [3]
I/O (D6[2])	P55	K12	P79	P112	379 [3]
I/O	P56	K13	P80	P113	382 [3]
I/O	-	-	-	P114	385 [3]
I/O	-	-	-	P115	388 [3]
I/O	-	-	-	P116	391 [3]
I/O	-	-	-	P117	394 [3]
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 [3]
I/O	-	J12	P83	P120	400 [3]
VCC[2]	-	-	-	P121	-
I/O (D5[2])	P57	J13	P84	P122	403 [3]
I/O	P58	H10	P85	P123	406 [3]
I/O	-	-	-	P124	409 [3]
I/O	-	-	-	P125	412 [3]
I/O	P59	H11	P86	P126	415 [3]
I/O	P60	H12	P87	P127	418 [3]
I/O (D4[2])	P61	H13	P88	P128	421 [3]
I/O	P62	G12	P89	P129	424 [3]
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3[2])	P65	G10	P92	P132	427 [3]
I/O	P66	F13	P93	P133	430 [3]
I/O	P67	F12	P94	P134	433 [3]
I/O	-	F11	P95	P135	436 [3]
I/O	-	-	-	P136	439 [3]
I/O	-	-	-	P137	442 [3]
I/O (D2[2])	P68	F10	P96	P138	445 [3]
I/O	P69	E13	P97	P139	448 [3]
VCC[2]	-	-	-	P140	-
I/O	-	E12	P98	P141	451 [3]
I/O	-	E11	P99	P142	454 [3]
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 [3]
I/O	-	-	-	P146	460 [3]
I/O	-	-	-	P147	463 [3]
I/O	-	-	-	P148	466 [3]
I/O (D1[2])	P70	D13	P101	P149	469 [3]
I/O	P71	D12	P102	P150	472 [3]
I/O	-	D11	P103	P151	475 [3]

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 [3]
I/O (D0[2], DIN)	P72	C12	P105	P153	481 [3]
I/O, SGCK4[1], GCK6[2] (DOUT)	P73	C11	P106	P154	484 [3]
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4[1], GCK7[2]	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1[2])	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC[2]	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

2/8/00

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	P18	P28	P44	P52	V1	T1	272
I/O	P19	P29	P45	P53	T4	T2	275
I/O	-	P30	P46	P54	U3	T3	278
I/O	-	P31	P47	P55	V2	U1	281
I/O	P20	P32	P48	P56	W1	V1	284
I/O, SGCK2[1], GCK2[2]	P21	P33	P49	P57	V3	U2	287
Not Connected[1], M1[2]	P22	P34	P50	P58	W2	V2	290
GND	P23	P35	P51	P59	GND[4]	GND[4]	-
MODE[1], M0[2]	P24	P36	P52	P60	Y1	W1	293
VCC	P25	P37	P53	P61	VCC[4]	U3	-
Not Connected [1], $\overline{\text{PWRDWN}}$[2]	P26	P38	P54	P62	W3	V3	294 [1]
I/O, PGCK2[1], GCK3[2]	P27	P39	P55	P63	Y2	W2	295 [3]
I/O (HDC)	P28	P40	P56	P64	W4	W3	298 [3]
I/O	-	P41	P57	P65	V4	T4	301 [3]
I/O	-	P42	P58	P66	U5	U4	304 [3]
I/O	P29	P43	P59	P67	Y3	V4	307 [3]
I/O ($\overline{\text{LDC}}$)	P30	P44	P60	P68	Y4	W4	310 [3]
I/O	-	-	P61	P69	V5	T5	313 [3]
I/O	-	-	P62	P70	W5	W5	316 [3]
I/O	-	-	P63	P71	Y5	R6	319 [3]
I/O	-	-	P64	P72	V6	U6	322 [3]
I/O	-	-	P65	P73	W6	V6	325 [3]
I/O	-	-	-	P74	Y6	T6	328 [3]
GND	-	P45	P66	P75	GND[4]	GND[4]	-
I/O	-	P46	P67	P76	W7	W6	331 [3]
I/O	-	P47	P68	P77	Y7	U7	334 [3]
I/O	P31	P48	P69	P78	V8	V7	337 [3]
I/O	P32	P49	P70	P79	W8	W7	340 [3]
VCC	-	-	P71	P80	VCC[4]	T7	-
I/O	-	-	P72	P81	Y8	W8	343 [3]
I/O	-	-	P73	P82	U9	U8	346 [3]
I/O	-	-	-	P84	Y9	W9	349 [3]
I/O	-	-	-	P85	W10	V9	352 [3]
I/O	P33	P50	P74	P86	V10	U9	355 [3]
I/O	P34	P51	P75	P87	Y10	T9	358 [3]
I/O	P35	P52	P76	P88	Y11	W10	361 [3]
I/O ($\overline{\text{INIT}}$)	P36	P53	P77	P89	W11	V10	364 [3]
VCC	P37	P54	P78	P90	VCC[4]	U10	-
GND	P38	P55	P79	P91	GND[4]	GND[4]	-
I/O	P39	P56	P80	P92	V11	T10	367 [3]
I/O	P40	P57	P81	P93	U11	R10	370 [3]
I/O	P41	P58	P82	P94	Y12	W11	373 [3]
I/O	P42	P59	P83	P95	W12	V11	376 [3]
I/O	-	-	P84	P96	V12	U11	379 [3]

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	-	P85	P97	U12	T11	382 [3]
I/O	-	-	-	P99	V13	U12	385 [3]
I/O	-	-	-	P100	Y14	T12	388 [3]
VCC	-	-	P86	P101	VCC[4]	W13	-
I/O	P43	P60	P87	P102	Y15	V13	391 [3]
I/O	P44	P61	P88	P103	V14	U13	394 [3]
I/O	-	P62	P89	P104	W15	T13	397 [3]
I/O	-	P63	P90	P105	Y16	W14	400 [3]
GND	-	P64	P91	P106	GND[4]	GND[4]	-
I/O	-	-	-	P107	V15	V14	403 [3]
I/O	-	-	P92	P108	W16	U14	406 [3]
I/O	-	-	P93	P109	Y17	T14	409 [3]
I/O	-	-	P94	P110	V16	R14	412 [3]
I/O	-	-	P95	P111	W17	W15	415 [3]
I/O	-	-	P96	P112	Y18	U15	418 [3]
I/O	P45	P65	P97	P113	U16	V16	421 [3]
I/O	P46	P66	P98	P114	V17	U16	424 [3]
I/O	-	P67	P99	P115	W18	W17	427 [3]
I/O	-	P68	P100	P116	Y19	W18	430 [3]
I/O	P47	P69	P101	P117	V18	V17	433 [3]
I/O, SGCK3[1], GCK4[2]	P48	P70	P102	P118	W19	V18	436 [3]
GND	P49	P71	P103	P119	GND[4]	GND[4]	-
DONE	P50	P72	P104	P120	Y20	W19	-
VCC	P51	P73	P105	P121	VCC[4]	U17	-
$\overline{\text{PROGRAM}}$	P52	P74	P106	P122	V19	U18	-
I/O (D7[2])	P53	P75	P107	P123	U19	V19	439 [3]
I/O, PGCK3[1], GCK5[2]	P54	P76	P108	P124	U18	U19	442 [3]
I/O	-	P77	P109	P125	T17	T16	445 [3]
I/O	-	P78	P110	P126	V20	T17	448 [3]
I/O	-	-	-	P127	U20	T18	451 [3]
I/O	-	-	P111	P128	T18	T19	454 [3]
I/O (D6[2])	P55	P79	P112	P129	T19	R16	457 [3]
I/O	P56	P80	P113	P130	T20	R19	460 [3]
I/O	-	-	P114	P131	R18	P15	463 [3]
I/O	-	-	P115	P132	R19	P17	466 [3]
I/O	-	-	P116	P133	R20	P18	469 [3]
I/O	-	-	P117	P134	P18	P16	472 [3]
GND	-	P81	P118	P135	GND[4]	GND[4]	-
I/O	-	-	-	P136	P20	P19	475 [3]
I/O	-	-	-	P137	N18	N17	478 [3]
I/O	-	P82	P119	P138	N19	N18	481 [3]
I/O	-	P83	P120	P139	N20	N19	484 [3]
VCC	-	-	P121	P140	VCC[4]	N16	-
I/O (D5[2])	P57	P84	P122	P141	M17	M19	487 [3]
I/O	P58	P85	P123	P142	M18	M17	490 [3]

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	-	-	P190	B16	A15	23
I/O	-	P117	P166	P191	A16	E14	26
I/O	-	-	P167	P192	C15	C14	29
I/O	-	-	P168	P193	B15	B14	32
I/O	-	-	P169	P194	A15	D14	35
GND	-	P118	P170	P196	GND[4]	GND[4]	-
I/O	-	P119	P171	P197	B14	A14	38
I/O	-	P120	P172	P198	A14	C13	41
I/O	-	-	-	P199	C13	B13	44
I/O	-	-	-	P200	B13	A13	47
VCC	-	-	P173	P201	VCC[4]	D13	-
I/O	P82	P121	P174	P202	C12	B12	50
I/O	P83	P122	P175	P203	B12	D12	53
I/O	-	-	P176	P205	A12	A11	56
I/O	-	-	P177	P206	B11	B11	59
I/O	P84	P123	P178	P207	C11	C11	62
I/O	P85	P124	P179	P208	A11	D11	65
I/O	P86	P125	P180	P209	A10	A10	68
I/O	P87	P126	P181	P210	B10	B10	71
GND	P88	P127	P182	P211	GND[4]	GND[4]	-

2/8/00

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND[4] or V_{CC}[4] are internally bonded to Ground or V_{CC} planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01

Additional XCS30/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

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BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

CS280

VCC Pins					
A1	A7	C10	C17	D13	G1
G1	G19	K2	K17	M4	N16
T7	U3	U10	U17	W13	-
GND Pins					

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	P90	P105	Y16	W14	466 (3)
GND	P91	P106	GND(4)	GND(4)	-
I/O	-	P107	V15	V14	469 (3)
I/O	P92	P108	W16	U14	472 (3)
I/O	P93	P109	Y17	T14	475 (3)
I/O	P94	P110	V16	R14	478 (3)
I/O	P95	P111	W17	W15	481 (3)
I/O	P96	P112	Y18	U15	484 (3)
I/O	-	-	-	T15	487 (3)
I/O	-	-	-	W16	490 (3)
I/O	P97	P113	U16	V16	493 (3)
I/O	P98	P114	V17	U16	496 (3)
I/O	P99	P115	W18	W17	499 (3)
I/O	P100	P116	Y19	W18	502 (3)
I/O	P101	P117	V18	V17	505 (3)
I/O, SGCK3(1), GCK4(2)	P102	P118	W19	V18	508 (3)
GND	P103	P119	GND(4)	GND(4)	-
DONE	P104	P120	Y20	W19	-
VCC	P105	P121	VCC(4)	VCC(4)	-
$\overline{\text{PROGRAM}}$	P106	P122	V19	U18	-
I/O (D7(2))	P107	P123	U19	V19	511 (3)
I/O, PGCK3(1), GCK5(2)	P108	P124	U18	U19	514 (3)
I/O	P109	P125	T17	T16	517 (3)
I/O	P110	P126	V20	T17	520 (3)
I/O	-	P127	U20	T18	523 (3)
I/O	P111	P128	T18	T19	526 (3)
I/O	-	-	-	R15	529 (3)
I/O	-	-	-	R17	523 (3)
I/O (D6(2))	P112	P129	T19	R16	535 (3)
I/O	P113	P130	T20	R19	538 (3)
I/O	P114	P131	R18	P15	541 (3)
I/O	P115	P132	R19	P17	544 (3)
I/O	P116	P133	R20	P18	547 (3)
I/O	P117	P134	P18	P16	550 (3)
GND	P118	P135	GND(4)	GND(4)	-
I/O	-	P136	P20	P19	553 (3)
I/O	-	P137	N18	N17	556 (3)
I/O	P119	P138	N19	N18	559 (3)
I/O	P120	P139	N20	N19	562 (3)
VCC	P121	P140	VCC(4)	VCC(4)	-
I/O (D5(2))	P122	P141	M17	M19	565 (3)
I/O	P123	P142	M18	M17	568 (3)

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	-	-	-	M18	571 (3)
I/O	-	-	M19	M16	574 (3)
I/O	P124	P144	M20	L19	577 (3)
I/O	P125	P145	L19	L18	580 (3)
I/O	P126	P146	L18	L17	583 (3)
I/O	P127	P147	L20	L16	586 (3)
I/O (D4(2))	P128	P148	K20	K19	589 (3)
I/O	P129	P149	K19	K18	592 (3)
VCC	P130	P150	VCC(4)	VCC(4)	-
GND	P131	P151	GND(4)	GND(4)	-
I/O (D3(2))	P132	P152	K18	K16	595 (3)
I/O	P133	P153	K17	K15	598 (3)
I/O	P134	P154	J20	J19	601 (3)
I/O	P135	P155	J19	J18	604 (3)
I/O	P136	P156	J18	J17	607 (3)
I/O	P137	P157	J17	J16	610 (3)
I/O	-	-	H20	H19	613 (3)
I/O	-	-	-	H18	616 (3)
I/O (D2(2))	P138	P159	H19	H17	619 (3)
I/O	P139	P160	H18	H16	622 (3)
VCC	P140	P161	VCC(4)	VCC(4)	-
I/O	P141	P162	G19	G18	625 (3)
I/O	P142	P163	F20	G17	628 (3)
I/O	-	P164	G18	G16	631 (3)
I/O	-	P165	F19	F19	634 (3)
GND	P143	P166	GND(4)	GND(4)	-
I/O	-	P167	F18	F18	637 (3)
I/O	P144	P168	E19	F17	640 (3)
I/O	P145	P169	D20	F16	643 (3)
I/O	P146	P170	E18	F15	646 (3)
I/O	P147	P171	D19	E19	649 (3)
I/O	P148	P172	C20	E17	652 (3)
I/O (D1(2))	P149	P173	E17	E16	655 (3)
I/O	P150	P174	D18	D19	658 (3)
I/O	-	-	-	D18	661 (3)
I/O	-	-	-	D17	664 (3)
I/O	P151	P175	C19	C19	667 (3)
I/O	P152	P176	B20	B19	670 (3)
I/O (D0(2), DIN)	P153	P177	C18	C18	673 (3)
I/O, SGCK4(1), GCK6(2) (DOUT)	P154	P178	B19	B18	676 (3)
CCLK	P155	P179	A20	A19	-
VCC	P156	P180	VCC(4)	VCC(4)	-

Table 20: **User I/O Chart for Spartan/XL FPGAs**

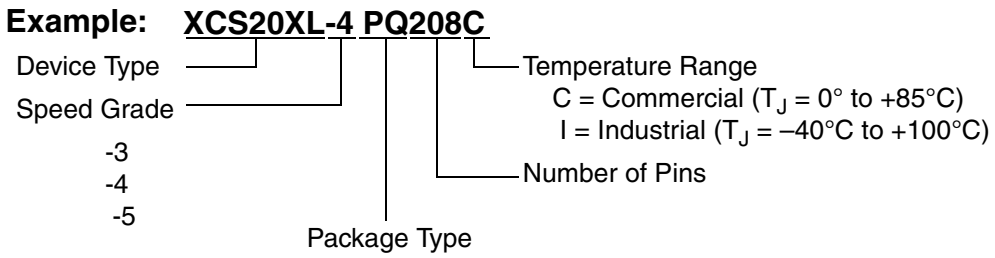
Device	Max I/O	Package Type							
		PC84(1)	VQ100(1)	CS144(1)	TQ144	PQ208	PQ240	BG256(1)	CS280(1)
XCS05	80	61(1)	77	-	-	-	-	-	-
XCS10	112	61(1)	77	-	112	-	-	-	-
XCS20	160	-	77	-	113	160	-	-	-
XCS30	192	-	77(1)	-	113	169	192	192(1)	-
XCS40	224	-	-	-	-	169	192	205	-
XCS05XL	80	61(1)	77(2)	-	-	-	-	-	-
XCS10XL	112	61(1)	77(2)	112(1)	112(2)	-	-	-	-
XCS20XL	160	-	77(2)	113(1)	113(2)	160(2)	-	-	-
XCS30XL	192	-	77(2)	-	113(2)	169(2)	192(2)	192(2)	192(1)
XCS40XL	224	-	-	-	-	169(2)	192(2)	205(2)	224(1)

6/25/08

Notes:

1. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01
2. These Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Ordering Information



BG = Ball Grid Array
BGG = Ball Grid Array (Pb-free)
PC = Plastic Lead Chip Carrier
PQ = Plastic Quad Flat Pack
PQG = Plastic Quad Flat Pack (Pb-free)
VQ = Very Thin Quad Flat Pack
VQG = Very Thin Quad Flat Pack (Pb-free)
TQ = Thin Quad Flat Pack
TQG = Thin Quad Flat Pack (Pb-free)
CS = Chip Scale