



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	950
Total RAM Bits	12800
Number of I/O	113
Number of Gates	20000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs20xl-5cs144c

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

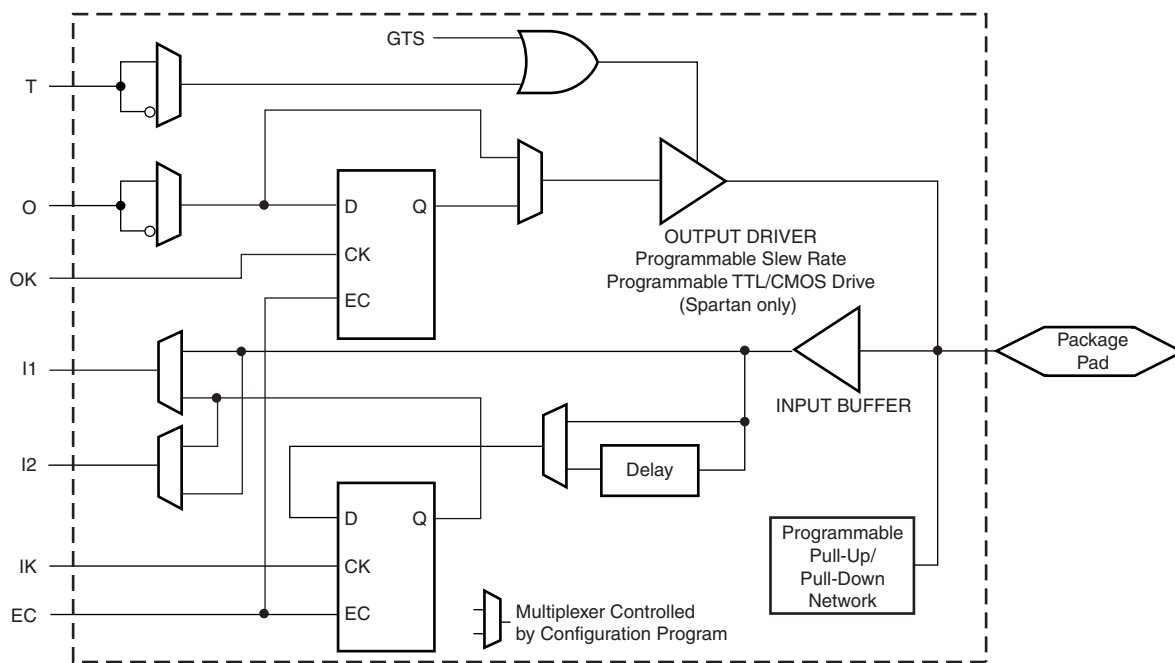
The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop. The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds,

using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.



DS060_06_041901

Figure 6: Simplified Spartan/XL IOB Block Diagram

and Spartan-XL families, speeding up arithmetic and counting functions.

The carry chain in 5V Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in Spartan-XL devices can only run up the column, providing even higher speed.

Figure 16, page 18 shows a Spartan/XL FPGA CLB with dedicated fast carry logic. The carry logic shares operand

and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 17, page 19 shows the details of the Spartan/XL FPGA carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 16.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

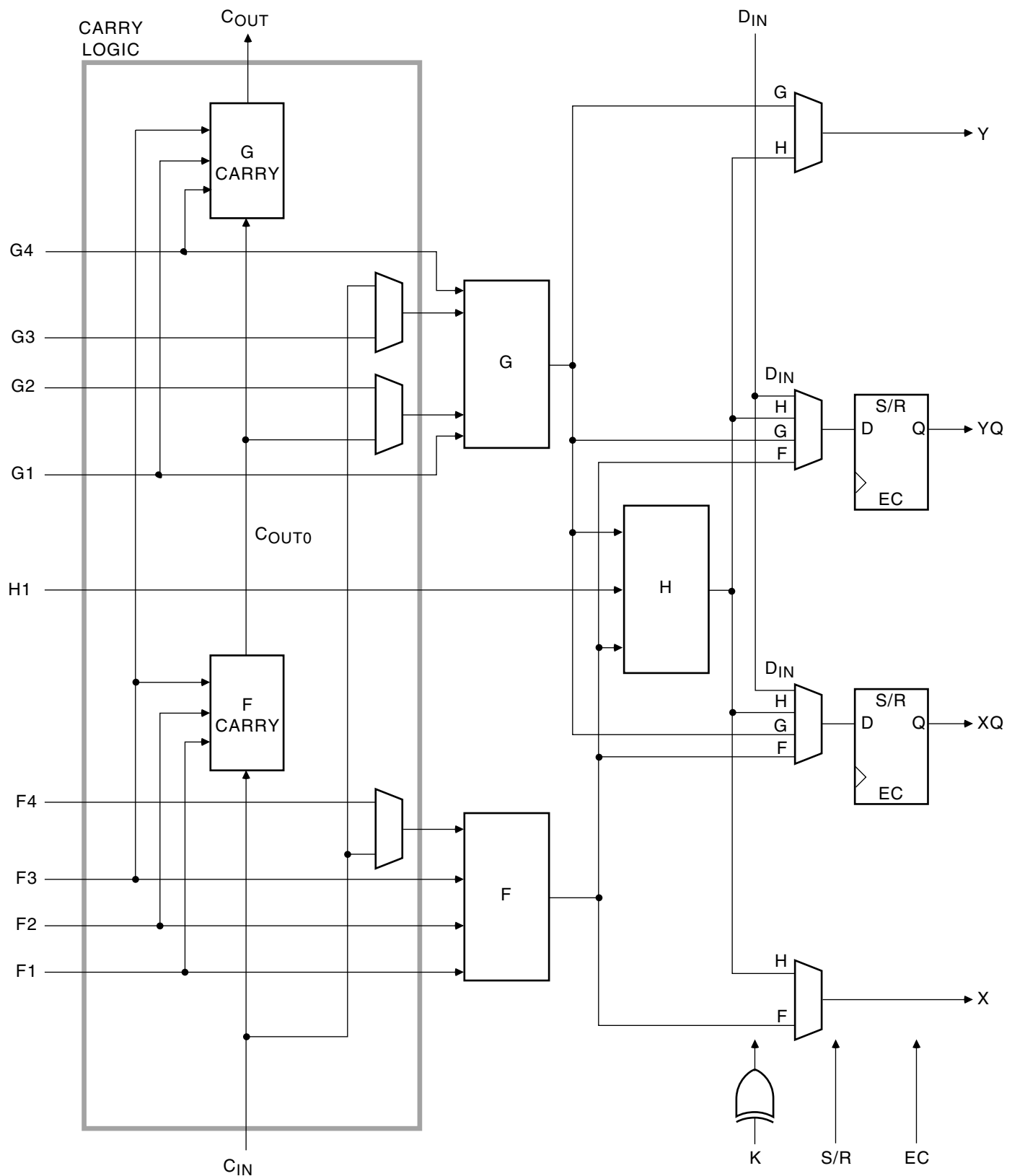


Figure 16: Fast Carry Logic in Spartan/XL CLB

DS060_16_080400

On-Chip Oscillator

Spartan/XL devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, V_{CC} , and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8-MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in [Figure 3, page 5](#) for the CLB and [Figure 5, page 6](#) for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

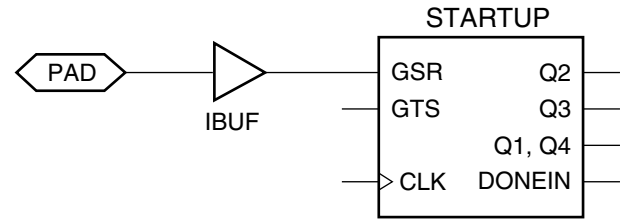
GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See [Figure 19.](#)) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

Global 3-State

A separate Global 3-state line (GTS) as shown in [Figure 6, page 7](#) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in [Figure 19](#) for GSR except the IBUF would be

connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-state signal. Alternatively, GTS can be driven from any internal node.



DS060_19_080400

Figure 19: Symbols for Global Set/Reset

Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan compatible device. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan and Spartan-XL families implement IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Spartan/XL devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "Boundary Scan in FPGA Devices."

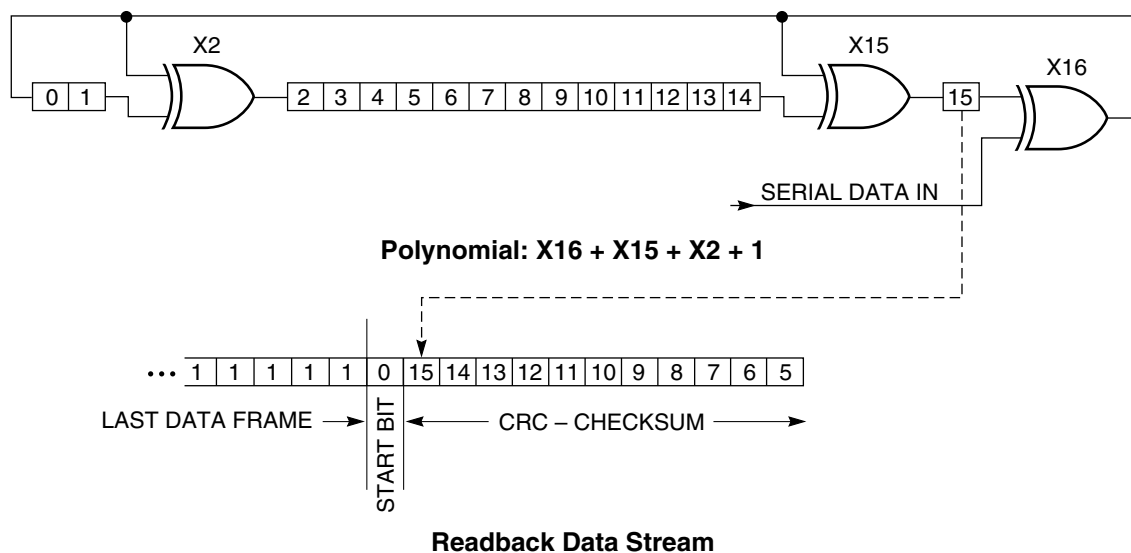


Figure 29: Circuit for Generating CRC-16

DS060_29_080400

Configuration Sequence

There are four major steps in the Spartan/XL FPGA power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC} . When all \overline{INIT} pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin

Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the \overline{INIT} input.

Initialization

During initialization and configuration, user pins \overline{HDC} , \overline{LDC} , \overline{INIT} and \overline{DONE} provide status outputs for the system interface. The outputs \overline{LDC} , \overline{INIT} and \overline{DONE} are held Low and \overline{HDC} is held High starting at the initial application of power.

The open drain \overline{INIT} pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive \overline{INIT} . Two internal clocks after the \overline{INIT} pin is recognized as High, the device samples the \overline{MODE} pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

to wait after completing the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing the state of the Mode pins, and is ready to start the configuration process. A master device waits up to an additional 300 μs to make sure that any slaves in the optional daisy chain have seen that $\overline{\text{INIT}}$ is High.

For more details on Configuration, refer to the Xilinx Application Note "FPGA Configuration Guidelines" (XAPP090).

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user system. Start-up must make sure that the user logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the Global Set/Reset (GSR) at the right time.

Start-Up Initiation

Two conditions have to be met in order for the start-up sequence to begin:

- The chip's internal memory must be full, and
- The configuration length count must be met, exactly.

In all configuration modes except Express mode, Spartan/XL devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

In Express mode, there is no length count. The start-up sequence for each device begins when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

Start-Up Events

The device can be programmed to control three start-up events.

- The release of the open-drain DONE output
- The termination of the Global Three-State and the change of configuration-related pins to the user function, activating all IOBs.
- The termination of the Global Set/Reset initialization of all CLB and IOB storage elements.

Figure 31 describes start-up timing in detail. The three events — DONE going High, the internal GSR being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. This relative timing is selected by options in the bitstream generation software. Heavy lines in Figure 31 show the default timing. The thin lines indicate all other possible timing options. The start-up logic must be clocked until the "F" (Finished) state is reached.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. GSR is then released another clock period later to make sure that user operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 31, but the designer can modify it to meet particular requirements.

Start-Up Clock

Normally, the start-up sequence is controlled by the internal device oscillator (CCLK), which is asynchronous to the system clock. As a configuration option, they can be triggered by an on-chip user net called UCLK. This user net can be accessed by placing the STARTUP library symbol, and the start-up modes are known as UCLK_NOSYNC or UCLK_SYNC. This allows the device to wake up in synchronism with the user system.

DONE Pin

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to the start-up control logic. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK_SYNC or UCLK_SYNC. When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK_NOSYNC or UCLK_NOSYNC. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, while the other configuration modes can use any of the four timing sequences.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

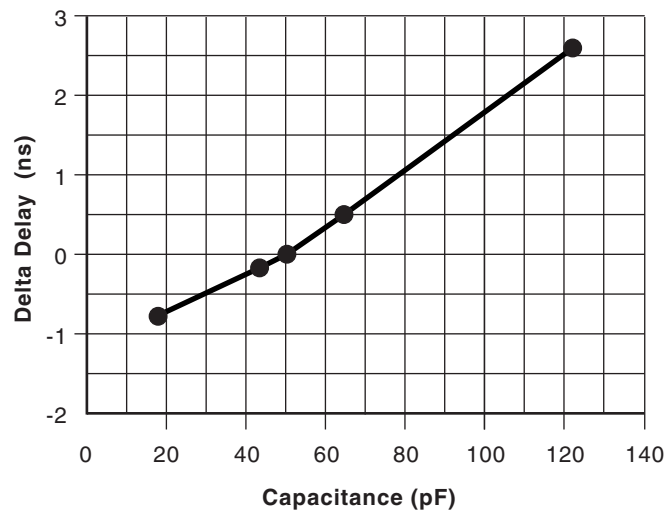
Symbol	Single Port RAM	Size ⁽¹⁾	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Write Operation							
T _{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T _{WCTS}		32x1	8.0	-	11.6	-	ns
T _{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T _{WPTS}		32x1	4.0	-	5.8	-	ns
T _{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T _{ASTS}		32x1	1.5	-	2.0	-	ns
T _{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{AHTS}		32x1	0.0	-	0.0	-	ns
T _{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T _{DSTS}		32x1	1.5	-	1.7	-	ns
T _{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{DHTS}		32x1	0.0	-	0.0	-	ns
T _{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T _{WSTS}		32x1	1.5	-	1.6	-	ns
T _{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{WHTS}		32x1	0.0	-	0.0	-	ns
T _{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T _{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T _{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T _{RCT}		32x1	3.8	-	3.8	-	ns
T _{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T _{IHO}		32x1	-	2.0	-	2.7	ns
T _{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T _{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



DS060_35_080400

Figure 34: Delay Factor at Various Capacitive Loads

Spartan-XL Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clocks						
T _{CH}	Clock High time	2.0	-	2.3	-	ns
T _{CL}	Clock Low time	2.0	-	2.3	-	ns
Combinatorial Delays						
T _{ILO}	F/G inputs to X/Y outputs	-	1.0	-	1.1	ns
T _{IHO}	F/G inputs via H to X/Y outputs	-	1.7	-	2.0	ns
T _{ITO}	F/G inputs via transparent latch to Q outputs	-	1.5	-	1.8	ns
T _{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.5	-	1.8	ns
Sequential Delays						
T _{CKO}	Clock K to Flip-Flop or latch outputs Q	-	1.2	-	1.4	ns
Setup Time before Clock K						
T _{ICK}	F/G inputs	0.6	-	0.7	-	ns
T _{IHCK}	F/G inputs via H	1.3	-	1.6	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T _{RPW}	Width (High)	2.5	-	2.8	-	ns
T _{RIO}	Delay from C inputs via S/R, going High to Q	-	2.3	-	2.7	ns
Global Set/Reset						
T _{MRW}	Minimum GSR Pulse Width	10.5	-	11.5	-	ns
T _{MRQ}	Delay from GSR input to any Q	See page 60 for T _{RRI} values per device.				
F _{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	250	-	217	MHz

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size ⁽¹⁾	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Write Operation							
T _{WCS}	Address write cycle time (clock K period)	16x2	7.7	-	8.4	-	ns
T _{WCTS}		32x1	7.7	-	8.4	-	ns
T _{WPS}	Clock K pulse width (active edge)	16x2	3.1	-	3.6	-	ns
T _{WPTS}		32x1	3.1	-	3.6	-	ns
T _{ASS}	Address setup time before clock K	16x2	1.3	-	1.5	-	ns
T _{ASTS}		32x1	1.5	-	1.7	-	ns
T _{DSS}	DIN setup time before clock K	16x2	1.5	-	1.7	-	ns
T _{DSTS}		32x1	1.8	-	2.1	-	ns
T _{WSS}	WE setup time before clock K	16x2	1.4	-	1.6	-	ns
T _{WSTS}		32x1	1.3	-	1.5	-	ns
	All hold times after clock K	16x2	0.0	-	0.0	-	ns
T _{WOS}	Data valid after clock K	32x1	-	4.5	-	5.3	ns
T _{WOTS}		16x2	-	5.4	-	6.3	ns
Read Operation							
T _{RC}	Address read cycle time	16x2	2.6	-	3.1	-	ns
T _{RCT}		32x1	3.8	-	5.5	-	ns
T _{ILO}	Data Valid after address change (no Write Enable)	16x2	-	1.0	-	1.1	ns
T _{IHO}		32x1	-	1.7	-	2.0	ns
T _{ICK}	Address setup time before clock K	16x2	0.6	-	0.7	-	ns
T _{IHCK}		32x1	1.3	-	1.6	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Setup and Hold

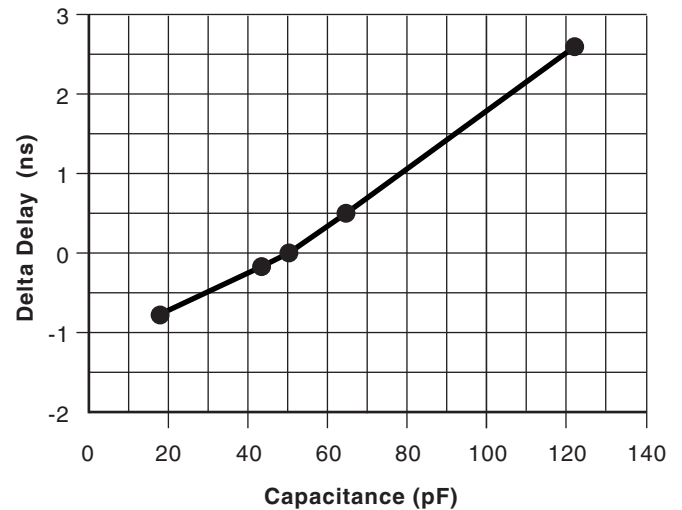
Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Input Setup/Hold Times Using Global Clock and IFF					
T _{SUF} /T _{HF}	No Delay	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
T _{SU} /T _H	Full Delay	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



DS060_35_080400

Figure 35: Delay Factor at Various Capacitive Loads

Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol		Device	Speed Grade				Units
			-5		-4		
	Description		Min	Max	Min	Max	
Setup Times							
T _{ECIK}	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T _{PICK}	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T _{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T _{PID}	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T _{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T _{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T _{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T _{Delay}	T _{PICKD} = T _{PICK} + T _{Delay} T _{PDLI} = T _{PLI} + T _{Delay}	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T _{RRI}	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

Notes:

- Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
- Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84(4)	VQ100	CS144(2,4)	TQ144	Bndry Scan
I/O	P80	P81	A10	P116	17
GND	-	-	C9	P118	-
I/O	-	-	B9	P119	20
I/O	-	-	A9	P120	23
I/O	P81	P82	D8	P121	26
I/O	P82	P83	C8	P122	29
I/O	-	P84	B8	P123	32
I/O	-	P85	A8	P124	35
I/O	P83	P86	B7	P125	38
I/O	P84	P87	A7	P126	41
GND	P1	P88	C7	P127	-

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS10XL is not part of the Boundary Scan chain. For the XCS10XL, subtract 1 from all Boundary Scan numbers from GCK3 on (175 and higher).
4. PC84 and CS144 packages discontinued by [PDN2004-01](#)

Additional XCS10/XL Package Pins

TQ144					
Not Connected Pins					
P117	-	-	-	-	-
5/5/97					

CS144					
Not Connected Pins					
D9	-	-	-	-	-
4/28/99					

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144(2,4)	TQ144	PQ208	Bndry Scan
VCC	P89	D7	P128	P183	-
I/O	P90	A6	P129	P184	62
I/O	P91	B6	P130	P185	65
I/O	P92	C6	P131	P186	68
I/O	P93	D6	P132	P187	71
I/O	-	-	-	P188	74
I/O	-	-	-	P189	77
I/O	P94	A5	P133	P190	80
I/O	P95	B5	P134	P191	83
VCC ⁽²⁾	-	-	-	P192	-
I/O	-	C5	P135	P193	86
I/O	-	D5	P136	P194	89
GND	-	A4	P137	P195	-
I/O	-	-	-	P196	92
I/O	-	-	-	P197	95
I/O	-	-	-	P198	98
I/O	-	-	-	P199	101
I/O	P96	B4	P138	P200	104
I/O	P97	C4	P139	P201	107
I/O	-	A3	P140	P204	110
I/O	-	B3	P141	P205	113
I/O	P98	C3	P142	P206	116

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144(2,4)	TQ144	PQ208	Bndry Scan
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P99	A2	P143	P207	119
VCC	P100	B2	P144	P208	-
GND	P1	A1	P1	P1	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	B1	P2	P2	122
I/O	P3	C2	P3	P3	125
I/O	-	C1	P4	P4	128
I/O	-	D4	P5	P5	131
I/O, TDI	P4	D3	P6	P6	134
I/O, TCK	P5	D2	P7	P7	137
I/O	-	-	-	P8	140
I/O	-	-	-	P9	143
I/O	-	-	-	P10	146
I/O	-	-	-	P11	149
GND	-	D1	P8	P13	-
I/O	-	E4	P9	P14	152
I/O	-	E3	P10	P15	155
I/O, TMS	P6	E2	P11	P16	158
I/O	P7	E1	P12	P17	161
VCC ⁽²⁾	-	-	-	P18	-
I/O	-	-	-	P19	164
I/O	-	-	-	P20	167

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7 ⁽²⁾)	P53	L12	P75	P107	367 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P54	L13	P76	P108	370 ⁽³⁾
I/O	-	K10	P77	P109	373 ⁽³⁾
I/O	-	K11	P78	P110	376 ⁽³⁾
I/O (D6 ⁽²⁾)	P55	K12	P79	P112	379 ⁽³⁾
I/O	P56	K13	P80	P113	382 ⁽³⁾
I/O	-	-	-	P114	385 ⁽³⁾
I/O	-	-	-	P115	388 ⁽³⁾
I/O	-	-	-	P116	391 ⁽³⁾
I/O	-	-	-	P117	394 ⁽³⁾
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 ⁽³⁾
I/O	-	J12	P83	P120	400 ⁽³⁾
VCC ⁽²⁾	-	-	-	P121	-
I/O (D5 ⁽²⁾)	P57	J13	P84	P122	403 ⁽³⁾
I/O	P58	H10	P85	P123	406 ⁽³⁾
I/O	-	-	-	P124	409 ⁽³⁾
I/O	-	-	-	P125	412 ⁽³⁾
I/O	P59	H11	P86	P126	415 ⁽³⁾
I/O	P60	H12	P87	P127	418 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	H13	P88	P128	421 ⁽³⁾
I/O	P62	G12	P89	P129	424 ⁽³⁾
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3 ⁽²⁾)	P65	G10	P92	P132	427 ⁽³⁾
I/O	P66	F13	P93	P133	430 ⁽³⁾
I/O	P67	F12	P94	P134	433 ⁽³⁾
I/O	-	F11	P95	P135	436 ⁽³⁾
I/O	-	-	-	P136	439 ⁽³⁾
I/O	-	-	-	P137	442 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	F10	P96	P138	445 ⁽³⁾
I/O	P69	E13	P97	P139	448 ⁽³⁾
VCC ⁽²⁾	-	-	-	P140	-
I/O	-	E12	P98	P141	451 ⁽³⁾
I/O	-	E11	P99	P142	454 ⁽³⁾
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 ⁽³⁾
I/O	-	-	-	P146	460 ⁽³⁾
I/O	-	-	-	P147	463 ⁽³⁾
I/O	-	-	-	P148	466 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	D13	P101	P149	469 ⁽³⁾
I/O	P71	D12	P102	P150	472 ⁽³⁾
I/O	-	D11	P103	P151	475 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	C12	P105	P153	481 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	C11	P106	P154	484 ⁽³⁾
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1 ⁽²⁾)	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC ⁽²⁾	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

2/8/00

Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 ⁽¹⁾	P33 ⁽¹⁾	P39	P65	P71 ⁽¹⁾
P86 ⁽¹⁾	P92	P111	P121 ⁽¹⁾	P140 ⁽¹⁾	P144
P165	P173 ⁽¹⁾	P192 ⁽¹⁾	P202	P203	-
9/16/98					

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by [PDN2004-01](#)

XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
VCC	P89	P128	P183	P212	VCC ⁽⁴⁾	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC ⁽⁴⁾	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC ⁽⁴⁾	A1	-
GND	P1	P1	P1	P1	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	P5	P5	P5	D3	C1	155
I/O, TDI	P4	P6	P6	P6	E4	D4	158
I/O, TCK	P5	P7	P7	P7	C1	D3	161
I/O	-	-	P8	P8	D1	E2	164
I/O	-	-	P9	P9	E3	E4	167
I/O	-	-	P10	P10	E2	E1	170
I/O	-	-	P11	P11	E1	F5	173
I/O	-	-	P12	P12	F3	F3	176
I/O	-	-	-	P13	F2	F2	179
GND	-	P8	P13	P14	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P9	P14	P15	G3	F4	182
I/O	-	P10	P15	P16	G2	F1	185
I/O, TMS	P6	P11	P16	P17	G1	G3	188
I/O	P7	P12	P17	P18	H3	G2	191
VCC	-	-	P18	P19	VCC ⁽⁴⁾	G1	-
I/O	-	-	-	P20	H2	G4	194
I/O	-	-	-	P21	H1	H1	197
I/O	-	-	P19	P23	J2	H4	200
I/O	-	-	P20	P24	J1	J1	203
I/O	-	P13	P21	P25	K2	J2	206
I/O	P8	P14	P22	P26	K3	J3	209
I/O	P9	P15	P23	P27	K1	J4	212
I/O	P10	P16	P24	P28	L1	K1	215
GND	P11	P17	P25	P29	GND ⁽⁴⁾	GND ⁽⁴⁾	-
VCC	P12	P18	P26	P30	VCC ⁽⁴⁾	K2	-
I/O	P13	P19	P27	P31	L2	K3	218
I/O	P14	P20	P28	P32	L3	K4	221
I/O	P15	P21	P29	P33	L4	K5	224
I/O	-	P22	P30	P34	M1	L1	227
I/O	-	-	P31	P35	M2	L2	230
I/O	-	-	P32	P36	M3	L3	233
I/O	-	-	-	P38	N1	M2	236
I/O	-	-	-	P39	N2	M3	239
VCC	-	-	P33	P40	VCC ⁽⁴⁾	M4	-
I/O	P16	P23	P34	P41	P1	N1	242
I/O	P17	P24	P35	P42	P2	N2	245
I/O	-	P25	P36	P43	R1	N3	248
I/O	-	P26	P37	P44	P3	N4	251
GND	-	P27	P38	P45	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P46	T1	P1	254
I/O	-	-	P39	P47	R3	P2	257
I/O	-	-	P40	P48	T2	P3	260
I/O	-	-	P41	P49	U1	P4	263
I/O	-	-	P42	P50	T3	P5	266
I/O	-	-	P43	P51	U2	R1	269

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	-	P190	B16	A15	23
I/O	-	P117	P166	P191	A16	E14	26
I/O	-	-	P167	P192	C15	C14	29
I/O	-	-	P168	P193	B15	B14	32
I/O	-	-	P169	P194	A15	D14	35
GND	-	P118	P170	P196	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P119	P171	P197	B14	A14	38
I/O	-	P120	P172	P198	A14	C13	41
I/O	-	-	-	P199	C13	B13	44
I/O	-	-	-	P200	B13	A13	47
VCC	-	-	P173	P201	VCC ⁽⁴⁾	D13	-
I/O	P82	P121	P174	P202	C12	B12	50
I/O	P83	P122	P175	P203	B12	D12	53
I/O	-	-	P176	P205	A12	A11	56
I/O	-	-	P177	P206	B11	B11	59
I/O	P84	P123	P178	P207	C11	C11	62
I/O	P85	P124	P179	P208	A11	D11	65
I/O	P86	P125	P180	P209	A10	A10	68
I/O	P87	P126	P181	P210	B10	B10	71
GND	P88	P127	P182	P211	GND ⁽⁴⁾	GND ⁽⁴⁾	-

2/8/00

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND⁽⁴⁾ or VCC⁽⁴⁾ are internally bonded to Ground or VCC planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)

Additional XCS30/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

2/12/98

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

GND Pins

A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

6/4/97

CS280

VCC Pins					
A1	A7	C10	C17	D13	G1
G1	G19	K2	K17	M4	N16
T7	U3	U10	U17	W13	-
GND Pins					

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
GND	P25	P29	GND ⁽⁴⁾	GND ⁽⁴⁾	-
VCC	P26	P30	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P27	P31	L2	K3	254
I/O	P28	P32	L3	K4	257
I/O	P29	P33	L4	K5	260
I/O	P30	P34	M1	L1	263
I/O	P31	P35	M2	L2	266
I/O	P32	P36	M3	L3	269
I/O	-	-	M4	L4	272
I/O	-	-	-	M1	275
I/O	-	P38	N1	M2	278
I/O	-	P39	N2	M3	281
VCC	P33	P40	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P34	P41	P1	N1	284
I/O	P35	P42	P2	N2	287
I/O	P36	P43	R1	N3	290
I/O	P37	P44	P3	N4	293
GND	P38	P45	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P46	T1	P1	296
I/O	P39	P47	R3	P2	299
I/O	P40	P48	T2	P3	302
I/O	P41	P49	U1	P4	305
I/O	P42	P50	T3	P5	308
I/O	P43	P51	U2	R1	311
I/O	-	-	-	R2	314
I/O	-	-	-	R4	317
I/O	P44	P52	V1	T1	320
I/O	P45	P53	T4	T2	323
I/O	P46	P54	U3	T3	326
I/O	P47	P55	V2	U1	329
I/O	P48	P56	W1	V1	332
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P49	P57	V3	U2	335
Not Connected ⁽¹⁾ M1 ⁽²⁾	P50	P58	W2	V2	338
GND	P51	P59	GND ⁽⁴⁾	GND ⁽⁴⁾	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P52	P60	Y1	W1	341
VCC	P53	P61	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
Not Connected ⁽¹⁾ PWRDWN ⁽²⁾	P54	P62	W3	V3	342 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P55	P63	Y2	W2	343 ⁽³⁾

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
I/O (HDC)	P56	P64	W4	W3	346 ⁽³⁾
I/O	P57	P65	V4	T4	349 ⁽³⁾
I/O	P58	P66	U5	U4	352 ⁽³⁾
I/O	P59	P67	Y3	V4	355 ⁽³⁾
I/O (LDC)	P60	P68	Y4	W4	358 ⁽³⁾
I/O	-	-	-	R5	361 ⁽³⁾
I/O	-	-	-	U5	364 ⁽³⁾
I/O	P61	P69	V5	T5	367 ⁽³⁾
I/O	P62	P70	W5	W5	370 ⁽³⁾
I/O	P63	P71	Y5	R6	373 ⁽³⁾
I/O	P64	P72	V6	U6	376 ⁽³⁾
I/O	P65	P73	W6	V6	379 ⁽³⁾
I/O	-	P74	Y6	T6	382 ⁽³⁾
GND	P66	P75	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P67	P76	W7	W6	385 ⁽³⁾
I/O	P68	P77	Y7	U7	388 ⁽³⁾
I/O	P69	P78	V8	V7	391 ⁽³⁾
I/O	P70	P79	W8	W7	394 ⁽³⁾
VCC	P71	P80	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P72	P81	Y8	W8	397 ⁽³⁾
I/O	P73	P82	U9	U8	400 ⁽³⁾
I/O	-	-	V9	V8	403 ⁽³⁾
I/O	-	-	W9	T8	406 ⁽³⁾
I/O	-	P84	Y9	W9	409 ⁽³⁾
I/O	-	P85	W10	V9	412 ⁽³⁾
I/O	P74	P86	V10	U9	415 ⁽³⁾
I/O	P75	P87	Y10	T9	418 ⁽³⁾
I/O	P76	P88	Y11	W10	421 ⁽³⁾
I/O (INIT)	P77	P89	W11	V10	424 ⁽³⁾
VCC	P78	P90	VCC ⁽⁴⁾	VCC ⁽⁴⁾	VCC ⁽⁴⁾
GND	P79	P91	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P80	P92	V11	T10	427 ⁽³⁾
I/O	P81	P93	U11	R10	430 ⁽³⁾
I/O	P82	P94	Y12	W11	433 ⁽³⁾
I/O	P83	P95	W12	V11	436 ⁽³⁾
I/O	P84	P96	V12	U11	439 ⁽³⁾
I/O	P85	P97	U12	T11	442 ⁽³⁾
I/O	-	-	Y13	W12	445 ⁽³⁾
I/O	-	-	W13	V12	448 ⁽³⁾
I/O	-	P99	V13	U12	451 ⁽³⁾
I/O	-	P100	Y14	T12	454 ⁽³⁾
VCC	P86	P101	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P87	P102	Y15	V13	457 ⁽³⁾
I/O	P88	P103	V14	U13	460 ⁽³⁾
I/O	P89	P104	W15	T13	463 ⁽³⁾

Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: Component Availability Chart for Spartan/XL FPGAs

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84 ⁽³⁾	VQ100 ⁽³⁾	CS144 ⁽³⁾	TQ144	PQ208	PQ240	BG256 ⁽³⁾	CS280 ⁽³⁾
XCS05	-3	C ⁽³⁾	C, I	-	-	-	-	-	-
	-4	C ⁽³⁾	C	-	-	-	-	-	-
XCS10	-3	C ⁽³⁾	C, I	-	C	-	-	-	-
	-4	C ⁽³⁾	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C ⁽³⁾	-	C, I	C, I	C	C ⁽³⁾	-
	-4	-	C ⁽³⁾	-	C	C	C	C ⁽³⁾	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C ⁽³⁾	C, I	-	-	-	-	-	-
	-5	C ⁽³⁾	C	-	-	-	-	-	-
XCS10XL	-4	C ⁽³⁾	C, I	C ⁽³⁾	C	-	-	-	-
	-5	C ⁽³⁾	C	C ⁽³⁾	C	-	-	-	-
XCS20XL	-4	-	C, I	C ⁽³⁾	C, I	C, I	-	-	-
	-5	-	C	C ⁽³⁾	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C ⁽³⁾
	-5	-	C	-	C	C	C	C	C ⁽³⁾
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C ⁽³⁾
	-5	-	-	-	-	C	C	C	C ⁽³⁾

6/25/08

Notes:

1. C = Commercial $T_J = 0^\circ$ to $+85^\circ\text{C}$
2. I = Industrial $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

www.xilinx.com/support/documentation/spartan-xl.htm#19687

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

www.xilinx.com/cgi-bin/thermal/thermal.pl

Table 20: User I/O Chart for Spartan/XL FPGAs

Device	Max I/O	Package Type							
		PC84 ⁽¹⁾	VQ100 ⁽¹⁾	CS144 ⁽¹⁾	TQ144	PQ208	PQ240	BG256 ⁽¹⁾	CS280 ⁽¹⁾
XCS05	80	61 ⁽¹⁾	77	-	-	-	-	-	-
XCS10	112	61 ⁽¹⁾	77	-	112	-	-	-	-
XCS20	160	-	77	-	113	160	-	-	-
XCS30	192	-	77 ⁽¹⁾	-	113	169	192	192 ⁽¹⁾	-
XCS40	224	-	-	-	-	169	192	205	-
XCS05XL	80	61 ⁽¹⁾	77 ⁽²⁾	-	-	-	-	-	-
XCS10XL	112	61 ⁽¹⁾	77 ⁽²⁾	112 ⁽¹⁾	112 ⁽²⁾	-	-	-	-
XCS20XL	160	-	77 ⁽²⁾	113 ⁽¹⁾	113 ⁽²⁾	160 ⁽²⁾	-	-	-
XCS30XL	192	-	77 ⁽²⁾	-	113 ⁽²⁾	169 ⁽²⁾	192 ⁽²⁾	192 ⁽²⁾	192 ⁽¹⁾
XCS40XL	224	-	-	-	-	169 ⁽²⁾	192 ⁽²⁾	205 ⁽²⁾	224 ⁽¹⁾

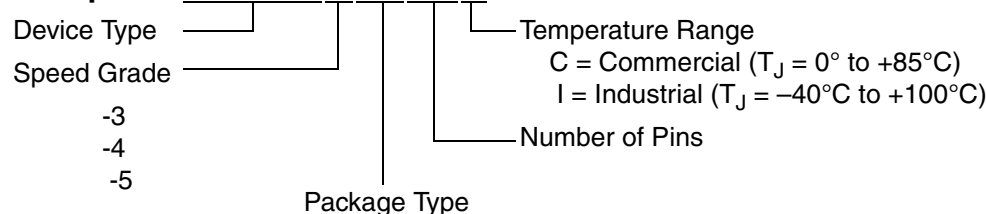
6/25/08

Notes:

1. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
2. These Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Ordering Information

Example: XCS20XL-4 PQ208C



BG = Ball Grid Array

BGG = Ball Grid Array (Pb-free)

PC = Plastic Lead Chip Carrier

PQ = Plastic Quad Flat Pack

PQG = Plastic Quad Flat Pack (Pb-free)

VQ = Very Thin Quad Flat Pack

VQG = Very Thin Quad Flat Pack (Pb-free)

TQ = Thin Quad Flat Pack

TQG = Thin Quad Flat Pack (Pb-free)

CS = Chip Scale