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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	950
Total RAM Bits	12800
Number of I/O	113
Number of Gates	20000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs20xl-5tq144c

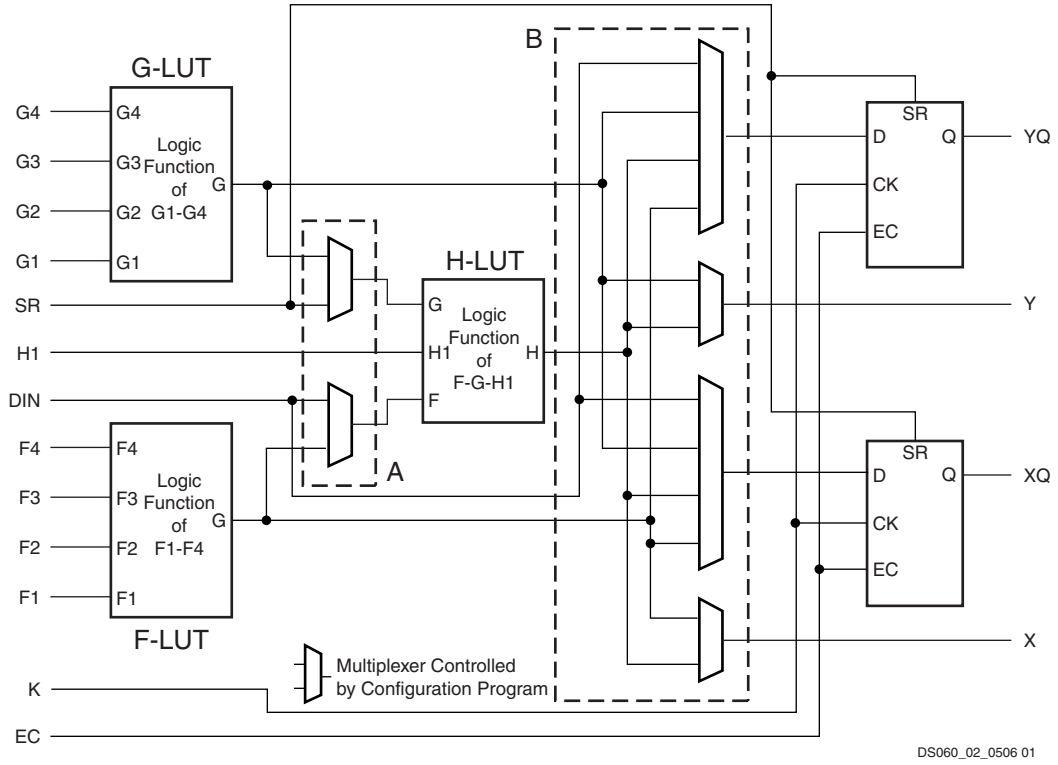


Figure 2: **Spartan/XL Simplified CLB Logic Diagram (some features not shown)**

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

  Note: When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.
- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.

Latches (Spartan-XL Family Only)

The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds, using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.

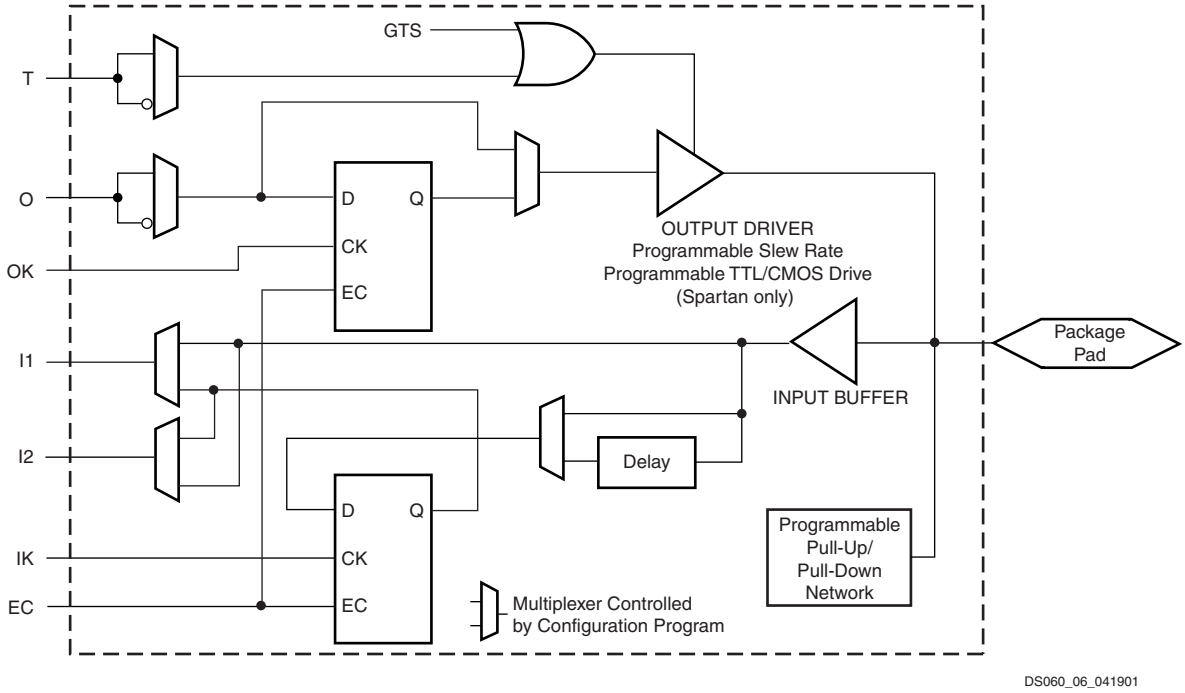


Figure 6: **Simplified Spartan/XL IOB Block Diagram**

This high value makes them unsuitable as wired-AND pull-up resistors.

Table 7: **Supported Destinations for Spartan/XL Outputs**

Destination	Spartan-XL Outputs	Spartan Outputs	
	3.3V, CMOS	5V, TTL	5V, CMOS
Any device, V_{CC} = 3.3V, CMOS-threshold inputs	√	√	Some(1)
Any device, V_{CC} = 5V, TTL-threshold inputs	√	√	√
Any device, V_{CC} = 5V, CMOS-threshold inputs	Unreliable Data		√

Notes:
1. Only if destination device has 5V tolerant inputs.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops (Figure 5). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (see EC signal in Figure 5), which through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan/XL FPGA CLB. It cannot be inverted within the IOB.

Routing Channel Description

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

This section describes the routing channels available in Spartan/XL devices. Figure 8 shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the designer should open a design in the FPGA Editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

CLB Routing Channels

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). Figure 8 shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.

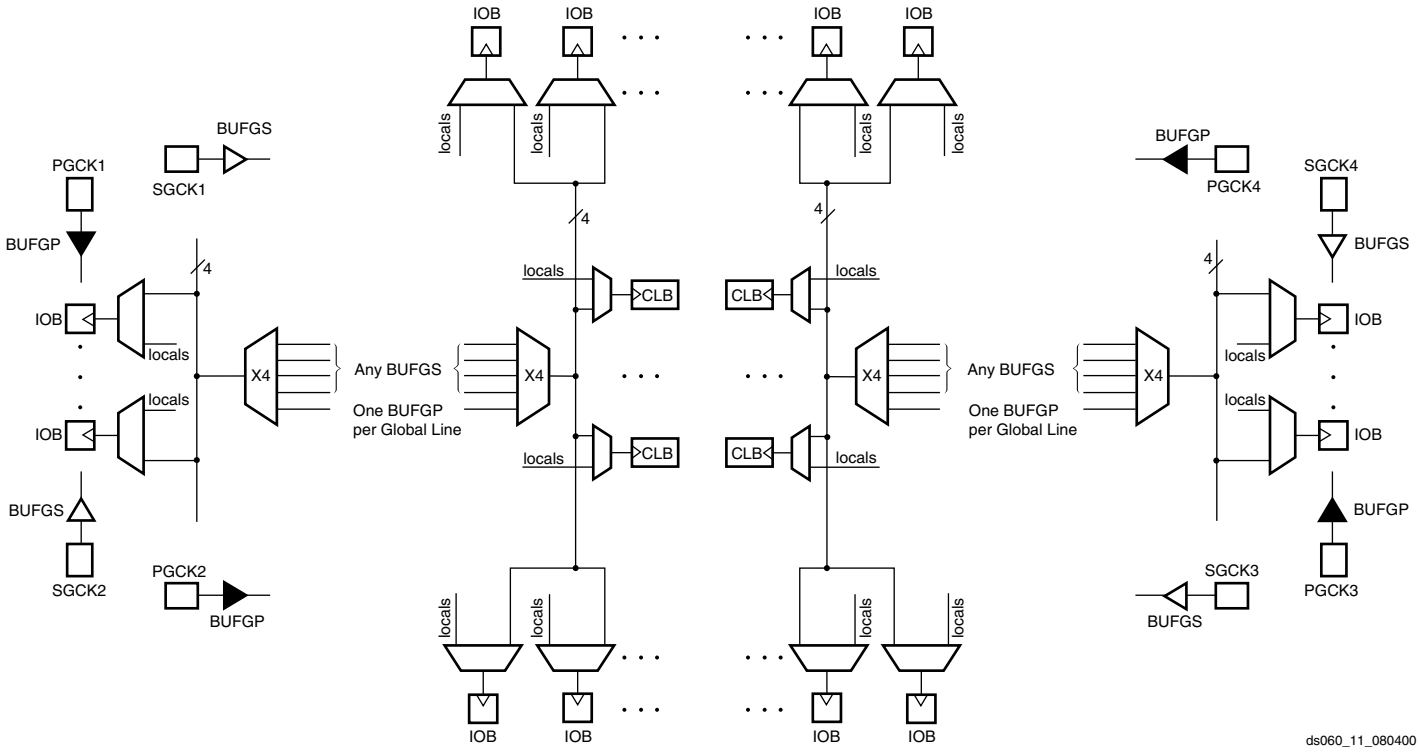


Figure 11: **5V Spartan Family Global Net Distribution**

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 8. Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 8: **CLB Memory Configurations**

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√	–	–

- The 16 x 1 single-port configuration contains a RAM array with 16 locations, each one-bit wide. One 4-bit address decoder determines the RAM location for write and read operations. There is one input for writing data and one output for reading data, all at the selected address.
- The (16 x 1) x 2 single-port configuration combines two 16 x 1 single-port configurations (each according to the preceding description). There is one data input, one data output and one address decoder for each array. These arrays can be addressed independently.
- The 32 x 1 single-port configuration contains a RAM array with 32 locations, each one-bit wide. There is one data input, one data output, and one 5-bit address decoder.
- The dual-port mode 16 x 1 configuration contains a RAM array with 16 locations, each one-bit wide. There are two 4-bit address decoders, one for each port. One port consists of an input for writing and an output for reading, all at a selected address. The other port consists of one output for reading from an independently selected address.

The appropriate choice of RAM configuration mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Selection criteria include the following: Whereas the 32 x 1 single-port, the (16 x 1) x 2 single-port, and the 16 x 1 dual-port configurations each use one entire CLB, the 16 x 1 single-port configuration uses only one half of a CLB. Due to its simultaneous read/write capability, the dual-port RAM can transfer twice as much data as the single-port RAM, which permits only one data operation at any given time.

CLB memory configuration options are selected by using the appropriate library symbol in the design entry.

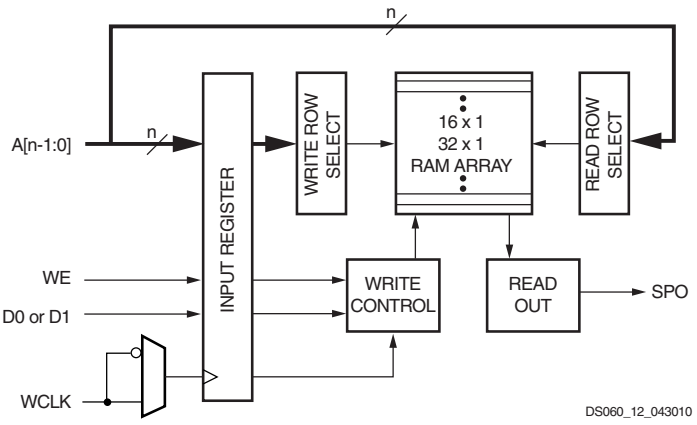
Single-Port Mode

There are three CLB memory configurations for the single-port RAM: 16 x 1, (16 x 1) x 2, and 32 x 1, the functional organization of which is shown in Figure 12.

The single-port RAM signals and the CLB signals (Figure 2, page 4) from which they are originally derived are shown in Table 9.

Table 9: **Single-Port RAM Signals**

RAM Signal	Function	CLB Signal
D0 or D1	Data In	DIN or H1
A[3:0]	Address	F[4:1] or G[4:1]
A4 (32 x 1 only)	Address	H1
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (Data Out)	F_{OUT} or G_{OUT}



Notes:
1. The (16 x 1) x 2 configuration combines two 16 x 1 single-port RAMs, each with its own independent address bus and data input. The same WE and WCLK signals are connected to both RAMs.
2. n = 4 for the 16 x 1 and (16 x 1) x 2 configurations. n = 5 for the 32 x 1 configuration.

Figure 12: **Logic Diagram for the Single-Port RAM**

Writing data to the single-port RAM is essentially the same as writing to a data register. It is an edge-triggered (synchronous) operation performed by applying an address to the A inputs and data to the D input during the active edge of WCLK while WE is High.

The timing relationships are shown in Figure 13. The High logic level on WE enables the input data register for writing. The active edge of WCLK latches the address, input data, and WE signals. Then, an internal write pulse is generated that loads the data into the memory cell.

CLB signals from which they are originally derived are shown in Table 10.

Table 10: **Dual-Port RAM Signals**

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F_{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G_{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: *"Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM,"* and *"Synchronous and Asynchronous FIFO Designs."* All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan

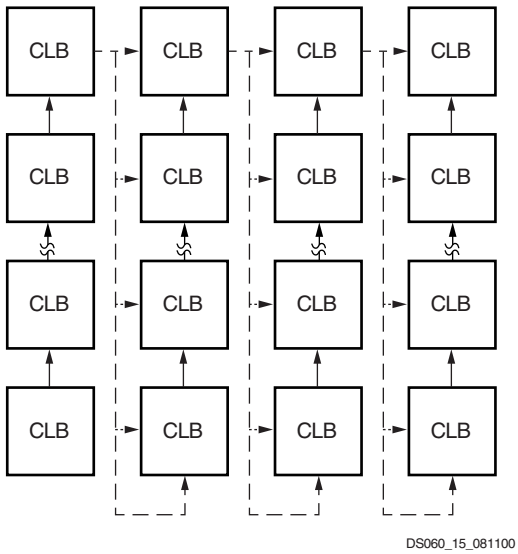


Figure 15: **Available Spartan/XL Carry Propagation Paths**

On-Chip Oscillator

Spartan/XL devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, V_{CC}, and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8-MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in Figure 3, page 5 for the CLB and Figure 5, page 6 for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 19.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

Global 3-State

A separate Global 3-state line (GTS) as shown in Figure 6, page 7 forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in Figure 19 for GSR except the IBUF would be connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-state signal. Alternatively, GTS can be driven from any internal node.

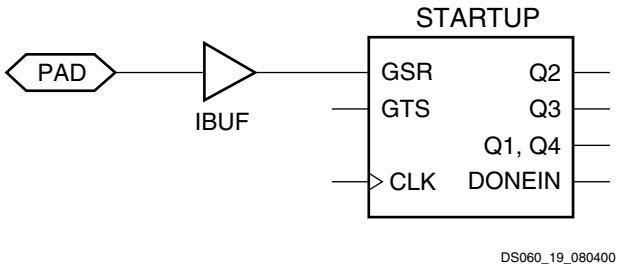


Figure 19: **Symbols for Global Set/Reset**

Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan compatible device. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan and Spartan-XL families implement IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Spartan/XL devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "*Boundary Scan in FPGA Devices*."

to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.

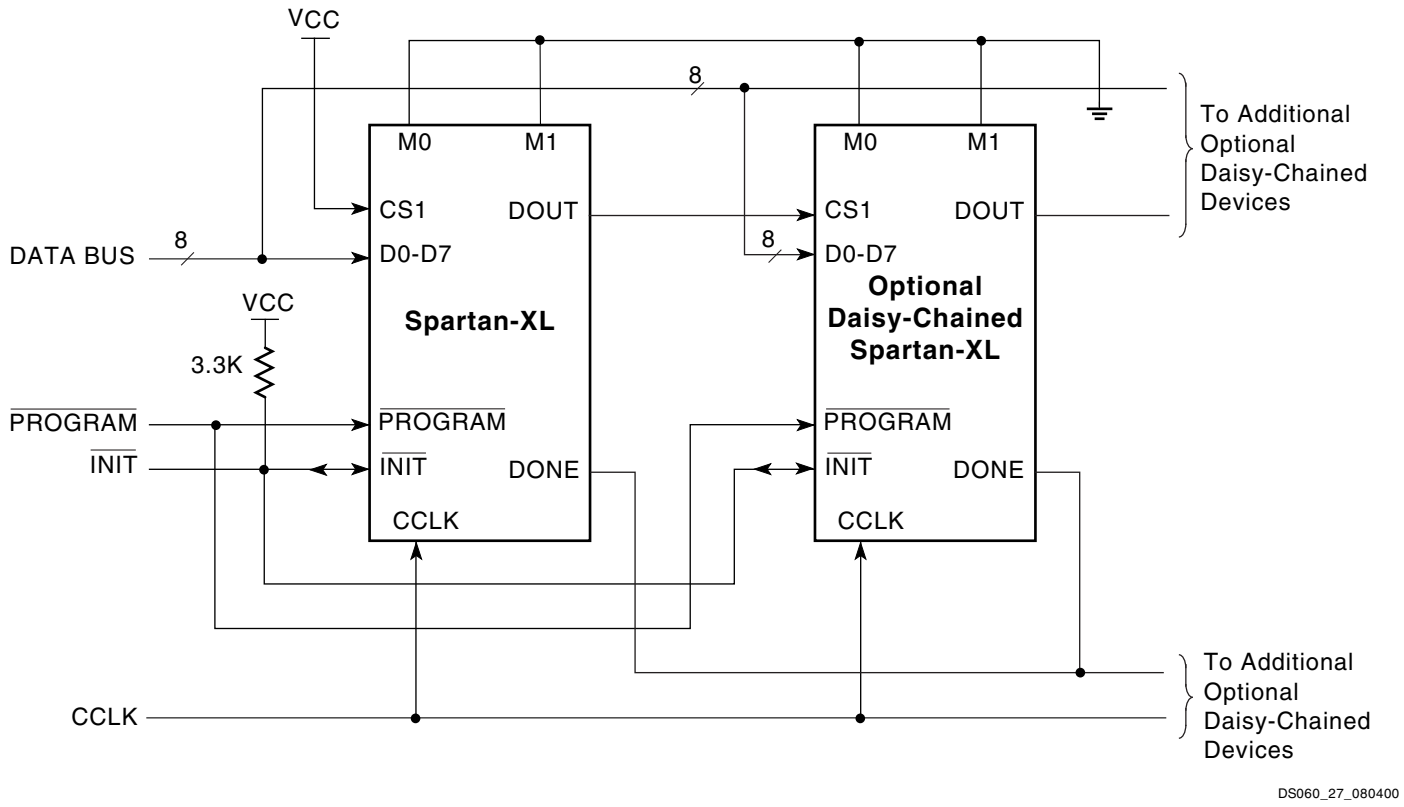


Figure 27: **Express Mode Circuit Diagram**

to wait after completing the configuration memory clear operation. When $\overline{INIT}$ is no longer held Low externally, the device determines its configuration mode by capturing the state of the Mode pins, and is ready to start the configuration process. A master device waits up to an additional 300 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{INIT}$ is High.

For more details on Configuration, refer to the Xilinx Application Note "FPGA Configuration Guidelines" (XAPP090).

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user system. Start-up must make sure that the user logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the Global Set/Reset (GSR) at the right time.

Start-Up Initiation

Two conditions have to be met in order for the start-up sequence to begin:

- The chip's internal memory must be full, and
- The configuration length count must be met, exactly.

In all configuration modes except Express mode, Spartan/XL devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

In Express mode, there is no length count. The start-up sequence for each device begins when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

Start-Up Events

The device can be programmed to control three start-up events.

- The release of the open-drain DONE output
- The termination of the Global Three-State and the change of configuration-related pins to the user function, activating all IOBs.
- The termination of the Global Set/Reset initialization of all CLB and IOB storage elements.

Figure 31 describes start-up timing in detail. The three events — DONE going High, the internal GSR being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. This relative timing is selected by options in the bitstream generation software. Heavy lines in Figure 31 show the default timing. The thin lines indicate all other possible timing options. The start-up logic must be clocked until the "F" (Finished) state is reached.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. GSR is then released another clock period later to make sure that user operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 31, but the designer can modify it to meet particular requirements.

Start-Up Clock

Normally, the start-up sequence is controlled by the internal device oscillator (CCLK), which is asynchronous to the system clock. As a configuration option, they can be triggered by an on-chip user net called UCLK. This user net can be accessed by placing the STARTUP library symbol, and the start-up modes are known as UCLK_NOSYNC or UCLK_SYNC. This allows the device to wake up in synchronism with the user system.

DONE Pin

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to the start-up control logic. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK_SYNC or UCLK_SYNC. When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK_NOSYNC or UCLK_NOSYNC. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, while the other configuration modes can use any of the four timing sequences.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

Spartan Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan Family Absolute Maximum Ratings(1)

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND(2,3)		–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output(2,3)		–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot (above V_{CC}) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = –40°C to +100°C(1)	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage(2)	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage(2)	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Spartan Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage @ I_{OH} = –1.0 mA, V_{CC} min	CMOS outputs	V_{CC} – 0.5	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min(1)	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		3.0	-	V
I_{CCO}	Quiescent FPGA supply current(2)	Commercial	-	3.0	mA
		Industrial	-	6.0	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)		-	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 5V (sample tested)		0.02	-	mA

Notes:
1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a Tie option.

Spartan Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
T_{PG}	From pad through Primary buffer, to any clock K	XCS05	2.0	4.0	ns
		XCS10	2.4	4.3	ns
		XCS20	2.8	5.4	ns
		XCS30	3.2	5.8	ns
		XCS40	3.5	6.4	ns
T_{SG}	From pad through Secondary buffer, to any clock K	XCS05	2.5	4.4	ns
		XCS10	2.9	4.7	ns
		XCS20	3.3	5.8	ns
		XCS30	3.6	6.2	ns
		XCS40	3.9	6.7	ns

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size[1]	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T_{WCTS}		32x1	8.0	-	11.6	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T_{WPTS}		32x1	4.0	-	5.8	-	ns
T_{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T_{ASTS}		32x1	1.5	-	2.0	-	ns
T_{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{AHTS}		32x1	0.0	-	0.0	-	ns
T_{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T_{DSTS}		32x1	1.5	-	1.7	-	ns
T_{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{DHTS}		32x1	0.0	-	0.0	-	ns
T_{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T_{WSTS}		32x1	1.5	-	1.6	-	ns
T_{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{WHTS}		32x1	0.0	-	0.0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T_{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T_{RCT}		32x1	3.8	-	3.8	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T_{IHO}		32x1	-	2.0	-	2.7	ns
T_{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T_{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:
1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Spartan Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
Global Primary Clock to TTL Output using OFF					
T_{ICKOF}	Fast	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
T_{ICKO}	Slew-rate limited	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
T_{ICKSOF}	Fast	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
T_{ICKSO}	Slew-rate limited	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
T_{CMOSOF}	Fast	All devices	0.8	1.0	ns
T_{CMOSO}	Slew-rate limited	All devices	1.5	2.0	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column,and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 34.
3. OFF = Output Flip-Flop

Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Min	Min	
Input Setup/Hold Times Using Primary Clock and IFF					
T_{PSUF}/T_{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T_{PSU}/T_{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T_{SSUF}/T_{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T_{SSU}/T_{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:

1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Propagation Delays							
T_{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.2	-	3.7	ns
T_{OPF}	Output (O) to Pad, fast	All devices	-	2.5	-	2.9	ns
T_{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	2.8	-	3.3	ns
T_{TSONF}	3-state to Pad active and valid, fast	All devices	-	2.6	-	3.0	ns
T_{OFPF}	Output (O) to Pad via Output MUX, fast	All devices	-	3.7	-	4.4	ns
T_{OKFPF}	Select (OK) to Pad via Output MUX, fast	All devices	-	3.3	-	3.9	ns
T_{SLOW}	For Output SLOW option add	All devices	-	1.5	-	1.7	ns
Setup and Hold Times							
T_{OOK}	Output (O) to clock (OK) setup time	All devices	0.5	-	0.5	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T_{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	0.0	-	0.0	-	ns
T_{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.1	-	0.2	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T_{RPO}	Delay from GSR input to any Pad	XCS05XL	-	11.9	-	14.0	ns
		XCS10XL	-	12.4	-	14.5	ns
		XCS20XL	-	12.9	-	15.0	ns
		XCS30XL	-	13.9	-	16.0	ns
		XCS40XL	-	14.9	-	17.0	ns

Notes:

1. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
VCC	P33	P25	N1	P37	-
Not Connect-ed[1] PWRDWN[2]	P34	P26	N2	P38	174 [1]
I/O, PGCK2[1] GCK3[2]	P35	P27	M3	P39	175[3]
I/O (HDC)	P36	P28	N3	P40	178 [3]
I/O	-	-	K4	P41	181 [3]
I/O	-	-	L4	P42	184 [3]
I/O	-	P29	M4	P43	187 [3]
I/O ($\overline{LDC}$)	P37	P30	N4	P44	190 [3]
GND	-	-	K5	P45	-
I/O	-	-	L5	P46	193 [3]
I/O	-	-	M5	P47	196 [3]
I/O	P38	P31	N5	P48	199 [3]
I/O	P39	P32	K6	P49	202 [3]
I/O	-	P33	L6	P50	205 [3]
I/O	-	P34	M6	P51	208 [3]
I/O	P40	P35	N6	P52	211 [3]
I/O ($\overline{INIT}$)	P41	P36	M7	P53	214 [3]
VCC	P42	P37	N7	P54	-
GND	P43	P38	L7	P55	-
I/O	P44	P39	K7	P56	217 [3]
I/O	P45	P40	N8	P57	220 [3]
I/O	-	P41	M8	P58	223 [3]
I/O	-	P42	L8	P59	226 [3]
I/O	P46	P43	K8	P60	229 [3]
I/O	P47	P44	N9	P61	232 [3]
I/O	-	-	M9	P62	235 [3]
I/O	-	-	L9	P63	238 [3]
GND	-	-	K9	P64	-
I/O	P48	P45	N10	P65	241 [3]
I/O	P49	P46	M10	P66	244 [3]
I/O	-	-	L10	P67	247 [3]
I/O	-	-	N11	P68	250 [3]
I/O	P50	P47	M11	P69	253 [3]
I/O, SGCK3[1] GCK4[2]	P51	P48	L11	P70	256 [3]
GND	P52	P49	N12	P71	-
DONE	P53	P50	M12	P72	-
VCC	P54	P51	N13	P73	-
$\overline{PROGRAM}$	P55	P52	M13	P74	-
I/O (D7[2])	P56	P53	L12	P75	259 [3]

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O, PGCK3[1] GCK5[2]	P57	P54	L13	P76	262 [3]
I/O	-	-	K10	P77	265 [3]
I/O	-	-	K11	P78	268 [3]
I/O (D6[2])	P58	P55	K12	P79	271 [3]
I/O	-	P56	K13	P80	274 [3]
GND	-	-	J10	P81	-
I/O	-	-	J11	P82	277 [3]
I/O	-	-	J12	P83	280 [3]
I/O (D5[2])	P59	P57	J13	P84	283 [3]
I/O	P60	P58	H10	P85	286 [3]
I/O	-	P59	H11	P86	289 [3]
I/O	-	P60	H12	P87	292 [3]
I/O (D4[2])	P61	P61	H13	P88	295 [3]
I/O	P62	P62	G12	P89	298 [3]
VCC	P63	P63	G13	P90	-
GND	P64	P64	G11	P91	-
I/O (D3[2])	P65	P65	G10	P92	301 [3]
I/O	P66	P66	F13	P93	304 [3]
I/O	-	P67	F12	P94	307 [3]
I/O	-	-	F11	P95	310 [3]
I/O (D2[2])	P67	P68	F10	P96	313 [3]
I/O	P68	P69	E13	P97	316 [3]
I/O	-	-	E12	P98	319 [3]
I/O	-	-	E11	P99	322 [3]
GND	-	-	E10	P100	-
I/O (D1[2])	P69	P70	D13	P101	325 [3]
I/O	P70	P71	D12	P102	328 [3]
I/O	-	-	D11	P103	331 [3]
I/O	-	-	C13	P104	334 [3]
I/O (D0[2], DIN)	P71	P72	C12	P105	337 [3]
I/O, SGCK4[1] GCK6[2] (DOUT)	P72	P73	C11	P106	340 [3]
CCLK	P73	P74	B13	P107	-
VCC	P74	P75	B12	P108	-
O, TDO	P75	P76	A13	P109	0
GND	P76	P77	A12	P110	-
I/O	P77	P78	B11	P111	2
I/O, PGCK4[1] GCK7[2]	P78	P79	A11	P112	5
I/O	-	-	D10	P113	8
I/O	-	-	C10	P114	11
I/O (CS1[2])	P79	P80	B10	P115	14

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC[2]	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2[1], GCK2[2]	P21	L2	P33	P49	239
Not Connected[1] M1[2]	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE[1], M0[2]	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected[1] $\overline{\text{PWRDWN}}$[2]	P26	N2	P38	P54	246 [1]
I/O, PGCK2[1], GCK3[2]	P27	M3	P39	P55	247 [3]
I/O (HDC)	P28	N3	P40	P56	250 [3]
I/O	-	K4	P41	P57	253 [3]
I/O	-	L4	P42	P58	256 [3]
I/O	P29	M4	P43	P59	259 [3]

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O ($\overline{\text{LDC}}$)	P30	N4	P44	P60	262 [3]
I/O	-	-	-	P61	265 [3]
I/O	-	-	-	P62	268 [3]
I/O	-	-	-	P63	271 [3]
I/O	-	-	-	P64	274 [3]
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 [3]
I/O	-	M5	P47	P68	280 [3]
I/O	P31	N5	P48	P69	283 [3]
I/O	P32	K6	P49	P70	286 [3]
VCC[2]	-	-	-	P71	-
I/O	-	-	-	P72	289 [3]
I/O	-	-	-	P73	292 [3]
I/O	P33	L6	P50	P74	295 [3]
I/O	P34	M6	P51	P75	298 [3]
I/O	P35	N6	P52	P76	301 [3]
I/O ($\overline{\text{INIT}}$)	P36	M7	P53	P77	304 [3]
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 [3]
I/O	P40	N8	P57	P81	310 [3]
I/O	P41	M8	P58	P82	313 [3]
I/O	P42	L8	P59	P83	316 [3]
I/O	-	-	-	P84	319 [3]
I/O	-	-	-	P85	322 [3]
VCC[2]	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 [3]
I/O	P44	N9	P61	P88	328 [3]
I/O	-	M9	P62	P89	331 [3]
I/O	-	L9	P63	P90	334 [3]
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 [3]
I/O	-	-	-	P94	340 [3]
I/O	-	-	-	P95	343 [3]
I/O	-	-	-	P96	346 [3]
I/O	P45	N10	P65	P97	349 [3]
I/O	P46	M10	P66	P98	352 [3]
I/O	-	L10	P67	P99	355 [3]
I/O	-	N11	P68	P100	358 [3]
I/O	P47	M11	P69	P101	361 [3]
I/O, SGCK3[1], GCK4[2]	P48	L11	P70	P102	364 [3]
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	-	P85	P97	U12	T11	382 [3]
I/O	-	-	-	P99	V13	U12	385 [3]
I/O	-	-	-	P100	Y14	T12	388 [3]
VCC	-	-	P86	P101	VCC[4]	W13	-
I/O	P43	P60	P87	P102	Y15	V13	391 [3]
I/O	P44	P61	P88	P103	V14	U13	394 [3]
I/O	-	P62	P89	P104	W15	T13	397 [3]
I/O	-	P63	P90	P105	Y16	W14	400 [3]
GND	-	P64	P91	P106	GND[4]	GND[4]	-
I/O	-	-	-	P107	V15	V14	403 [3]
I/O	-	-	P92	P108	W16	U14	406 [3]
I/O	-	-	P93	P109	Y17	T14	409 [3]
I/O	-	-	P94	P110	V16	R14	412 [3]
I/O	-	-	P95	P111	W17	W15	415 [3]
I/O	-	-	P96	P112	Y18	U15	418 [3]
I/O	P45	P65	P97	P113	U16	V16	421 [3]
I/O	P46	P66	P98	P114	V17	U16	424 [3]
I/O	-	P67	P99	P115	W18	W17	427 [3]
I/O	-	P68	P100	P116	Y19	W18	430 [3]
I/O	P47	P69	P101	P117	V18	V17	433 [3]
I/O, SGCK3[1], GCK4[2]	P48	P70	P102	P118	W19	V18	436 [3]
GND	P49	P71	P103	P119	GND[4]	GND[4]	-
DONE	P50	P72	P104	P120	Y20	W19	-
VCC	P51	P73	P105	P121	VCC[4]	U17	-
$\overline{\text{PROGRAM}}$	P52	P74	P106	P122	V19	U18	-
I/O (D7[2])	P53	P75	P107	P123	U19	V19	439 [3]
I/O, PGCK3[1], GCK5[2]	P54	P76	P108	P124	U18	U19	442 [3]
I/O	-	P77	P109	P125	T17	T16	445 [3]
I/O	-	P78	P110	P126	V20	T17	448 [3]
I/O	-	-	-	P127	U20	T18	451 [3]
I/O	-	-	P111	P128	T18	T19	454 [3]
I/O (D6[2])	P55	P79	P112	P129	T19	R16	457 [3]
I/O	P56	P80	P113	P130	T20	R19	460 [3]
I/O	-	-	P114	P131	R18	P15	463 [3]
I/O	-	-	P115	P132	R19	P17	466 [3]
I/O	-	-	P116	P133	R20	P18	469 [3]
I/O	-	-	P117	P134	P18	P16	472 [3]
GND	-	P81	P118	P135	GND[4]	GND[4]	-
I/O	-	-	-	P136	P20	P19	475 [3]
I/O	-	-	-	P137	N18	N17	478 [3]
I/O	-	P82	P119	P138	N19	N18	481 [3]
I/O	-	P83	P120	P139	N20	N19	484 [3]
VCC	-	-	P121	P140	VCC[4]	N16	-
I/O (D5[2])	P57	P84	P122	P141	M17	M19	487 [3]
I/O	P58	P85	P123	P142	M18	M17	490 [3]

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	P90	P105	Y16	W14	466 (3)
GND	P91	P106	GND(4)	GND(4)	-
I/O	-	P107	V15	V14	469 (3)
I/O	P92	P108	W16	U14	472 (3)
I/O	P93	P109	Y17	T14	475 (3)
I/O	P94	P110	V16	R14	478 (3)
I/O	P95	P111	W17	W15	481 (3)
I/O	P96	P112	Y18	U15	484 (3)
I/O	-	-	-	T15	487 (3)
I/O	-	-	-	W16	490 (3)
I/O	P97	P113	U16	V16	493 (3)
I/O	P98	P114	V17	U16	496 (3)
I/O	P99	P115	W18	W17	499 (3)
I/O	P100	P116	Y19	W18	502 (3)
I/O	P101	P117	V18	V17	505 (3)
I/O, SGCK3(1), GCK4(2)	P102	P118	W19	V18	508 (3)
GND	P103	P119	GND(4)	GND(4)	-
DONE	P104	P120	Y20	W19	-
VCC	P105	P121	VCC(4)	VCC(4)	-
$\overline{\text{PROGRAM}}$	P106	P122	V19	U18	-
I/O (D7(2))	P107	P123	U19	V19	511 (3)
I/O, PGCK3(1), GCK5(2)	P108	P124	U18	U19	514 (3)
I/O	P109	P125	T17	T16	517 (3)
I/O	P110	P126	V20	T17	520 (3)
I/O	-	P127	U20	T18	523 (3)
I/O	P111	P128	T18	T19	526 (3)
I/O	-	-	-	R15	529 (3)
I/O	-	-	-	R17	523 (3)
I/O (D6(2))	P112	P129	T19	R16	535 (3)
I/O	P113	P130	T20	R19	538 (3)
I/O	P114	P131	R18	P15	541 (3)
I/O	P115	P132	R19	P17	544 (3)
I/O	P116	P133	R20	P18	547 (3)
I/O	P117	P134	P18	P16	550 (3)
GND	P118	P135	GND(4)	GND(4)	-
I/O	-	P136	P20	P19	553 (3)
I/O	-	P137	N18	N17	556 (3)
I/O	P119	P138	N19	N18	559 (3)
I/O	P120	P139	N20	N19	562 (3)
VCC	P121	P140	VCC(4)	VCC(4)	-
I/O (D5(2))	P122	P141	M17	M19	565 (3)
I/O	P123	P142	M18	M17	568 (3)

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	-	-	-	M18	571 (3)
I/O	-	-	M19	M16	574 (3)
I/O	P124	P144	M20	L19	577 (3)
I/O	P125	P145	L19	L18	580 (3)
I/O	P126	P146	L18	L17	583 (3)
I/O	P127	P147	L20	L16	586 (3)
I/O (D4(2))	P128	P148	K20	K19	589 (3)
I/O	P129	P149	K19	K18	592 (3)
VCC	P130	P150	VCC(4)	VCC(4)	-
GND	P131	P151	GND(4)	GND(4)	-
I/O (D3(2))	P132	P152	K18	K16	595 (3)
I/O	P133	P153	K17	K15	598 (3)
I/O	P134	P154	J20	J19	601 (3)
I/O	P135	P155	J19	J18	604 (3)
I/O	P136	P156	J18	J17	607 (3)
I/O	P137	P157	J17	J16	610 (3)
I/O	-	-	H20	H19	613 (3)
I/O	-	-	-	H18	616 (3)
I/O (D2(2))	P138	P159	H19	H17	619 (3)
I/O	P139	P160	H18	H16	622 (3)
VCC	P140	P161	VCC(4)	VCC(4)	-
I/O	P141	P162	G19	G18	625 (3)
I/O	P142	P163	F20	G17	628 (3)
I/O	-	P164	G18	G16	631 (3)
I/O	-	P165	F19	F19	634 (3)
GND	P143	P166	GND(4)	GND(4)	-
I/O	-	P167	F18	F18	637 (3)
I/O	P144	P168	E19	F17	640 (3)
I/O	P145	P169	D20	F16	643 (3)
I/O	P146	P170	E18	F15	646 (3)
I/O	P147	P171	D19	E19	649 (3)
I/O	P148	P172	C20	E17	652 (3)
I/O (D1(2))	P149	P173	E17	E16	655 (3)
I/O	P150	P174	D18	D19	658 (3)
I/O	-	-	-	D18	661 (3)
I/O	-	-	-	D17	664 (3)
I/O	P151	P175	C19	C19	667 (3)
I/O	P152	P176	B20	B19	670 (3)
I/O (D0(2), DIN)	P153	P177	C18	C18	673 (3)
I/O, SGCK4(1), GCK6(2) (DOUT)	P154	P178	B19	B18	676 (3)
CCLK	P155	P179	A20	A19	-
VCC	P156	P180	VCC(4)	VCC(4)	-

Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: **Component Availability Chart for Spartan/XL FPGAs**

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84(3)	VQ100(3)	CS144(3)	TQ144	PQ208	PQ240	BG256(3)	CS280(3)
XCS05	-3	C(3)	C, I	-	-	-	-	-	-
	-4	C(3)	C	-	-	-	-	-	-
XCS10	-3	C(3)	C, I	-	C	-	-	-	-
	-4	C(3)	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C(3)	-	C, I	C, I	C	C(3)	-
	-4	-	C(3)	-	C	C	C	C(3)	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C(3)	C, I	-	-	-	-	-	-
	-5	C(3)	C	-	-	-	-	-	-
XCS10XL	-4	C(3)	C, I	C(3)	C	-	-	-	-
	-5	C(3)	C	C(3)	C	-	-	-	-
XCS20XL	-4	-	C, I	C(3)	C, I	C, I	-	-	-
	-5	-	C	C(3)	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C(3)
	-5	-	C	-	C	C	C	C	C(3)
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C(3)
	-5	-	-	-	-	C	C	C	C(3)

6/25/08

Notes:

1. C = Commercial T_J = 0° to +85°C
2. I = Industrial T_J = –40°C to +100°C
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

www.xilinx.com/support/documentation/spartan-xl.htm#19687

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

www.xilinx.com/cgi-bin/thermal/thermal.pl