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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	400
Number of Logic Elements/Cells	950
Total RAM Bits	12800
Number of I/O	77
Number of Gates	20000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs20xl-5vq100c

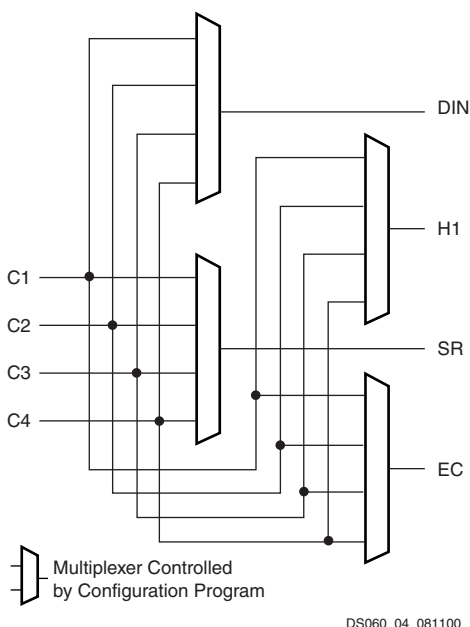


Figure 4: CLB Control Signal Interface

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

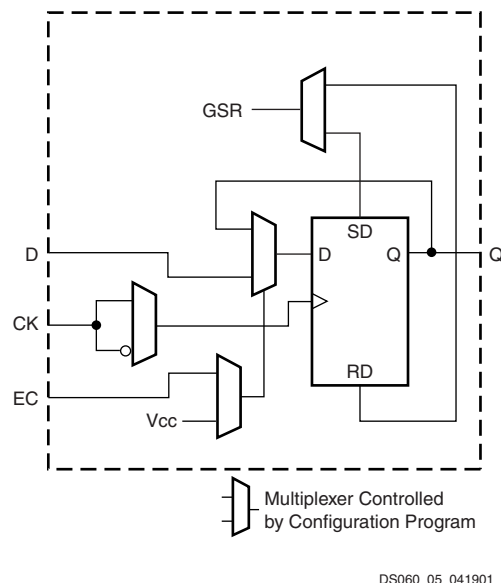


Figure 5: IOB Flip-Flop/Latch Functional Block Diagram

IOB Input Signal Path

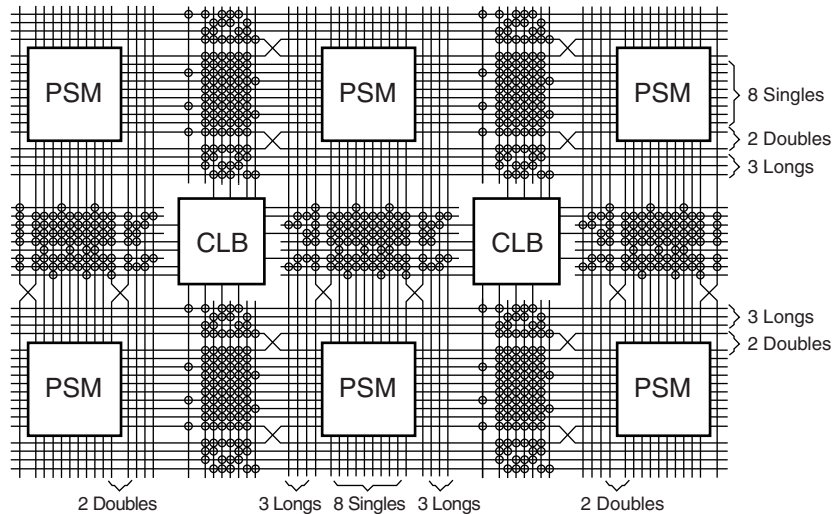
The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: Input Register Functionality

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop		1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

- X Don't care.
- Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0* Input is Low or unconnected (default value)
- 1* Input is High or unconnected (default value)

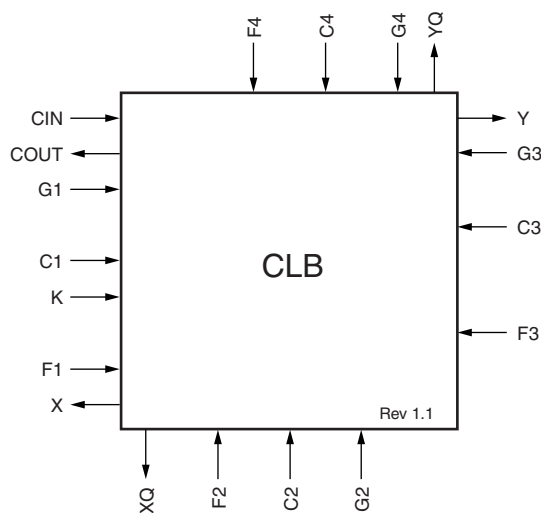


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Figure 8: Spartan/XL CLB Routing Channels and Interface Block Diagram

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.



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Figure 9: CLB Interconnect Signals

Programmable Switch Matrices

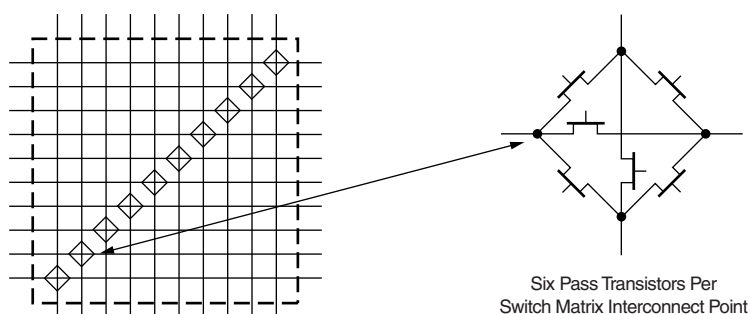
The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs. Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.



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Figure 10: Programmable Switch Matrix

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 8).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 8. The longlines also interface to some 3-state buffers which is described later in **3-State Long Line Drivers**, page 19.

I/O Routing

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 11. In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.

CLB signals from which they are originally derived are shown in Table 10.

Table 10: Dual-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F _{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G _{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

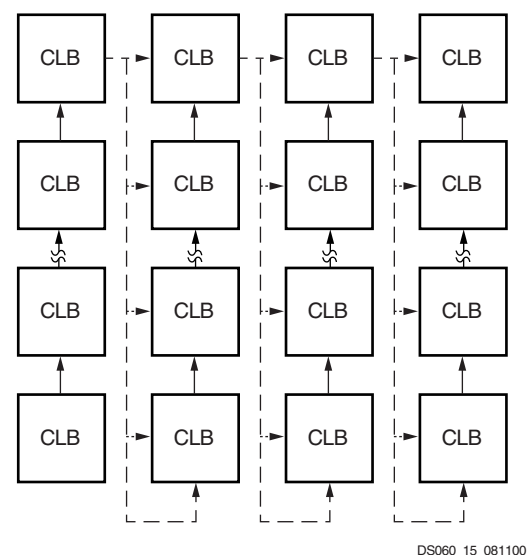
Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in micro-processor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan



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Figure 15: Available Spartan/XL Carry Propagation Paths

On-Chip Oscillator

Spartan/XL devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, V_{CC} , and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8-MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in [Figure 3, page 5](#) for the CLB and [Figure 5, page 6](#) for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

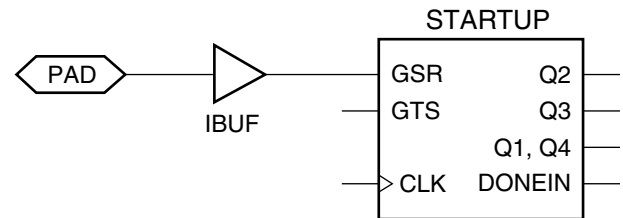
GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See [Figure 19.](#)) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

Global 3-State

A separate Global 3-state line (GTS) as shown in [Figure 6, page 7](#) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in [Figure 19](#) for GSR except the IBUF would be

connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-state signal. Alternatively, GTS can be driven from any internal node.



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Figure 19: Symbols for Global Set/Reset

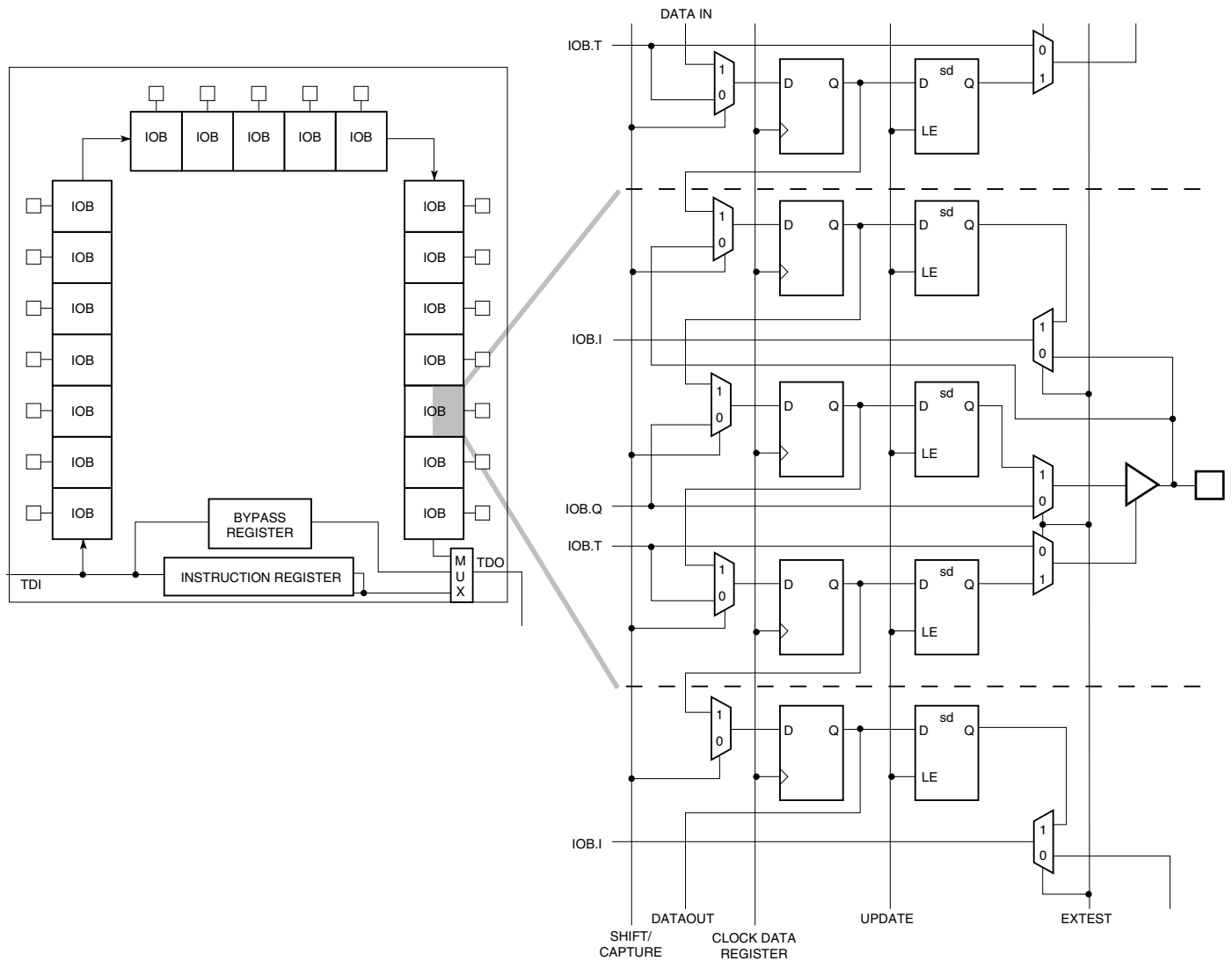
Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan compatible device. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan and Spartan-XL families implement IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Spartan/XL devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "Boundary Scan in FPGA Devices."



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Figure 20: Spartan/XL Boundary Scan Logic

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

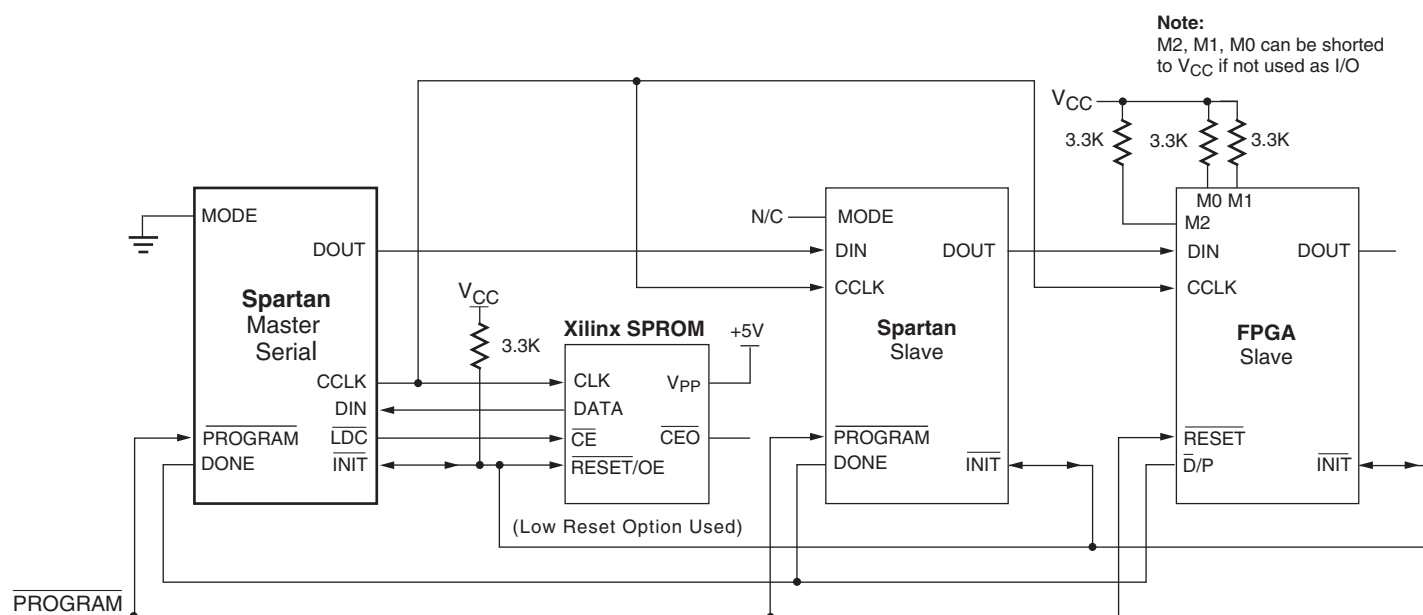
Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through

and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

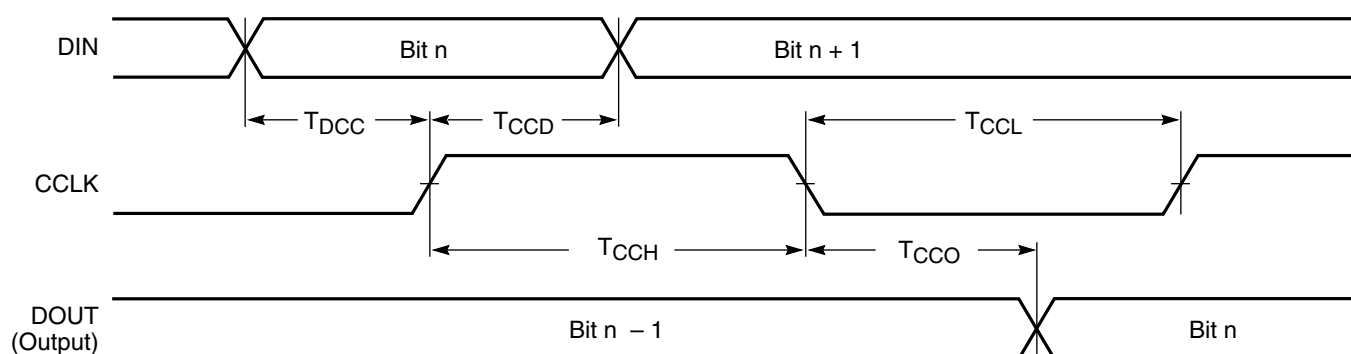
After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.



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Figure 25: Master/Slave Serial Mode Circuit Diagram



DS060_26_080400

Symbol		Description	Min	Max	Units
T_{DCC}	CCLK	DIN setup	20	-	ns
T_{CCD}		DIN hold	0	-	ns
T_{CCO}		DIN to DOUT	-	30	ns
T_{CCH}		High time	40	-	ns
T_{CCL}		Low time	40	-	ns
F_{CC}		Frequency	-	12.5	MHz

Notes:

1. Configuration must be delayed until the \overline{INIT} pins of all daisy-chained FPGAs are High.

Figure 26: Slave Serial Mode Programming Switching Characteristics

Express Mode (Spartan-XL Family Only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

Pseudo Daisy Chain

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices

are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be

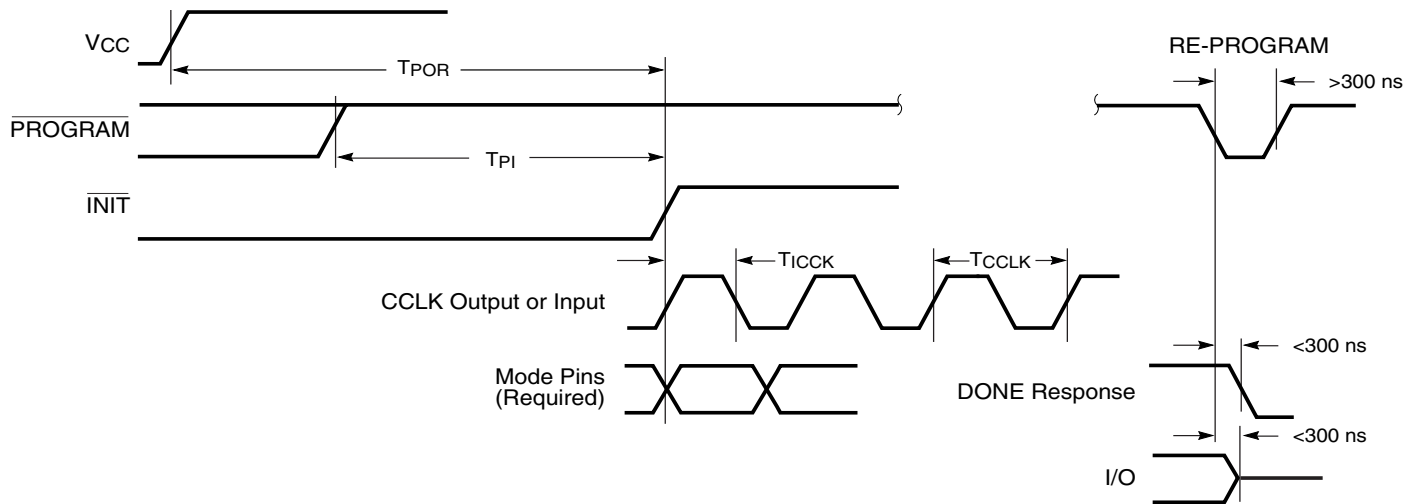
met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in [Table 16](#) and [Table 17](#).

Configuration Switching Characteristics



DS060_33_080400

Master Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	40	130	ms
T_{PI}	Program Latency	30	200	μ s per CLB column
T_{ICCK}	CCLK (output) delay	40	250	μ s
T_{CCLK}	CCLK (output) period, slow	640	2000	ns
T_{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	10	33	ms
T_{PI}	Program latency	30	200	μ s per CLB column
T_{ICCK}	CCLK (input) delay (required)	4	-	μ s
T_{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan Family Absolute Maximum Ratings⁽¹⁾

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND ^(2,3)		-0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output ^(2,3)		-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- Maximum DC overshoot (above V_{CC}) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to -2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Spartan Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	4.75	5.25	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ ⁽¹⁾	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage ⁽²⁾	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage ⁽²⁾	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:

- At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-4		-3		
		Min	Max	Min	Max	
Clocks						
T _{CH}	Clock High time	3.0	-	4.0	-	ns
T _{CL}	Clock Low time	3.0	-	4.0	-	ns
Combinatorial Delays						
T _{ILO}	F/G inputs to X/Y outputs	-	1.2	-	1.6	ns
T _{IHO}	F/G inputs via H to X/Y outputs	-	2.0	-	2.7	ns
T _{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.7	-	2.2	ns
CLB Fast Carry Logic						
T _{OPCY}	Operand inputs (F1, F2, G1, G4) to C _{OUT}	-	1.7	-	2.1	ns
T _{ASCY}	Add/Subtract input (F3) to C _{OUT}	-	2.8	-	3.7	ns
T _{INCY}	Initialization inputs (F1, F3) to C _{OUT}	-	1.2	-	1.4	ns
T _{SUM}	C _{IN} through function generators to X/Y outputs	-	2.0	-	2.6	ns
T _{BYP}	C _{IN} to C _{OUT} , bypass function generators	-	0.5	-	0.6	ns
Sequential Delays						
T _{CKO}	Clock K to Flip-Flop outputs Q	-	2.1	-	2.8	ns
Setup Time before Clock K						
T _{ICK}	F/G inputs	1.8	-	2.4	-	ns
T _{IHCK}	F/G inputs via H	2.9	-	3.9	-	ns
T _{HH1CK}	C inputs via H1 through H	2.3	-	3.3	-	ns
T _{DICK}	C inputs via DIN	1.3	-	2.0	-	ns
T _{ECKK}	C inputs via EC	2.0	-	2.6	-	ns
T _{RCK}	C inputs via S/R, going Low (inactive)	2.5	-	4.0	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T _{RPW}	Width (High)	3.0	-	4.0	-	ns
T _{RIO}	Delay from C inputs via S/R, going High to Q	-	3.0	-	4.0	ns
Global Set/Reset						
T _{MRW}	Minimum GSR pulse width	11.5	-	13.5	-	ns
T _{MRQ}	Delay from GSR input to any Q	See page 50 for T _{RRI} values per device.				
F _{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	166	-	125	MHz

Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Min	Min	
Input Setup/Hold Times Using Primary Clock and IFF					
T _{PSUF} /T _{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T _{PSU} /T _{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T _{SSUF} /T _{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T _{SSU} /T _{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:

1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

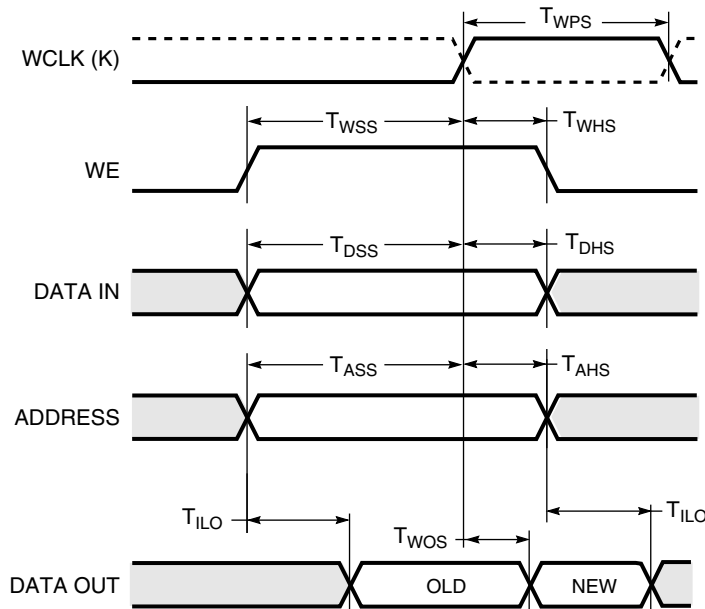
Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation ⁽¹⁾							
T _{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T _{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T _{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T _{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T _{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T _{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

Notes:

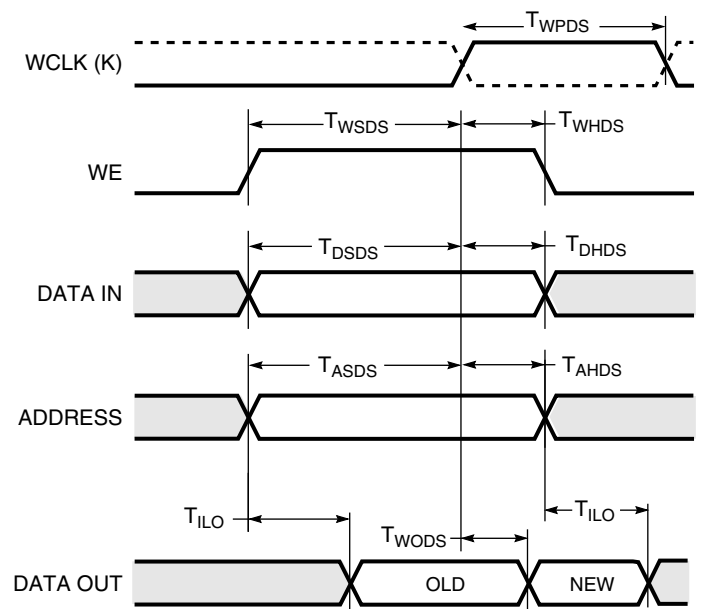
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



DS060_34_011300

Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Setup and Hold

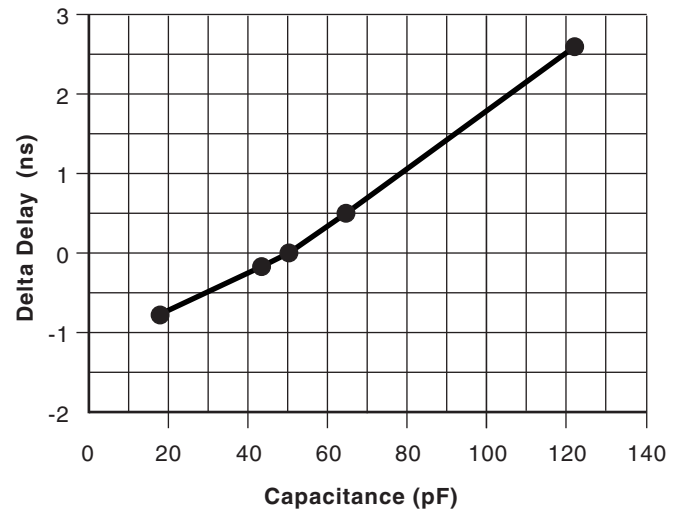
Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Input Setup/Hold Times Using Global Clock and IFF					
T _{SUF} /T _{HF}	No Delay	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
T _{SU} /T _H	Full Delay	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



DS060_35_080400

Figure 35: Delay Factor at Various Capacitive Loads

Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to

the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Propagation Delays							
T _{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.2	-	3.7	ns
T _{OPF}	Output (O) to Pad, fast	All devices	-	2.5	-	2.9	ns
T _{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	2.8	-	3.3	ns
T _{TSONF}	3-state to Pad active and valid, fast	All devices	-	2.6	-	3.0	ns
T _{OFFPF}	Output (O) to Pad via Output MUX, fast	All devices	-	3.7	-	4.4	ns
T _{OKFPF}	Select (OK) to Pad via Output MUX, fast	All devices	-	3.3	-	3.9	ns
T _{SLOW}	For Output SLOW option add	All devices	-	1.5	-	1.7	ns
Setup and Hold Times							
T _{OOK}	Output (O) to clock (OK) setup time	All devices	0.5	-	0.5	-	ns
T _{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T _{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	0.0	-	0.0	-	ns
T _{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.1	-	0.2	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T _{RPO}	Delay from GSR input to any Pad	XCS05XL	-	11.9	-	14.0	ns
		XCS10XL	-	12.4	-	14.5	ns
		XCS20XL	-	12.9	-	15.0	ns
		XCS30XL	-	13.9	-	16.0	ns
		XCS40XL	-	14.9	-	17.0	ns

Notes:

- Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
- Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84 ⁽⁴⁾	VQ100	CS144 ^(2,4)	TQ144	Bndry Scan
VCC	P33	P25	N1	P37	-
Not Connect-ed ⁽¹⁾	P34	P26	N2	P38	174 ⁽¹⁾
PWRDWN ⁽²⁾					
I/O, PGCK2 ⁽¹⁾ GCK3 ⁽²⁾	P35	P27	M3	P39	175 ⁽³⁾
I/O (HDC)	P36	P28	N3	P40	178 ⁽³⁾
I/O	-	-	K4	P41	181 ⁽³⁾
I/O	-	-	L4	P42	184 ⁽³⁾
I/O	-	P29	M4	P43	187 ⁽³⁾
I/O (LDC)	P37	P30	N4	P44	190 ⁽³⁾
GND	-	-	K5	P45	-
I/O	-	-	L5	P46	193 ⁽³⁾
I/O	-	-	M5	P47	196 ⁽³⁾
I/O	P38	P31	N5	P48	199 ⁽³⁾
I/O	P39	P32	K6	P49	202 ⁽³⁾
I/O	-	P33	L6	P50	205 ⁽³⁾
I/O	-	P34	M6	P51	208 ⁽³⁾
I/O	P40	P35	N6	P52	211 ⁽³⁾
I/O (INIT)	P41	P36	M7	P53	214 ⁽³⁾
VCC	P42	P37	N7	P54	-
GND	P43	P38	L7	P55	-
I/O	P44	P39	K7	P56	217 ⁽³⁾
I/O	P45	P40	N8	P57	220 ⁽³⁾
I/O	-	P41	M8	P58	223 ⁽³⁾
I/O	-	P42	L8	P59	226 ⁽³⁾
I/O	P46	P43	K8	P60	229 ⁽³⁾
I/O	P47	P44	N9	P61	232 ⁽³⁾
I/O	-	-	M9	P62	235 ⁽³⁾
I/O	-	-	L9	P63	238 ⁽³⁾
GND	-	-	K9	P64	-
I/O	P48	P45	N10	P65	241 ⁽³⁾
I/O	P49	P46	M10	P66	244 ⁽³⁾
I/O	-	-	L10	P67	247 ⁽³⁾
I/O	-	-	N11	P68	250 ⁽³⁾
I/O	P50	P47	M11	P69	253 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ GCK4 ⁽²⁾	P51	P48	L11	P70	256 ⁽³⁾
GND	P52	P49	N12	P71	-
DONE	P53	P50	M12	P72	-
VCC	P54	P51	N13	P73	-
PROGRAM	P55	P52	M13	P74	-
I/O (D7 ⁽²⁾)	P56	P53	L12	P75	259 ⁽³⁾

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84 ⁽⁴⁾	VQ100	CS144 ^(2,4)	TQ144	Bndry Scan
I/O, PGCK3 ⁽¹⁾ GCK5 ⁽²⁾	P57	P54	L13	P76	262 ⁽³⁾
I/O	-	-	K10	P77	265 ⁽³⁾
I/O	-	-	K11	P78	268 ⁽³⁾
I/O (D6 ⁽²⁾)	P58	P55	K12	P79	271 ⁽³⁾
I/O	-	P56	K13	P80	274 ⁽³⁾
GND	-	-	J10	P81	-
I/O	-	-	J11	P82	277 ⁽³⁾
I/O	-	-	J12	P83	280 ⁽³⁾
I/O (D5 ⁽²⁾)	P59	P57	J13	P84	283 ⁽³⁾
I/O	P60	P58	H10	P85	286 ⁽³⁾
I/O	-	P59	H11	P86	289 ⁽³⁾
I/O	-	P60	H12	P87	292 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	P61	H13	P88	295 ⁽³⁾
I/O	P62	P62	G12	P89	298 ⁽³⁾
VCC	P63	P63	G13	P90	-
GND	P64	P64	G11	P91	-
I/O (D3 ⁽²⁾)	P65	P65	G10	P92	301 ⁽³⁾
I/O	P66	P66	F13	P93	304 ⁽³⁾
I/O	-	P67	F12	P94	307 ⁽³⁾
I/O	-	-	F11	P95	310 ⁽³⁾
I/O (D2 ⁽²⁾)	P67	P68	F10	P96	313 ⁽³⁾
I/O	P68	P69	E13	P97	316 ⁽³⁾
I/O	-	-	E12	P98	319 ⁽³⁾
I/O	-	-	E11	P99	322 ⁽³⁾
GND	-	-	E10	P100	-
I/O (D1 ⁽²⁾)	P69	P70	D13	P101	325 ⁽³⁾
I/O	P70	P71	D12	P102	328 ⁽³⁾
I/O	-	-	D11	P103	331 ⁽³⁾
I/O	-	-	C13	P104	334 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P71	P72	C12	P105	337 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ GCK6 ⁽²⁾ (DOUT)	P72	P73	C11	P106	340 ⁽³⁾
CCLK	P73	P74	B13	P107	-
VCC	P74	P75	B12	P108	-
O, TDO	P75	P76	A13	P109	0
GND	P76	P77	A12	P110	-
I/O	P77	P78	B11	P111	2
I/O, PGCK4 ⁽¹⁾ GCK7 ⁽²⁾	P78	P79	A11	P112	5
I/O	-	-	D10	P113	8
I/O	-	-	C10	P114	11
I/O (CS1 ⁽²⁾)	P79	P80	B10	P115	14

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC ⁽²⁾	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P21	L2	P33	P49	239
Not Connected ⁽¹⁾ M1 ⁽²⁾	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected ⁽¹⁾ PWRDWN ⁽²⁾	P26	N2	P38	P54	246 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P27	M3	P39	P55	247 ⁽³⁾
I/O (HDC)	P28	N3	P40	P56	250 ⁽³⁾
I/O	-	K4	P41	P57	253 ⁽³⁾
I/O	-	L4	P42	P58	256 ⁽³⁾
I/O	P29	M4	P43	P59	259 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O (LDC)	P30	N4	P44	P60	262 ⁽³⁾
I/O	-	-	-	P61	265 ⁽³⁾
I/O	-	-	-	P62	268 ⁽³⁾
I/O	-	-	-	P63	271 ⁽³⁾
I/O	-	-	-	P64	274 ⁽³⁾
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 ⁽³⁾
I/O	-	M5	P47	P68	280 ⁽³⁾
I/O	P31	N5	P48	P69	283 ⁽³⁾
I/O	P32	K6	P49	P70	286 ⁽³⁾
VCC ⁽²⁾	-	-	-	P71	-
I/O	-	-	-	P72	289 ⁽³⁾
I/O	-	-	-	P73	292 ⁽³⁾
I/O	P33	L6	P50	P74	295 ⁽³⁾
I/O	P34	M6	P51	P75	298 ⁽³⁾
I/O	P35	N6	P52	P76	301 ⁽³⁾
I/O (INIT)	P36	M7	P53	P77	304 ⁽³⁾
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 ⁽³⁾
I/O	P40	N8	P57	P81	310 ⁽³⁾
I/O	P41	M8	P58	P82	313 ⁽³⁾
I/O	P42	L8	P59	P83	316 ⁽³⁾
I/O	-	-	-	P84	319 ⁽³⁾
I/O	-	-	-	P85	322 ⁽³⁾
VCC ⁽²⁾	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 ⁽³⁾
I/O	P44	N9	P61	P88	328 ⁽³⁾
I/O	-	M9	P62	P89	331 ⁽³⁾
I/O	-	L9	P63	P90	334 ⁽³⁾
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 ⁽³⁾
I/O	-	-	-	P94	340 ⁽³⁾
I/O	-	-	-	P95	343 ⁽³⁾
I/O	-	-	-	P96	346 ⁽³⁾
I/O	P45	N10	P65	P97	349 ⁽³⁾
I/O	P46	M10	P66	P98	352 ⁽³⁾
I/O	-	L10	P67	P99	355 ⁽³⁾
I/O	-	N11	P68	P100	358 ⁽³⁾
I/O	P47	M11	P69	P101	361 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P48	L11	P70	P102	364 ⁽³⁾
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 ⁽¹⁾	P33 ⁽¹⁾	P39	P65	P71 ⁽¹⁾
P86 ⁽¹⁾	P92	P111	P121 ⁽¹⁾	P140 ⁽¹⁾	P144
P165	P173 ⁽¹⁾	P192 ⁽¹⁾	P202	P203	-
9/16/98					

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by [PDN2004-01](#)

XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
VCC	P89	P128	P183	P212	VCC ⁽⁴⁾	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC ⁽⁴⁾	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC ⁽⁴⁾	A1	-
GND	P1	P1	P1	P1	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
O, TDO	P157	P181	A19	B17	0
GND	P158	P182	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P159	P183	B18	A18	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P160	P184	B17	A17	5
I/O	P161	P185	C17	D16	8
I/O	P162	P186	D16	C16	11
I/O (CS1 ⁽²⁾)	P163	P187	A18	B16	14
I/O	P164	P188	A17	A16	17
I/O	-	-	-	E15	20
I/O	-	-	-	C15	23
I/O	P165	P189	C16	D15	26
I/O	-	P190	B16	A15	29
I/O	P166	P191	A16	E14	32
I/O	P167	P192	C15	C14	35
I/O	P168	P193	B15	B14	38
I/O	P169	P194	A15	D14	41
GND	P170	P196	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P171	P197	B14	A14	44
I/O	P172	P198	A14	C13	47
I/O	-	P199	C13	B13	50
I/O	-	P200	B13	A13	53
VCC	P173	P201	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	-	A13	A12	56
I/O	-	-	D12	C12	59
I/O	P174	P202	C12	B12	62
I/O	P175	P203	B12	D12	65
I/O	P176	P205	A12	A11	68
I/O	P177	P206	B11	B11	71
I/O	P178	P207	C11	C11	74
I/O	P179	P208	A11	D11	77
I/O	P180	P209	A10	A10	80
I/O	P181	P210	B10	B10	83
GND	P182	P211	GND ⁽⁴⁾	GND ⁽⁴⁾	-

2/8/00

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS40XL is not part of the Boundary Scan chain. For the XCS40XL, subtract 1 from all Boundary Scan numbers from GCK3 on (343 and higher).
4. Pads labeled GND⁽⁴⁾ or VCC⁽⁴⁾ are internally bonded to Ground or VCC planes within the package.
5. CS280 package discontinued by [PDN2004-01](#)

Additional XCS40/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

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CS280

VCC Pins					
A1	A7	B5	B15	C10	C17
D13	E3	E18	G1	G19	K2
K17	M4	N16	R3	R18	T7
U3	U10	U17	V5	V15	W13
GND Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-

5/19/99