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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	576
Number of Logic Elements/Cells	1368
Total RAM Bits	18432
Number of I/O	192
Number of Gates	30000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcs30-3pq240c">https://www.e-xfl.com/product-detail/xilinx/xcs30-3pq240c</a>

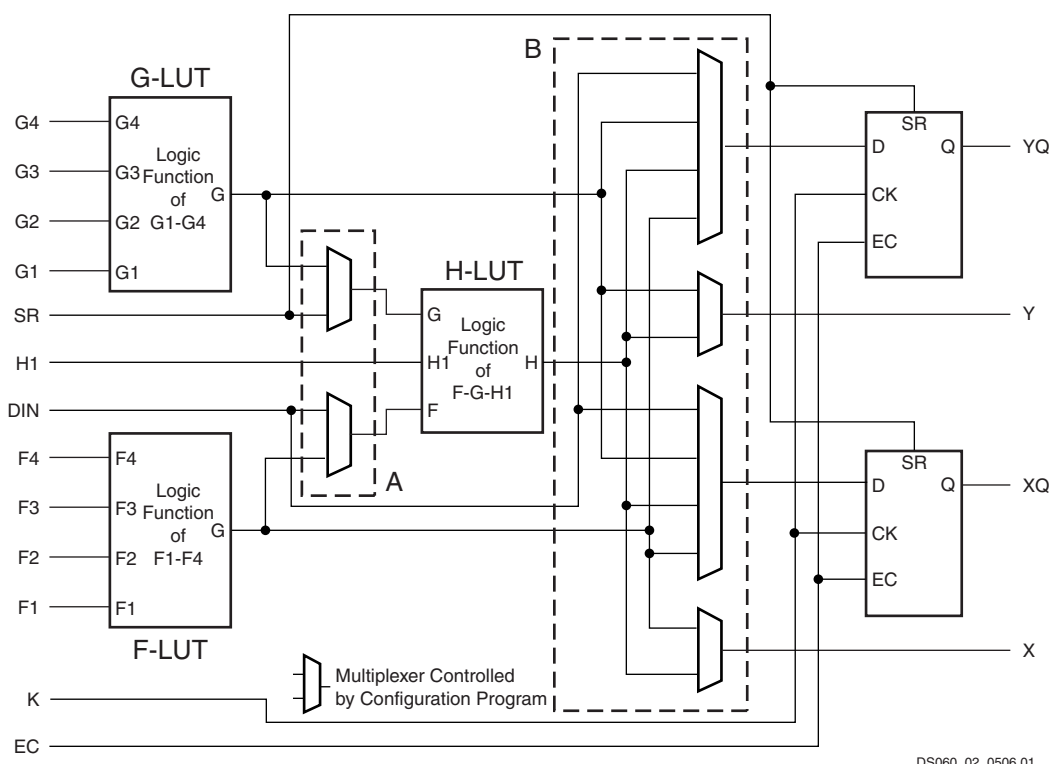


Figure 2: Spartan/XL Simplified CLB Logic Diagram (some features not shown)

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

**Note:** When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

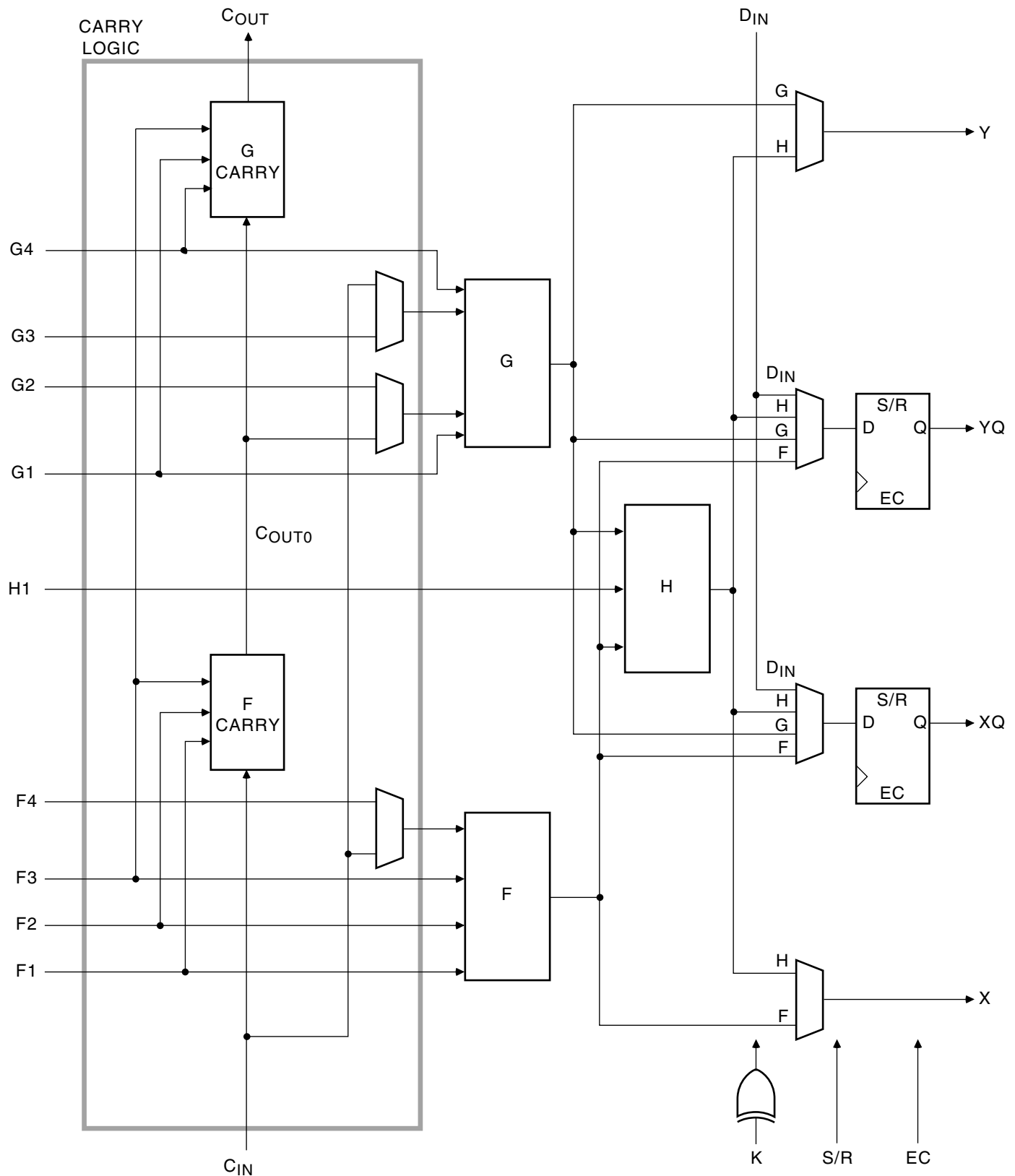
### Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.

### Latches (Spartan-XL Family Only)

The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.



**Figure 16: Fast Carry Logic in Spartan/XL CLB**

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Table 12: Boundary Scan Instructions

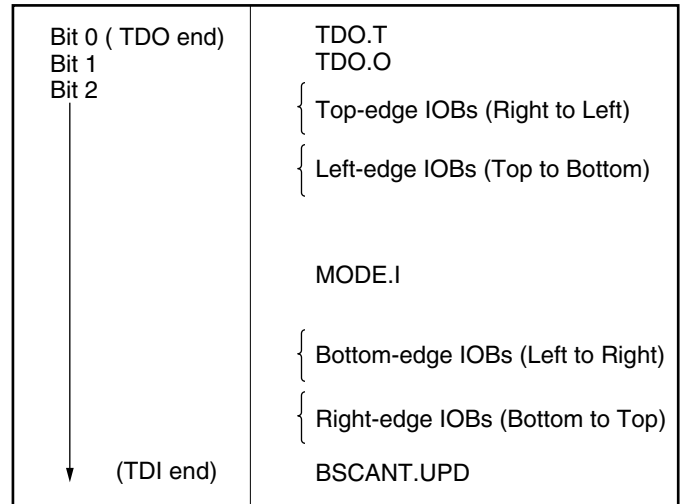
Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	IDCODE (Spartan-XL only)	IDCODE Register	-
1	1	1	BYPASS	Bypass Register	-

### Bit Sequence

The bit sequence within each IOB is: In, Out, 3-state. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contribute all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 21. The device-specific pinout tables for the Spartan/XL devices include the boundary scan locations for each IOB pin.



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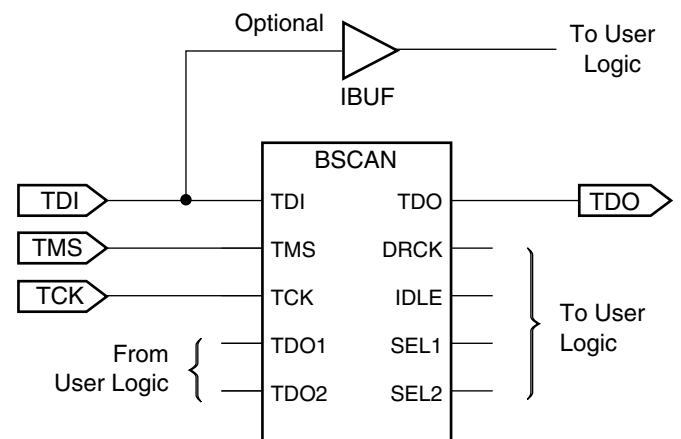
Figure 21: Boundary Scan Bit Sequence

BSDL (Boundary Scan Description Language) files for Spartan/XL devices are available on the Xilinx website in the File Download area. Note that the 5V Spartan devices and 3V Spartan-XL devices have different BSDL files.

### Including Boundary Scan in a Design

If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 22.



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Figure 22: Boundary Scan Example

Even if the boundary scan symbol is used in a design, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

### Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state.
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "Boundary Scan in FPGA Devices."

### Boundary Scan Enhancements (Spartan-XL Family Only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

**IDCODE:** The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

c = the company code (49h for Xilinx)

a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)

f = the family code (02h for Spartan-XL family)

v = the die version number

Table 13: IDCODEs Assigned to Spartan-XL FPGAs

FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

**Configuration State:** The configuration state is available to JTAG controllers.

**Configuration Disable:** The JTAG port can be prevented from configuring the FPGA.

**TCK Startup:** TCK can now be used to clock the start-up block in addition to other user clocks.

**CCLK Holdoff:** Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

**Reissue Configure:** The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

**Bypass FF:** Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

### Power-Down (Spartan-XL Family Only)

All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low power-down pin (PWRDWN) to reduce supply current to 100  $\mu$ A typical. The PWRDWN pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The PWRDWN pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

$V_{CC}$  must continue to be supplied during Power-down, and configuration data is maintained. When the PWRDWN pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The PROGRAM pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

PWRDWN has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before PWRDWN to affect the order of events. When the PWRDWN signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of PWRDWN before using the device.

figuration are shown in Table 14 and Table 15.

**Table 14: Pin Functions During Configuration (Spartan Family Only)**

Configuration Mode (MODE Pin)		User Operation
Slave Serial (High)	Master Serial (Low)	
MODE (I)	MODE (I)	MODE
HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

**Notes:**

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3.  $\overline{\text{INIT}}$  is an open-drain output during configuration.

**Table 15: Pin Functions During Configuration (Spartan-XL Family Only)**

CONFIGURATION MODE <M1:M0>			User Operation
Slave Serial [1:1]	Master Serial [1:0]	Express [0:X]	
M1 (High) (I)	M1 (High) (I)	M1(Low) (I)	M1
M0 (High) (I)	M0 (Low) (I)	M0 (I)	M0
HDC (High)	HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

**Notes:**

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3.  $\overline{\text{INIT}}$  is an open-drain output during configuration.

## Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is –50% to +25%.

In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

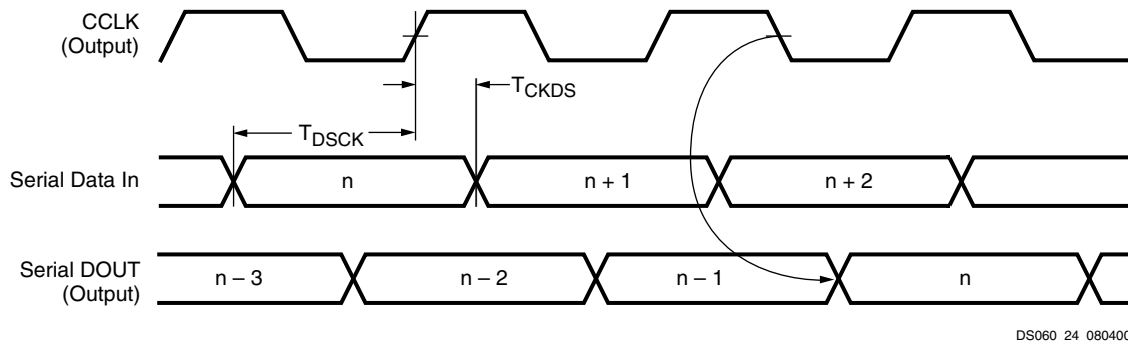
When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the

falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in [Figure 24](#).

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Earlier families such as the XC3000 series do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either  $\overline{\text{LDC}}$  or DONE. Using  $\overline{\text{LDC}}$  avoids potential contention on the DIN pin, if this pin is configured as user I/O, but  $\overline{\text{LDC}}$  is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

[Figure 25](#) shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Symbol	Description	Min	Units
CCLK	$T_{\text{DSCK}}$	DIN setup	20	ns
	$T_{\text{CKDS}}$	DIN hold	0	ns

### Notes:

1. At power-up,  $V_{\text{CC}}$  must rise from 2.0V to  $V_{\text{CC}}$  min in less than 25 ms, otherwise delay configuration by pulling  $\overline{\text{PROGRAM}}$  Low until  $V_{\text{CC}}$  is valid.
2. Master Serial mode timing is based on testing in slave mode.

**Figure 24: Master Serial Mode Programming Switching Characteristics**

## Slave Serial Mode

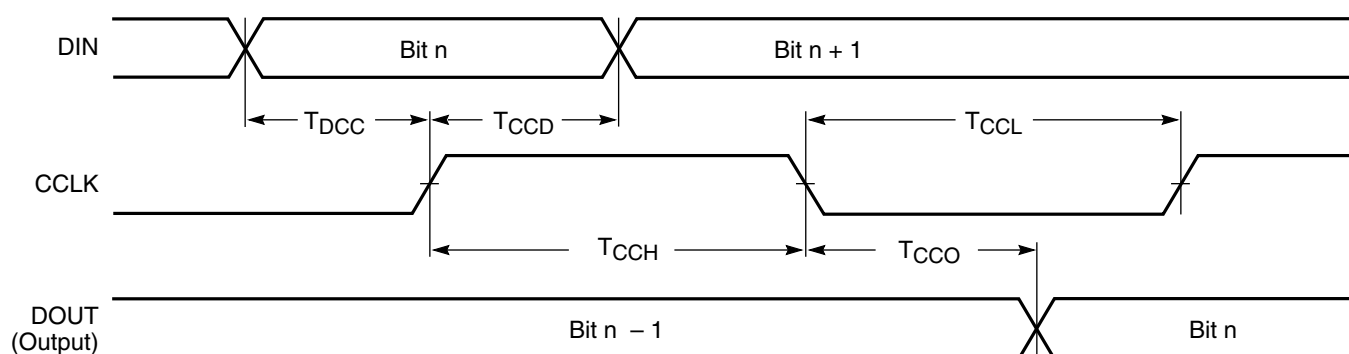
In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

[Figure 25](#) shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.





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Symbol		Description	Min	Max	Units
$T_{DCC}$	CCLK	DIN setup	20	-	ns
$T_{CCD}$		DIN hold	0	-	ns
$T_{CCO}$		DIN to DOUT	-	30	ns
$T_{CCH}$		High time	40	-	ns
$T_{CCL}$		Low time	40	-	ns
$F_{CC}$		Frequency	-	12.5	MHz

**Notes:**

1. Configuration must be delayed until the  $\overline{INIT}$  pins of all daisy-chained FPGAs are High.

Figure 26: Slave Serial Mode Programming Switching Characteristics

**Express Mode (Spartan-XL Family Only)**

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

**Pseudo Daisy Chain**

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices

are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

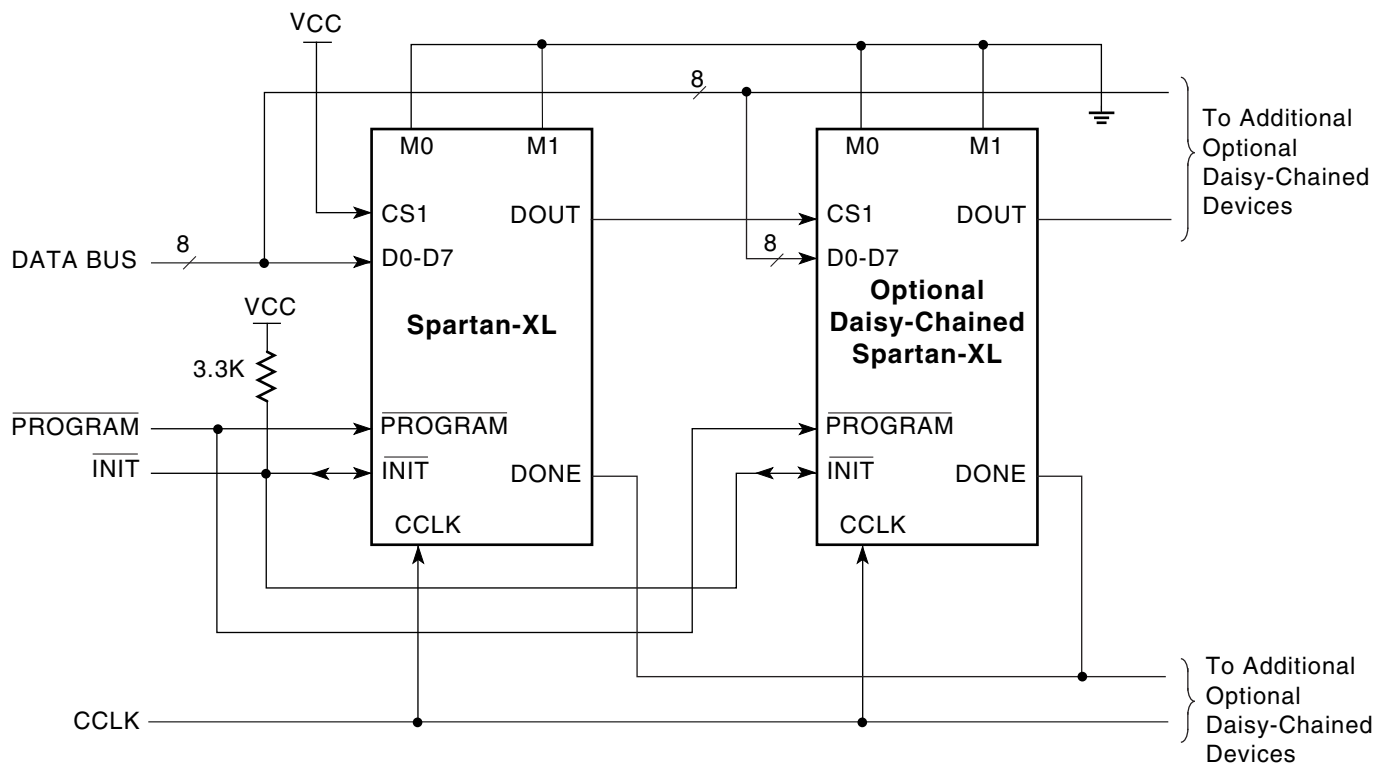
The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized



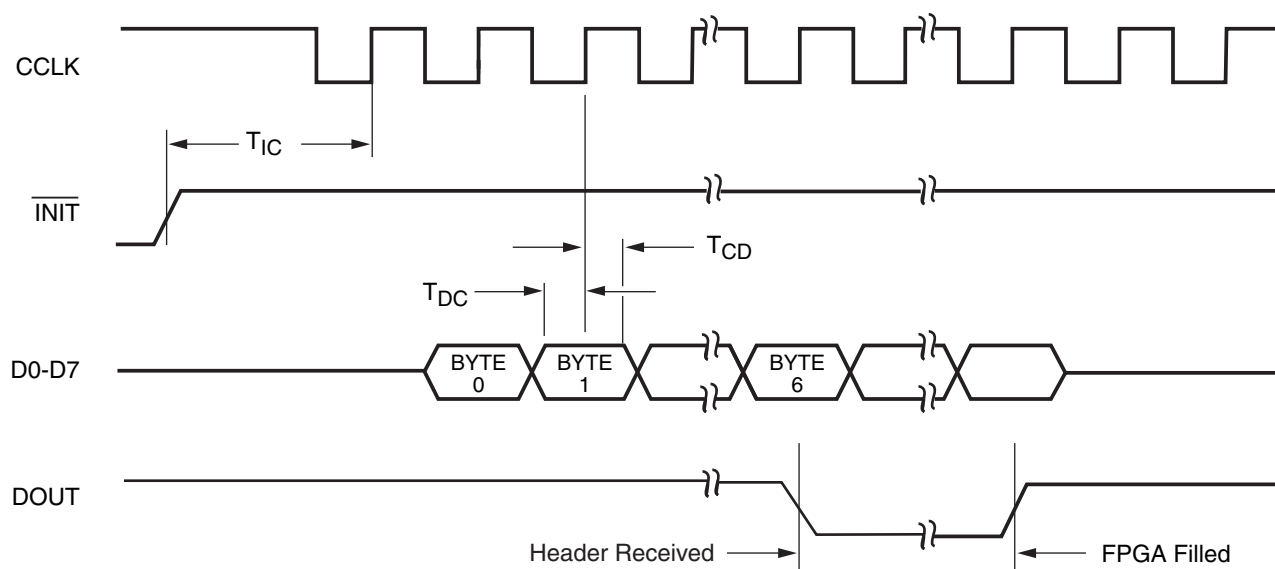
to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device

in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.



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Figure 27: Express Mode Circuit Diagram



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Symbol		Description	Min	Max	Units
$T_{IC}$	CCLK	$\overline{INIT}$ (High) setup time	5	-	$\mu s$
$T_{DC}$		D0-D7 setup time	20	-	ns
$T_{CD}$		D0-D7 hold time	0	-	ns
$T_{CCH}$		CCLK High time	45	-	ns
$T_{CCL}$		CCLK Low time	45	-	ns
$F_{CC}$		CCLK Frequency	-	10	MHz

**Notes:**

1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: Express Mode Programming Switching Characteristics

## Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

## Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right.

Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

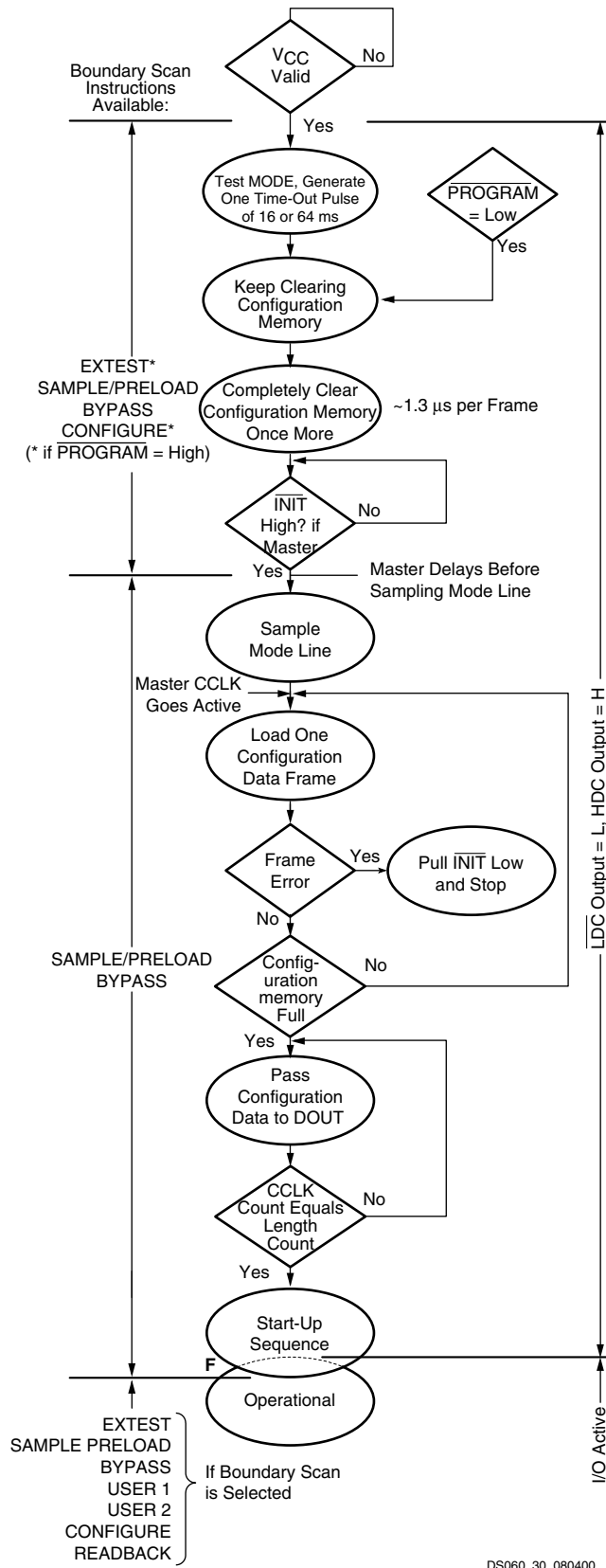


Figure 30: Power-up Configuration Sequence

## Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count for serial modes. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Spartan-XL family Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain  $\overline{\text{INIT}}$  pin Low. After all configuration frames have been loaded into an FPGA using a serial mode, DOUT again follows the input data so that the remaining data is passed on to the next device. In Spartan-XL family Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

## Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the  $\overline{\text{PROGRAM}}$  input, or pull the bidirectional  $\overline{\text{INIT}}$  pin Low, using an open-collector (open-drain) driver. (See Figure 30.)

A Low on the  $\overline{\text{PROGRAM}}$  input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as  $\overline{\text{PROGRAM}}$  is Low, the FPGA keeps clearing its configuration memory. When  $\overline{\text{PROGRAM}}$  goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the  $\overline{\text{INIT}}$  input is not externally held Low. Note that a Low on the  $\overline{\text{PROGRAM}}$  input automatically forces a Low on the  $\overline{\text{INIT}}$  output. The Spartan/XL FPGA  $\overline{\text{PROGRAM}}$  pin has a permanent weak pull-up.

Avoid holding  $\overline{\text{PROGRAM}}$  Low for more than 500  $\mu\text{s}$ . The 500  $\mu\text{s}$  maximum limit is only a recommendation, not a requirement. The only effect of holding  $\overline{\text{PROGRAM}}$  Low for more than 500  $\mu\text{s}$  is an increase in current, measured at about 40 mA in the XCS40XL. This increased current cannot damage the device. This applies only during reconfiguration, not during power-up. The  $\overline{\text{INIT}}$  pin can also be held Low to delay reconfiguration, and the same characteristics apply as for the  $\overline{\text{PROGRAM}}$  pin.

Using an open-collector or open-drain driver to hold  $\overline{\text{INIT}}$  Low before the beginning of configuration causes the FPGA

## Spartan-XL Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For

more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
$T_{GLS}$	From pad through buffer, to any clock K	XCS05XL	1.4	1.5	ns
		XCS10XL	1.7	1.8	ns
		XCS20XL	2.0	2.1	ns
		XCS30XL	2.3	2.5	ns
		XCS40XL	2.6	2.8	ns

### Spartan-XL Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clocks						
T <sub>CH</sub>	Clock High time	2.0	-	2.3	-	ns
T <sub>CL</sub>	Clock Low time	2.0	-	2.3	-	ns
Combinatorial Delays						
T <sub>ILO</sub>	F/G inputs to X/Y outputs	-	1.0	-	1.1	ns
T <sub>IHO</sub>	F/G inputs via H to X/Y outputs	-	1.7	-	2.0	ns
T <sub>ITO</sub>	F/G inputs via transparent latch to Q outputs	-	1.5	-	1.8	ns
T <sub>HH1O</sub>	C inputs via H1 via H to X/Y outputs	-	1.5	-	1.8	ns
Sequential Delays						
T <sub>CKO</sub>	Clock K to Flip-Flop or latch outputs Q	-	1.2	-	1.4	ns
Setup Time before Clock K						
T <sub>ICK</sub>	F/G inputs	0.6	-	0.7	-	ns
T <sub>IHCK</sub>	F/G inputs via H	1.3	-	1.6	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T <sub>RPW</sub>	Width (High)	2.5	-	2.8	-	ns
T <sub>RIO</sub>	Delay from C inputs via S/R, going High to Q	-	2.3	-	2.7	ns
Global Set/Reset						
T <sub>MRW</sub>	Minimum GSR Pulse Width	10.5	-	11.5	-	ns
T <sub>MRQ</sub>	Delay from GSR input to any Q	See <a href="#">page 60</a> for T <sub>RRI</sub> values per device.				
F <sub>TOG</sub>	Toggle Frequency (MHz) (for export control purposes)	-	250	-	217	MHz

## Spartan-XL Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case oper-

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

### Spartan-XL Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Global Clock to Output using OFF					
T <sub>ICKOF</sub>	Fast	XCS05XL	4.6	5.2	ns
		XCS10XL	4.9	5.5	ns
		XCS20XL	5.2	5.8	ns
		XCS30XL	5.5	6.2	ns
		XCS40XL	5.8	6.5	ns
Slew Rate Adjustment					
T <sub>SLOW</sub>	For Output SLOW option add	All Devices	1.5	1.7	ns

#### Notes:

1. Output delays are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V<sub>CC</sub> threshold with 50 pF external capacitive load.
3. OFF = Output Flip Flop

## Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See **Global Signals: GSR and GTS**, page 20 for more information.

Device pins for Spartan/XL devices are described in **Table 18**.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pin-outs as the standard package options.

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
<b>Permanently Dedicated Pins</b>			
V <sub>CC</sub>	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 – 0.1 $\mu$ F capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See <b>Violating the Maximum High and Low Time Specification for the Readback Clock</b> , page 39 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an open-drain output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs.  The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$ .  The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used.  During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.



### XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 <sup>(2,4)</sup>	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC <sup>(2)</sup>	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2 <sup>(1)</sup> , GCK2 <sup>(2)</sup>	P21	L2	P33	P49	239
Not Connected <sup>(1)</sup> M1 <sup>(2)</sup>	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE <sup>(1)</sup> , M0 <sup>(2)</sup>	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected <sup>(1)</sup> PWRDWN <sup>(2)</sup>	P26	N2	P38	P54	246 <sup>(1)</sup>
I/O, PGCK2 <sup>(1)</sup> , GCK3 <sup>(2)</sup>	P27	M3	P39	P55	247 <sup>(3)</sup>
I/O (HDC)	P28	N3	P40	P56	250 <sup>(3)</sup>
I/O	-	K4	P41	P57	253 <sup>(3)</sup>
I/O	-	L4	P42	P58	256 <sup>(3)</sup>
I/O	P29	M4	P43	P59	259 <sup>(3)</sup>

### XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 <sup>(2,4)</sup>	TQ144	PQ208	Bndry Scan
I/O (LDC)	P30	N4	P44	P60	262 <sup>(3)</sup>
I/O	-	-	-	P61	265 <sup>(3)</sup>
I/O	-	-	-	P62	268 <sup>(3)</sup>
I/O	-	-	-	P63	271 <sup>(3)</sup>
I/O	-	-	-	P64	274 <sup>(3)</sup>
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 <sup>(3)</sup>
I/O	-	M5	P47	P68	280 <sup>(3)</sup>
I/O	P31	N5	P48	P69	283 <sup>(3)</sup>
I/O	P32	K6	P49	P70	286 <sup>(3)</sup>
VCC <sup>(2)</sup>	-	-	-	P71	-
I/O	-	-	-	P72	289 <sup>(3)</sup>
I/O	-	-	-	P73	292 <sup>(3)</sup>
I/O	P33	L6	P50	P74	295 <sup>(3)</sup>
I/O	P34	M6	P51	P75	298 <sup>(3)</sup>
I/O	P35	N6	P52	P76	301 <sup>(3)</sup>
I/O (INIT)	P36	M7	P53	P77	304 <sup>(3)</sup>
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 <sup>(3)</sup>
I/O	P40	N8	P57	P81	310 <sup>(3)</sup>
I/O	P41	M8	P58	P82	313 <sup>(3)</sup>
I/O	P42	L8	P59	P83	316 <sup>(3)</sup>
I/O	-	-	-	P84	319 <sup>(3)</sup>
I/O	-	-	-	P85	322 <sup>(3)</sup>
VCC <sup>(2)</sup>	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 <sup>(3)</sup>
I/O	P44	N9	P61	P88	328 <sup>(3)</sup>
I/O	-	M9	P62	P89	331 <sup>(3)</sup>
I/O	-	L9	P63	P90	334 <sup>(3)</sup>
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 <sup>(3)</sup>
I/O	-	-	-	P94	340 <sup>(3)</sup>
I/O	-	-	-	P95	343 <sup>(3)</sup>
I/O	-	-	-	P96	346 <sup>(3)</sup>
I/O	P45	N10	P65	P97	349 <sup>(3)</sup>
I/O	P46	M10	P66	P98	352 <sup>(3)</sup>
I/O	-	L10	P67	P99	355 <sup>(3)</sup>
I/O	-	N11	P68	P100	358 <sup>(3)</sup>
I/O	P47	M11	P69	P101	361 <sup>(3)</sup>
I/O, SGCK3 <sup>(1)</sup> , GCK4 <sup>(2)</sup>	P48	L11	P70	P102	364 <sup>(3)</sup>
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

## XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 <sup>(2,4)</sup>	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7 <sup>(2)</sup> )	P53	L12	P75	P107	367 <sup>(3)</sup>
I/O, PGCK3 <sup>(1)</sup> , GCK5 <sup>(2)</sup>	P54	L13	P76	P108	370 <sup>(3)</sup>
I/O	-	K10	P77	P109	373 <sup>(3)</sup>
I/O	-	K11	P78	P110	376 <sup>(3)</sup>
I/O (D6 <sup>(2)</sup> )	P55	K12	P79	P112	379 <sup>(3)</sup>
I/O	P56	K13	P80	P113	382 <sup>(3)</sup>
I/O	-	-	-	P114	385 <sup>(3)</sup>
I/O	-	-	-	P115	388 <sup>(3)</sup>
I/O	-	-	-	P116	391 <sup>(3)</sup>
I/O	-	-	-	P117	394 <sup>(3)</sup>
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 <sup>(3)</sup>
I/O	-	J12	P83	P120	400 <sup>(3)</sup>
VCC <sup>(2)</sup>	-	-	-	P121	-
I/O (D5 <sup>(2)</sup> )	P57	J13	P84	P122	403 <sup>(3)</sup>
I/O	P58	H10	P85	P123	406 <sup>(3)</sup>
I/O	-	-	-	P124	409 <sup>(3)</sup>
I/O	-	-	-	P125	412 <sup>(3)</sup>
I/O	P59	H11	P86	P126	415 <sup>(3)</sup>
I/O	P60	H12	P87	P127	418 <sup>(3)</sup>
I/O (D4 <sup>(2)</sup> )	P61	H13	P88	P128	421 <sup>(3)</sup>
I/O	P62	G12	P89	P129	424 <sup>(3)</sup>
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3 <sup>(2)</sup> )	P65	G10	P92	P132	427 <sup>(3)</sup>
I/O	P66	F13	P93	P133	430 <sup>(3)</sup>
I/O	P67	F12	P94	P134	433 <sup>(3)</sup>
I/O	-	F11	P95	P135	436 <sup>(3)</sup>
I/O	-	-	-	P136	439 <sup>(3)</sup>
I/O	-	-	-	P137	442 <sup>(3)</sup>
I/O (D2 <sup>(2)</sup> )	P68	F10	P96	P138	445 <sup>(3)</sup>
I/O	P69	E13	P97	P139	448 <sup>(3)</sup>
VCC <sup>(2)</sup>	-	-	-	P140	-
I/O	-	E12	P98	P141	451 <sup>(3)</sup>
I/O	-	E11	P99	P142	454 <sup>(3)</sup>
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 <sup>(3)</sup>
I/O	-	-	-	P146	460 <sup>(3)</sup>
I/O	-	-	-	P147	463 <sup>(3)</sup>
I/O	-	-	-	P148	466 <sup>(3)</sup>
I/O (D1 <sup>(2)</sup> )	P70	D13	P101	P149	469 <sup>(3)</sup>
I/O	P71	D12	P102	P150	472 <sup>(3)</sup>
I/O	-	D11	P103	P151	475 <sup>(3)</sup>

## XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 <sup>(2,4)</sup>	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 <sup>(3)</sup>
I/O (D0 <sup>(2)</sup> , DIN)	P72	C12	P105	P153	481 <sup>(3)</sup>
I/O, SGCK4 <sup>(1)</sup> , GCK6 <sup>(2)</sup> (DOUT)	P73	C11	P106	P154	484 <sup>(3)</sup>
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4 <sup>(1)</sup> , GCK7 <sup>(2)</sup>	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1 <sup>(2)</sup> )	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC <sup>(2)</sup>	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

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### XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 <sup>(5)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(5)</sup>	CS280 <sup>(2,5)</sup>	Bndry Scan
I/O	-	-	P124	P144	M20	L19	493 <sup>(3)</sup>
I/O	-	-	P125	P145	L19	L18	496 <sup>(3)</sup>
I/O	P59	P86	P126	P146	L18	L17	499 <sup>(3)</sup>
I/O	P60	P87	P127	P147	L20	L16	502 <sup>(3)</sup>
I/O (D4 <sup>(2)</sup> )	P61	P88	P128	P148	K20	K19	505 <sup>(3)</sup>
I/O	P62	P89	P129	P149	K19	K18	508 <sup>(3)</sup>
VCC	P63	P90	P130	P150	VCC <sup>(4)</sup>	K17	-
GND	P64	P91	P131	P151	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O (D3 <sup>(2)</sup> )	P65	P92	P132	P152	K18	K16	511 <sup>(3)</sup>
I/O	P66	P93	P133	P153	K17	K15	514 <sup>(3)</sup>
I/O	P67	P94	P134	P154	J20	J19	517 <sup>(3)</sup>
I/O	-	P95	P135	P155	J19	J18	520 <sup>(3)</sup>
I/O	-	-	P136	P156	J18	J17	523 <sup>(3)</sup>
I/O	-	-	P137	P157	J17	J16	526 <sup>(3)</sup>
I/O (D2 <sup>(2)</sup> )	P68	P96	P138	P159	H19	H17	529 <sup>(3)</sup>
I/O	P69	P97	P139	P160	H18	H16	532 <sup>(3)</sup>
VCC	-	-	P140	P161	VCC <sup>(4)</sup>	G19	-
I/O	-	P98	P141	P162	G19	G18	535 <sup>(3)</sup>
I/O	-	P99	P142	P163	F20	G17	538 <sup>(3)</sup>
I/O	-	-	-	P164	G18	G16	541 <sup>(3)</sup>
I/O	-	-	-	P165	F19	F19	544 <sup>(3)</sup>
GND	-	P100	P143	P166	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	-	-	-	P167	F18	F18	547 <sup>(3)</sup>
I/O	-	-	P144	P168	E19	F17	550 <sup>(3)</sup>
I/O	-	-	P145	P169	D20	F16	553 <sup>(3)</sup>
I/O	-	-	P146	P170	E18	F15	556 <sup>(3)</sup>
I/O	-	-	P147	P171	D19	E19	559 <sup>(3)</sup>
I/O	-	-	P148	P172	C20	E17	562 <sup>(3)</sup>
I/O (D1 <sup>(2)</sup> )	P70	P101	P149	P173	E17	E16	565 <sup>(3)</sup>
I/O	P71	P102	P150	P174	D18	D19	568 <sup>(3)</sup>
I/O	-	P103	P151	P175	C19	C19	571 <sup>(3)</sup>
I/O	-	P104	P152	P176	B20	B19	574 <sup>(3)</sup>
I/O (D0 <sup>(2)</sup> , DIN)	P72	P105	P153	P177	C18	C18	577 <sup>(3)</sup>
I/O, SGCK4 <sup>(1)</sup> , GCK6 <sup>(2)</sup> (DOUT)	P73	P106	P154	P178	B19	B18	580 <sup>(3)</sup>
CCLK	P74	P107	P155	P179	A20	A19	-
VCC	P75	P108	P156	P180	VCC <sup>(4)</sup>	C17	-
O, TDO	P76	P109	P157	P181	A19	B17	0
GND	P77	P110	P158	P182	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P78	P111	P159	P183	B18	A18	2
I/O, PGCK4 <sup>(1)</sup> , GCK7 <sup>(2)</sup>	P79	P112	P160	P184	B17	A17	5
I/O	-	P113	P161	P185	C17	D16	8
I/O	-	P114	P162	P186	D16	C16	11
I/O (CS1 <sup>(2)</sup> )	P80	P115	P163	P187	A18	B16	14
I/O	P81	P116	P164	P188	A17	A16	17
I/O	-	-	P165	P189	C16	D15	20

## XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 <sup>(5)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(5)</sup>	CS280 <sup>(2,5)</sup>	Bndry Scan
I/O	-	-	-	P190	B16	A15	23
I/O	-	P117	P166	P191	A16	E14	26
I/O	-	-	P167	P192	C15	C14	29
I/O	-	-	P168	P193	B15	B14	32
I/O	-	-	P169	P194	A15	D14	35
GND	-	P118	P170	P196	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	-	P119	P171	P197	B14	A14	38
I/O	-	P120	P172	P198	A14	C13	41
I/O	-	-	-	P199	C13	B13	44
I/O	-	-	-	P200	B13	A13	47
VCC	-	-	P173	P201	VCC <sup>(4)</sup>	D13	-
I/O	P82	P121	P174	P202	C12	B12	50
I/O	P83	P122	P175	P203	B12	D12	53
I/O	-	-	P176	P205	A12	A11	56
I/O	-	-	P177	P206	B11	B11	59
I/O	P84	P123	P178	P207	C11	C11	62
I/O	P85	P124	P179	P208	A11	D11	65
I/O	P86	P125	P180	P209	A10	A10	68
I/O	P87	P126	P181	P210	B10	B10	71
GND	P88	P127	P182	P211	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-

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## Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND<sup>(4)</sup> or VCC<sup>(4)</sup> are internally bonded to Ground or VCC planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)

## Additional XCS30/XL Package Pins

## PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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## BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

## GND Pins

A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

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## CS280

VCC Pins					
A1	A7	C10	C17	D13	G1
G1	G19	K2	K17	M4	N16
T7	U3	U10	U17	W13	-
GND Pins					

### CS280

VCC Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-
Not Connected Pins					
A4	A12	C8	C12	C15	D1
D2	D5	D8	D17	D18	E15
H2	H3	H18	H19	L4	M1
M16	M18	R2	R4	R5	R15
R17	T8	T15	U5	V8	V12
W12	W16	-	-	-	-
Not Connected Pins (VCC in XCS40XL)					
B5	B15	E3	E18	R3	R18
V5	V15	-	-	-	-

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### XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 <sup>(2,5)</sup>	Bndry Scan
VCC	P183	P212	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	P184	P213	C10	D10	86
I/O	P185	P214	D10	E10	89
I/O	P186	P215	A9	A9	92
I/O	P187	P216	B9	B9	95
I/O	P188	P217	C9	C9	98
I/O	P189	P218	D9	D9	101
I/O	P190	P220	A8	A8	104
I/O	P191	P221	B8	B8	107
I/O	-	-	C8	C8	110
I/O	-	-	A7	D8	113
VCC	P192	P222	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	-	P223	A6	B7	116
I/O	-	P224	C7	C7	119
I/O	P193	P225	B6	D7	122
I/O	P194	P226	A5	A6	125
GND	P195	P227	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P196	P228	C6	B6	128
I/O	P197	P229	B5	C6	131
I/O	P198	P230	A4	D6	134
I/O	P199	P231	C5	E6	137

### XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 <sup>(2,5)</sup>	Bndry Scan
I/O	P200	P232	B4	A5	140
I/O	P201	P233	A3	C5	143
I/O	-	-	-	D5	146
I/O	-	-	-	A4	149
I/O	P202	P234	D5	B4	152
I/O	P203	P235	C4	C4	155
I/O	P204	P236	B3	A3	158
I/O	P205	P237	B2	A2	161
I/O	P206	P238	A2	B3	164
I/O, SGCK1 <sup>(1)</sup> , GCK8 <sup>(2)</sup>	P207	P239	C3	B2	167
VCC	P208	P240	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
GND	P1	P1	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O, PGCK1 <sup>(1)</sup> , GCK1 <sup>(2)</sup>	P2	P2	B1	C3	170
I/O	P3	P3	C2	C2	173
I/O	P4	P4	D2	B1	176
I/O	P5	P5	D3	C1	179
I/O, TDI	P6	P6	E4	D4	182
I/O, TCK	P7	P7	C1	D3	185
I/O	-	-	-	D2	188
I/O	-	-	-	D1	191
I/O	P8	P8	D1	E2	194
I/O	P9	P9	E3	E4	197
I/O	P10	P10	E2	E1	200
I/O	P11	P11	E1	F5	203
I/O	P12	P12	F3	F3	206
I/O	-	P13	F2	F2	209
GND	P13	P14	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P14	P15	G3	F4	212
I/O	P15	P16	G2	F1	215
I/O, TMS	P16	P17	G1	G3	218
I/O	P17	P18	H3	G2	221
VCC	P18	P19	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	-	P20	H2	G4	224
I/O	-	P21	H1	H1	227
I/O	-	-	J4	H3	230
I/O	-	-	J3	H2	233
I/O	P19	P23	J2	H4	236
I/O	P20	P24	J1	J1	239
I/O	P21	P25	K2	J2	242
I/O	P22	P26	K3	J3	245
I/O	P23	P27	K1	J4	248
I/O	P24	P28	L1	K1	251

## XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 <sup>(2,5)</sup>	Bndry Scan
O, TDO	P157	P181	A19	B17	0
GND	P158	P182	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P159	P183	B18	A18	2
I/O, PGCK4 <sup>(1)</sup> , GCK7 <sup>(2)</sup>	P160	P184	B17	A17	5
I/O	P161	P185	C17	D16	8
I/O	P162	P186	D16	C16	11
I/O (CS1 <sup>(2)</sup> )	P163	P187	A18	B16	14
I/O	P164	P188	A17	A16	17
I/O	-	-	-	E15	20
I/O	-	-	-	C15	23
I/O	P165	P189	C16	D15	26
I/O	-	P190	B16	A15	29
I/O	P166	P191	A16	E14	32
I/O	P167	P192	C15	C14	35
I/O	P168	P193	B15	B14	38
I/O	P169	P194	A15	D14	41
GND	P170	P196	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P171	P197	B14	A14	44
I/O	P172	P198	A14	C13	47
I/O	-	P199	C13	B13	50
I/O	-	P200	B13	A13	53
VCC	P173	P201	VCC <sup>(4)</sup>	VCC <sup>(4)</sup>	-
I/O	-	-	A13	A12	56
I/O	-	-	D12	C12	59
I/O	P174	P202	C12	B12	62
I/O	P175	P203	B12	D12	65
I/O	P176	P205	A12	A11	68
I/O	P177	P206	B11	B11	71
I/O	P178	P207	C11	C11	74
I/O	P179	P208	A11	D11	77
I/O	P180	P209	A10	A10	80
I/O	P181	P210	B10	B10	83
GND	P182	P211	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-

2/8/00

## Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS40XL is not part of the Boundary Scan chain. For the XCS40XL, subtract 1 from all Boundary Scan numbers from GCK3 on (343 and higher).
4. Pads labeled GND<sup>(4)</sup> or VCC<sup>(4)</sup> are internally bonded to Ground or VCC planes within the package.
5. CS280 package discontinued by [PDN2004-01](#)

## Additional XCS40/XL Package Pins

## PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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## BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

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## CS280

VCC Pins					
A1	A7	B5	B15	C10	C17
D13	E3	E18	G1	G19	K2
K17	M4	N16	R3	R18	T7
U3	U10	U17	V5	V15	W13
GND Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-

5/19/99