# AMD Xilinx - XCS30-3TQ144I Datasheet

**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 576 |
| Number of Logic Elements/Cells | 1368 |
| Total RAM Bits | 18432 |
| Number of I/O | 113 |
| Number of Gates | 30000 |
| Voltage - Supply | 4.5V ~ 5.5V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcs30-3tq144i |

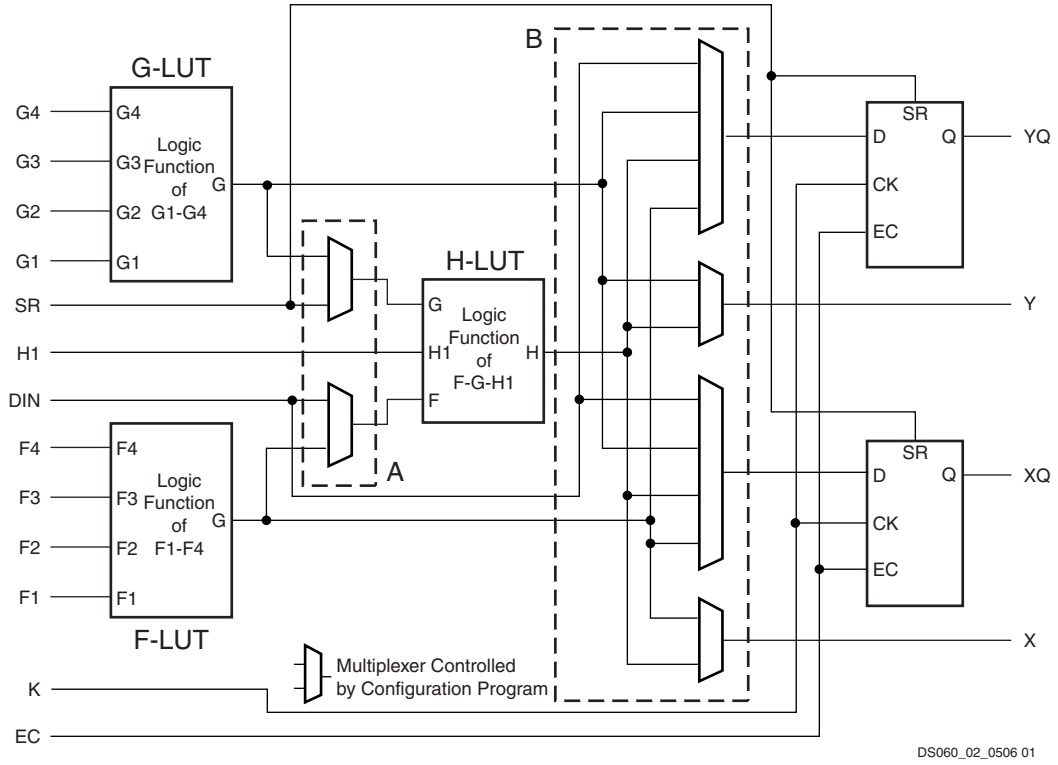



*Figure 2:* **Spartan/XL Simplified CLB Logic Diagram (some features not shown)**

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

  **Note:** When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.
- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

### *Flip-Flops*

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.

### *Latches (Spartan-XL Family Only)*

The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.

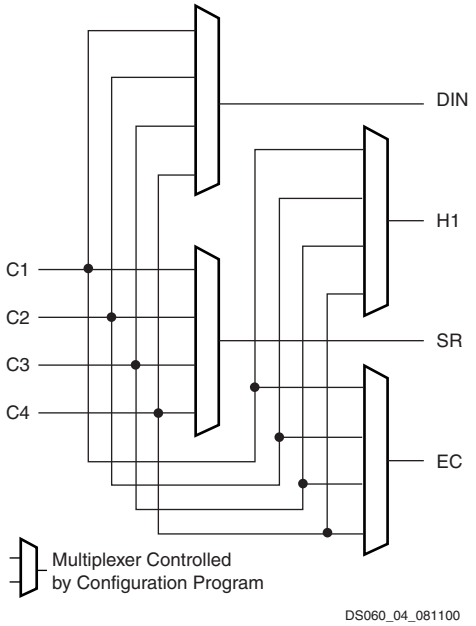



*Figure 4:* **CLB Control Signal Interface**

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

## Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

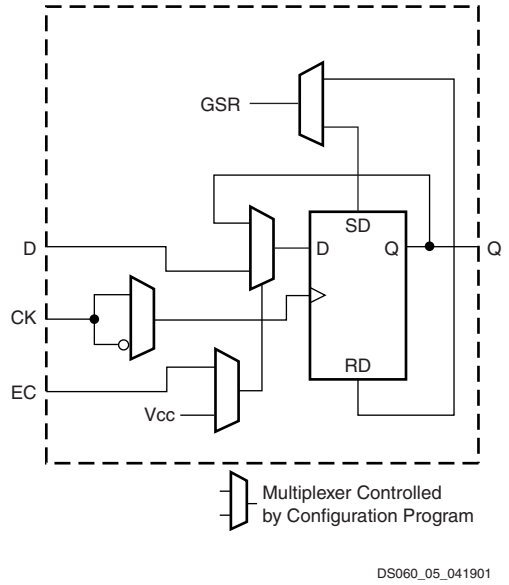



*Figure 5:* **IOB Flip-Flop/Latch Functional Block Diagram**

### *IOB Input Signal Path*

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

*Table 3:* **Input Register Functionality**

| Mode | CK | EC | D | Q |
|---|---|---|---|---|
| Power-Up or GSR | X | X | X | SR |
| Flip-Flop | ⌐ | 1* | D | D |
| | 0 | X | X | Q |
| Latch | 1 | 1* | X | Q |
| | 0 | 1* | D | D |
| Both | X | 0 | X | Q |

**Legend:**

| | |
|---|---|
| X | Don't care. |
| ⌐ | Rising edge (clock not inverted). |
| SR | Set or Reset value. Reset is default. |
| 0* | Input is Low or unconnected (default value) |
| 1* | Input is High or unconnected (default value) |

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds, using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the $V_{CC}$ is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V $V_{CC}$ can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.

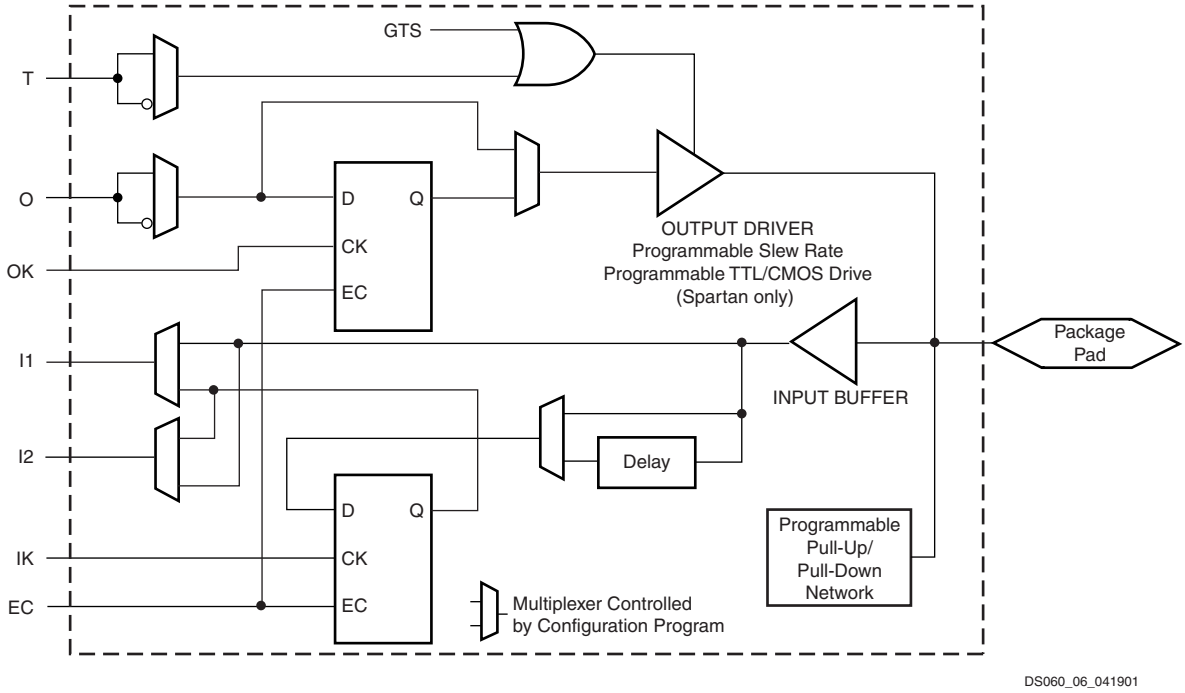



*Figure 6:* **Simplified Spartan/XL IOB Block Diagram**

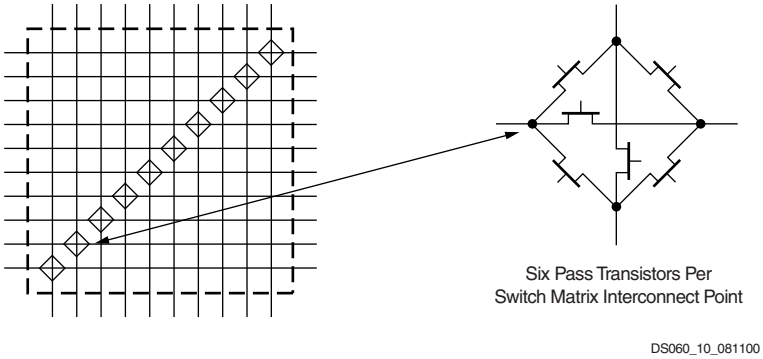



*Figure 10:* **Programmable Switch Matrix**

### Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 8).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

### Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 8. The longlines also interface to some 3-state buffers which is described later in **3-State Long Line Drivers**, page 19.

### *I/O Routing*

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

## Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 11. In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.

CLB signals from which they are originally derived are shown in Table 10.

*Table 10:* **Dual-Port RAM Signals**

| RAM Signal | Function | CLB Signal |
|---|---|---|
| D | Data In | DIN |
| A[3:0] | Read Address for Single-Port.<br>Write Address for Single-Port and Dual-Port. | F[4:1] |
| DPRA[3:0] | Read Address for Dual-Port | G[4:1] |
| WE | Write Enable | SR |
| WCLK | Clock | K |
| SPO | Single Port Out (addressed by A[3:0]) | $F_{OUT}$ |
| DPO | Dual Port Out (addressed by DPRA[3:0]) | $G_{OUT}$ |

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

### Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

### More Information on Using RAM Inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: *"Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM,"* and *"Synchronous and Asynchronous FIFO Designs."* All three application notes apply to both the Spartan and the Spartan-XL families.

## Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan

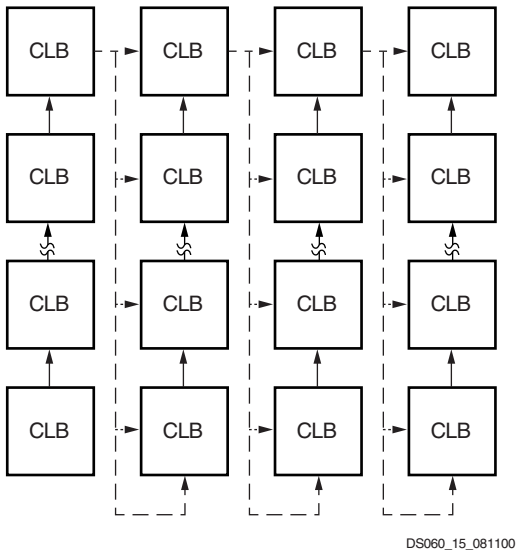



*Figure 15:* **Available Spartan/XL Carry Propagation Paths**

and Spartan-XL families, speeding up arithmetic and counting functions.

The carry chain in 5V Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in Spartan-XL devices can only run up the column, providing even higher speed.

Figure 16, page 18 shows a Spartan/XL FPGA CLB with dedicated fast carry logic. The carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 17, page 19 shows the details of the Spartan/XL FPGA carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 16.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

to wait after completing the configuration memory clear operation. When $\overline{INIT}$ is no longer held Low externally, the device determines its configuration mode by capturing the state of the Mode pins, and is ready to start the configuration process. A master device waits up to an additional 300 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{INIT}$ is High.

For more details on Configuration, refer to the Xilinx Application Note "FPGA Configuration Guidelines" (XAPP090).

### *Start-Up*

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user system. Start-up must make sure that the user logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the Global Set/Reset (GSR) at the right time.

#### Start-Up Initiation

Two conditions have to be met in order for the start-up sequence to begin:

- The chip's internal memory must be full, and
- The configuration length count must be met, exactly.

In all configuration modes except Express mode, Spartan/XL devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

In Express mode, there is no length count. The start-up sequence for each device begins when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

#### Start-Up Events

The device can be programmed to control three start-up events.

- The release of the open-drain DONE output
- The termination of the Global Three-State and the change of configuration-related pins to the user function, activating all IOBs.
- The termination of the Global Set/Reset initialization of all CLB and IOB storage elements.

Figure 31 describes start-up timing in detail. The three events — DONE going High, the internal GSR being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. This relative timing is selected by options in the bitstream generation software. Heavy lines in Figure 31 show the default timing. The thin lines indicate all other possible timing options. The start-up logic must be clocked until the "F" (Finished) state is reached.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. GSR is then released another clock period later to make sure that user operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 31, but the designer can modify it to meet particular requirements.

#### Start-Up Clock

Normally, the start-up sequence is controlled by the internal device oscillator (CCLK), which is asynchronous to the system clock. As a configuration option, they can be triggered by an on-chip user net called UCLK. This user net can be accessed by placing the STARTUP library symbol, and the start-up modes are known as UCLK_NOSYNC or UCLK_SYNC. This allows the device to wake up in synchronism with the user system.

#### DONE Pin

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to the start-up control logic. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK_SYNC or UCLK_SYNC. When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK_NOSYNC or UCLK_NOSYNC. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, while the other configuration modes can use any of the four timing sequences.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

## Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 32.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

### *Readback Options*

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

#### Readback Capture

When the Readback Capture option is selected, the data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.

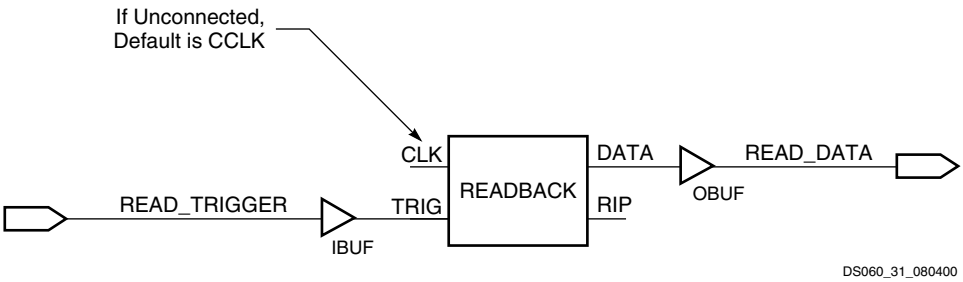



*Figure 32:* **Readback Example**

## Spartan Family DC Characteristics Over Operating Conditions

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage @ $I_{OH}$ = –4.0 mA, $V_{CC}$ min | TTL outputs | 2.4 | - | V |
| | High-level output voltage @ $I_{OH}$ = –1.0 mA, $V_{CC}$ min | CMOS outputs | $V_{CC}$ – 0.5 | - | V |
| $V_{OL}$ | Low-level output voltage @ $I_{OL}$ = 12.0 mA, $V_{CC}$ min(1) | TTL outputs | - | 0.4 | V |
| | | CMOS outputs | - | 0.4 | V |
| $V_{DR}$ | Data retention supply voltage (below which configuration data may be lost) | | 3.0 | - | V |
| $I_{CCO}$ | Quiescent FPGA supply current(2) | Commercial | - | 3.0 | mA |
| | | Industrial | - | 6.0 | mA |
| $I_L$ | Input or output leakage current | | –10 | +10 | µA |
| $C_{IN}$ | Input capacitance (sample tested) | | - | 10 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V (sample tested) | | 0.02 | 0.25 | mA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 5V (sample tested) | | 0.02 | - | mA |

**Notes:**
1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input pull-up resistors, all package pins at $V_{CC}$ or GND, and the FPGA configured with a Tie option.

## Spartan Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -4 | -3 | |
| | | | Max | Max | |
| $T_{PG}$ | From pad through Primary buffer, to any clock K | XCS05 | 2.0 | 4.0 | ns |
| | | XCS10 | 2.4 | 4.3 | ns |
| | | XCS20 | 2.8 | 5.4 | ns |
| | | XCS30 | 3.2 | 5.8 | ns |
| | | XCS40 | 3.5 | 6.4 | ns |
| $T_{SG}$ | From pad through Secondary buffer, to any clock K | XCS05 | 2.5 | 4.4 | ns |
| | | XCS10 | 2.9 | 4.7 | ns |
| | | XCS20 | 3.3 | 5.8 | ns |
| | | XCS30 | 3.6 | 6.2 | ns |
| | | XCS40 | 3.9 | 6.7 | ns |

## Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

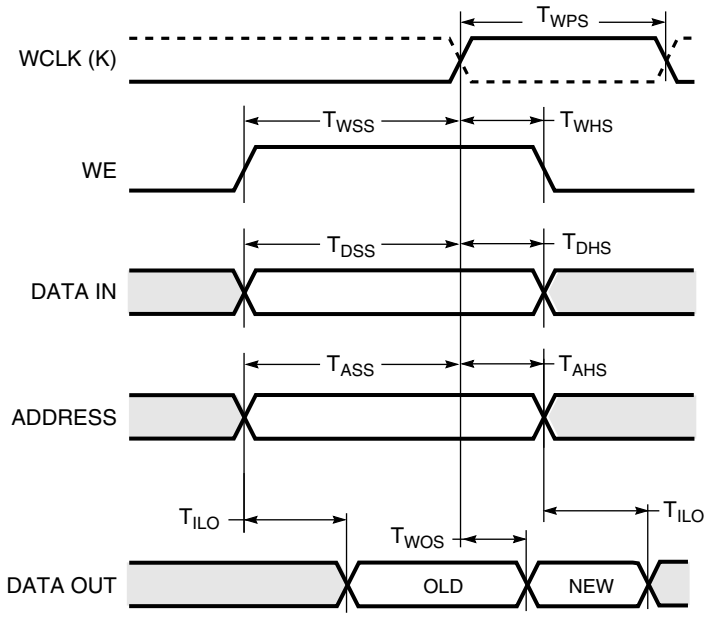
## Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

| Symbol | Dual Port RAM | Size[1] | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| **Write Operation** | | | | | | | |
| $T_{WCDS}$ | Address write cycle time (clock K period) | 16x1 | 8.0 | - | 11.6 | - | ns |
| $T_{WPDS}$ | Clock K pulse width (active edge) | 16x1 | 4.0 | - | 5.8 | - | ns |
| $T_{ASDS}$ | Address setup time before clock K | 16x1 | 1.5 | - | 2.1 | - | ns |
| $T_{AHDS}$ | Address hold time after clock K | 16x1 | 0 | - | 0 | - | ns |
| $T_{DSDS}$ | DIN setup time before clock K | 16x1 | 1.5 | - | 1.6 | - | ns |
| $T_{DHDS}$ | DIN hold time after clock K | 16x1 | 0 | - | 0 | - | ns |
| $T_{WSDS}$ | WE setup time before clock K | 16x1 | 1.5 | - | 1.6 | - | ns |
| $T_{WHDS}$ | WE hold time after clock K | 16x1 | 0 | - | 0 | - | ns |
| $T_{WODS}$ | Data valid after clock K | 16x1 | - | 6.5 | - | 7.0 | ns |

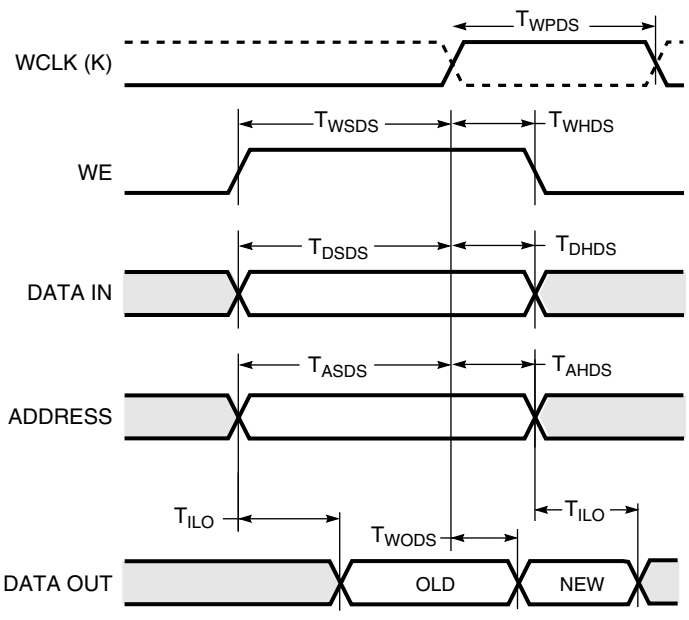
**Notes:**
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

## Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Timing

**Single Port**




**Dual Port**




DS060_34_011300

## Spartan Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -4 | | -3 | | |
| | | | Min | Max | Min | Max | |
| **Clocks** | | | | | | | |
| $T_{CH}$ | Clock High | All devices | 3.0 | - | 4.0 | - | ns |
| $T_{CL}$ | Clock Low | All devices | 3.0 | - | 4.0 | - | ns |
| **Propagation Delays - TTL Outputs(1,2)** | | | | | | | |
| $T_{OKPOF}$ | Clock (OK) to Pad, fast | All devices | - | 3.3 | - | 4.5 | ns |
| $T_{OKPOS}$ | Clock (OK to Pad, slew-rate limited | All devices | - | 6.9 | - | 7.0 | ns |
| $T_{OPF}$ | Output (O) to Pad, fast | All devices | - | 3.6 | - | 4.8 | ns |
| $T_{OPS}$ | Output (O) to Pad, slew-rate limited | All devices | - | 7.2 | - | 7.3 | ns |
| $T_{TSHZ}$ | 3-state to Pad High-Z (slew-rate independent) | All devices | - | 3.0 | - | 3.8 | ns |
| $T_{TSONF}$ | 3-state to Pad active and valid, fast | All devices | - | 6.0 | - | 7.3 | ns |
| $T_{TSONS}$ | 3-state to Pad active and valid, slew-rate limited | All devices | - | 9.6 | - | 9.8 | ns |
| **Setup and Hold Times** | | | | | | | |
| $T_{OOK}$ | Output (O) to clock (OK) setup time | All devices | 2.5 | - | 3.8 | - | ns |
| $T_{OKO}$ | Output (O) to clock (OK) hold time | All devices | 0.0 | - | 0.0 | - | ns |
| $T_{ECOK}$ | Clock Enable (EC) to clock (OK) setup time | All devices | 2.0 | - | 2.7 | - | ns |
| $T_{OKEC}$ | Clock Enable (EC) to clock (OK) hold time | All devices | 0.0 | - | 0.5 | - | ns |
| **Global Set/Reset** | | | | | | | |
| $T_{MRW}$ | Minimum GSR pulse width | All devices | 11.5 | | 13.5 | | ns |
| $T_{RPO}$ | Delay from GSR input to any Pad | XCS05 | - | 12.0 | - | 15.0 | ns |
| | | XCS10 | - | 12.5 | - | 15.7 | ns |
| | | XCS20 | - | 13.0 | - | 16.2 | ns |
| | | XCS30 | - | 13.5 | - | 16.9 | ns |
| | | XCS40 | - | 14.0 | - | 17.5 | ns |

**Notes:**

1. Delay adder for CMOS Outputs option (with fast slew rate option): for -3 speed grade, add 1.0 ns; for -4 speed grade, add 0.8 ns.
2. Delay adder for CMOS Outputs option (with slow slew rate option): for -3 speed grade, add 2.0 ns; for -4 speed grade, add 1.5 ns.
3. Output timing is measured at ~50% $V_{CC}$ threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
4. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## Spartan-XL Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -5 | -4 | |
| | | | Max | Max | |
| $T_{GLS}$ | From pad through buffer, to any clock K | XCS05XL | 1.4 | 1.5 | ns |
| | | XCS10XL | 1.7 | 1.8 | ns |
| | | XCS20XL | 2.0 | 2.1 | ns |
| | | XCS30XL | 2.3 | 2.5 | ns |
| | | XCS40XL | 2.6 | 2.8 | ns |

*Table 18:* **Pin Descriptions *(Continued)***

| Pin Name | I/O During Config. | I/O After Config. | Pin Description |
|---|---|---|---|
| SGCK1 - SGCK4 (Spartan) | Weak Pull-up (except SGCK4 is DOUT) | I or I/O | Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin.<br>The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins. |
| GCK1 - GCK8 (Spartan-XL) | Weak Pull-up (except GCK6 is DOUT) | I or I/O | Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin.<br>The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins. |
| CS1 (Spartan-XL) | I | I/O | During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining. |
| D0-D7 (Spartan-XL) | I | I/O | During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins. |
| DIN | I | I/O | During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin. |
| DOUT | O | I/O | During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input.<br>In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices.<br>After configuration, DOUT is a user-programmable I/O pin. |
| **Unrestricted User-Programmable I/O Pins** | | | |
| I/O | Weak Pull-up | I/O | These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High. |

# Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and Spartan-XL device. They follow the pad locations around the die, and include boundary scan register locations.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

## XCS05 and XCS05XL Device Pinouts

| XCS05/XL Pad Name | PC84(4) | VQ100 | Bndry Scan |
|---|---|---|---|
| VCC | P2 | P89 | - |
| I/O | P3 | P90 | 32 |
| I/O | P4 | P91 | 35 |
| I/O | - | P92 | 38 |
| I/O | - | P93 | 41 |
| I/O | P5 | P94 | 44 |
| I/O | P6 | P95 | 47 |
| I/O | P7 | P96 | 50 |
| I/O | P8 | P97 | 53 |
| I/O | P9 | P98 | 56 |
| I/O, SGCK1(1), GCK8(2) | P10 | P99 | 59 |
| VCC | P11 | P100 | - |
| GND | P12 | P1 | - |
| I/O, PGCK1(1), GCK1(2) | P13 | P2 | 62 |
| I/O | P14 | P3 | 65 |
| I/O, TDI | P15 | P4 | 68 |
| I/O, TCK | P16 | P5 | 71 |
| I/O, TMS | P17 | P6 | 74 |
| I/O | P18 | P7 | 77 |
| I/O | - | P8 | 83 |
| I/O | P19 | P9 | 86 |
| I/O | P20 | P10 | 89 |
| GND | P21 | P11 | - |
| VCC | P22 | P12 | - |
| I/O | P23 | P13 | 92 |
| I/O | P24 | P14 | 95 |
| I/O | - | P15 | 98 |
| I/O | P25 | P16 | 104 |
| I/O | P26 | P17 | 107 |
| I/O | P27 | P18 | 110 |
| I/O | - | P19 | 113 |
| I/O | P28 | P20 | 116 |
| I/O, SGCK2(1), GCK2(2) | P29 | P21 | 119 |
| Not Connected(1), M1(2) | P30 | P22 | 122 |
| GND | P31 | P23 | - |
| MODE(1), M0 (2) | P32 | P24 | 125 |
| VCC | P33 | P25 | - |

## XCS05 and XCS05XL Device Pinouts

| XCS05/XL Pad Name | PC84(4) | VQ100 | Bndry Scan |
|---|---|---|---|
| Not Connected(1), $\overline{\text{PWRDWN}}$(2) | P34 | P26 | 126(1) |
| I/O, PGCK2(1), GCK3 (2) | P35 | P27 | 127(3) |
| I/O (HDC) | P36 | P28 | 130(3) |
| I/O | - | P29 | 133(3) |
| I/O ($\overline{\text{LDC}}$) | P37 | P30 | 136(3) |
| I/O | P38 | P31 | 139(3) |
| I/O | P39 | P32 | 142(3) |
| I/O | - | P33 | 145(3) |
| I/O | - | P34 | 148(3) |
| I/O | P40 | P35 | 151(3) |
| I/O ($\overline{\text{INIT}}$) | P41 | P36 | 154(3) |
| VCC | P42 | P37 | - |
| GND | P43 | P38 | - |
| I/O | P44 | P39 | 157(3) |
| I/O | P45 | P40 | 160(3) |
| I/O | - | P41 | 163(3) |
| I/O | - | P42 | 166(3) |
| I/O | P46 | P43 | 169(3) |
| I/O | P47 | P44 | 172(3) |
| I/O | P48 | P45 | 175(3) |
| I/O | P49 | P46 | 178(3) |
| I/O | P50 | P47 | 181(3) |
| I/O, SGCK3(1), GCK4(2) | P51 | P48 | 184(3) |
| GND | P52 | P49 | - |
| DONE | P53 | P50 | - |
| VCC | P54 | P51 | - |
| $\overline{\text{PROGRAM}}$ | P55 | P52 | - |
| I/O (D7(2)) | P56 | P53 | 187(3) |
| I/O, PGCK3(1), GCK5(2) | P57 | P54 | 190(3) |
| I/O (D6(2)) | P58 | P55 | 193(3) |
| I/O | - | P56 | 196(3) |
| I/O (D5(2)) | P59 | P57 | 199(3) |
| I/O | P60 | P58 | 202(3) |
| I/O | - | P59 | 205(3) |
| I/O | - | P60 | 208(3) |
| I/O (D4(2)) | P61 | P61 | 211(3) |
| I/O | P62 | P62 | 214(3) |
| VCC | P63 | P63 | - |
| GND | P64 | P64 | - |
| I/O (D3(2)) | P65 | P65 | 217(3) |
| I/O | P66 | P66 | 220(3) |
| I/O | - | P67 | 223(3) |
| I/O (D2(2)) | P67 | P68 | 229(3) |
| I/O | P68 | P69 | 232(3) |
| I/O (D1(2)) | P69 | P70 | 235(3) |

## XCS05 and XCS05XL Device Pinouts

| XCS05/XL Pad Name | PC84[4] | VQ100 | Bndry Scan |
|---|---|---|---|
| I/O | P70 | P71 | 238[3] |
| I/O (D0[2], DIN) | P71 | P72 | 241[3] |
| I/O, SGCK4[1], GCK6[2] (DOUT) | P72 | P73 | 244[3] |
| CCLK | P73 | P74 | - |
| VCC | P74 | P75 | - |
| O, TDO | P75 | P76 | 0 |
| GND | P76 | P77 | - |
| I/O | P77 | P78 | 2 |
| I/O, PGCK4[1], GCK7[2] | P78 | P79 | 5 |
| I/O (CS1[2]) | P79 | P80 | 8 |
| I/O | P80 | P81 | 11 |
| I/O | P81 | P82 | 14 |
| I/O | P82 | P83 | 17 |
| I/O | - | P84 | 20 |
| I/O | - | P85 | 23 |
| I/O | P83 | P86 | 26 |
| I/O | P84 | P87 | 29 |
| GND | P1 | P88 | - |

**Notes:**
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS05XL is not part of the Boundary Scan chain. For the XCS05XL, subtract 1 from all Boundary Scan numbers from GCK3 on (127 and higher).
4. PC84 package discontinued by PDN2004-01

## XCS10 and XCS10XL Device Pinouts

| XCS10/XL Pad Name | PC84[4] | VQ100 | CS144[2,4] | TQ144 | Bndry Scan |
|---|---|---|---|---|---|
| VCC | P2 | P89 | D7 | P128 | - |
| I/O | P3 | P90 | A6 | P129 | 44 |
| I/O | P4 | P91 | B6 | P130 | 47 |
| I/O | - | P92 | C6 | P131 | 50 |
| I/O | - | P93 | D6 | P132 | 53 |
| I/O | P5 | P94 | A5 | P133 | 56 |
| I/O | P6 | P95 | B5 | P134 | 59 |
| I/O | - | - | C5 | P135 | 62 |
| I/O | - | - | D5 | P136 | 65 |
| GND | - | - | A4 | P137 | - |
| I/O | P7 | P96 | B4 | P138 | 68 |
| I/O | P8 | P97 | C4 | P139 | 71 |
| I/O | - | - | A3 | P140 | 74 |
| I/O | - | - | B3 | P141 | 77 |
| I/O | P9 | P98 | C3 | P142 | 80 |

## XCS10 and XCS10XL Device Pinouts

| XCS10/XL Pad Name | PC84[4] | VQ100 | CS144[2,4] | TQ144 | Bndry Scan |
|---|---|---|---|---|---|
| I/O, SGCK1[1] GCK8[2] | P10 | P99 | A2 | P143 | 83 |
| VCC | P11 | P100 | B2 | P144 | - |
| GND | P12 | P1 | A1 | P1 | - |
| I/O, PGCK1[1] GCK1[2] | P13 | P2 | B1 | P2 | 86 |
| I/O | P14 | P3 | C2 | P3 | 89 |
| I/O | - | - | C1 | P4 | 92 |
| I/O | - | - | D4 | P5 | 95 |
| I/O, TDI | P15 | P4 | D3 | P6 | 98 |
| I/O, TCK | P16 | P5 | D2 | P7 | 101 |
| GND | - | - | D1 | P8 | - |
| I/O | - | - | E4 | P9 | 104 |
| I/O | - | - | E3 | P10 | 107 |
| I/O, TMS | P17 | P6 | E2 | P11 | 110 |
| I/O | P18 | P7 | E1 | P12 | 113 |
| I/O | - | - | F4 | P13 | 116 |
| I/O | - | P8 | F3 | P14 | 119 |
| I/O | P19 | P9 | F2 | P15 | 122 |
| I/O | P20 | P10 | F1 | P16 | 125 |
| GND | P21 | P11 | G2 | P17 | - |
| VCC | P22 | P12 | G1 | P18 | - |
| I/O | P23 | P13 | G3 | P19 | 128 |
| I/O | P24 | P14 | G4 | P20 | 131 |
| I/O | - | P15 | H1 | P21 | 134 |
| I/O | - | - | H2 | P22 | 137 |
| I/O | P25 | P16 | H3 | P23 | 140 |
| I/O | P26 | P17 | H4 | P24 | 143 |
| I/O | - | - | J1 | P25 | 146 |
| I/O | - | - | J2 | P26 | 149 |
| GND | - | - | J3 | P27 | - |
| I/O | P27 | P18 | J4 | P28 | 152 |
| I/O | - | P19 | K1 | P29 | 155 |
| I/O | - | - | K2 | P30 | 158 |
| I/O | - | - | K3 | P31 | 161 |
| I/O | P28 | P20 | L1 | P32 | 164 |
| I/O, SGCK2[1] GCK2[2] | P29 | P21 | L2 | P33 | 167 |
| Not Connect-ed[1] M1[2] | P30 | P22 | L3 | P34 | 170 |
| GND | P31 | P23 | M1 | P35 | - |
| MODE[1], M0[2] | P32 | P24 | M2 | P36 | 173 |

### *Additional XCS20/XL Package Pins*

| PQ208 | | | | | |
|---|---|---|---|---|---|
| Not Connected Pins | | | | | |
| P12 | P18 (1) | P33 (1) | P39 | P65 | P71 (1) |
| P86 (1) | P92 | P111 | P121(1) | P140(1) | P144 |
| P165 | P173(1) | P192(1) | P202 | P203 | - |
| 9/16/98 | | | | | |

**Notes:**
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by PDN2004-01

## XCS30 and XCS30XL Device Pinouts

| XCS30/XL Pad Name | VQ100(5) | TQ144 | PQ208 | PQ240 | BG256(5) | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|---|---|
| VCC | P89 | P128 | P183 | P212 | VCC(4) | C10 | - |
| I/O | P90 | P129 | P184 | P213 | C10 | D10 | 74 |
| I/O | P91 | P130 | P185 | P214 | D10 | E10 | 77 |
| I/O | P92 | P131 | P186 | P215 | A9 | A9 | 80 |
| I/O | P93 | P132 | P187 | P216 | B9 | B9 | 83 |
| I/O | - | - | P188 | P217 | C9 | C9 | 86 |
| I/O | - | - | P189 | P218 | D9 | D9 | 89 |
| I/O | P94 | P133 | P190 | P220 | A8 | A8 | 92 |
| I/O | P95 | P134 | P191 | P221 | B8 | B8 | 95 |
| VCC | - | - | P192 | P222 | VCC(4) | A7 | - |
| I/O | - | - | - | P223 | A6 | B7 | 98 |
| I/O | - | - | - | P224 | C7 | C7 | 101 |
| I/O | - | P135 | P193 | P225 | B6 | D7 | 104 |
| I/O | - | P136 | P194 | P226 | A5 | A6 | 107 |
| GND | - | P137 | P195 | P227 | GND(4) | GND(4) | - |
| I/O | - | - | P196 | P228 | C6 | B6 | 110 |
| I/O | - | - | P197 | P229 | B5 | C6 | 113 |
| I/O | - | - | P198 | P230 | A4 | D6 | 116 |
| I/O | - | - | P199 | P231 | C5 | E6 | 119 |
| I/O | P96 | P138 | P200 | P232 | B4 | A5 | 122 |
| I/O | P97 | P139 | P201 | P233 | A3 | C5 | 125 |
| I/O | - | - | P202 | P234 | D5 | B4 | 128 |
| I/O | - | - | P203 | P235 | C4 | C4 | 131 |
| I/O | - | P140 | P204 | P236 | B3 | A3 | 134 |
| I/O | - | P141 | P205 | P237 | B2 | A2 | 137 |
| I/O | P98 | P142 | P206 | P238 | A2 | B3 | 140 |
| I/O, SGCK1(1), GCK8(2) | P99 | P143 | P207 | P239 | C3 | B2 | 143 |
| VCC | P100 | P144 | P208 | P240 | VCC(4) | A1 | - |
| GND | P1 | P1 | P1 | P1 | GND(4) | GND(4) | - |
| I/O, PGCK1(1), GCK1(2) | P2 | P2 | P2 | P2 | B1 | C3 | 146 |
| I/O | P3 | P3 | P3 | P3 | C2 | C2 | 149 |
| I/O | - | P4 | P4 | P4 | D2 | B1 | 152 |

## XCS30 and XCS30XL Device Pinouts *(Continued)*

| XCS30/XL Pad Name | VQ100[5] | TQ144 | PQ208 | PQ240 | BG256[5] | CS280[2,5] | Bndry Scan |
|---|---|---|---|---|---|---|---|
| I/O | - | P5 | P5 | P5 | D3 | C1 | 155 |
| I/O, TDI | P4 | P6 | P6 | P6 | E4 | D4 | 158 |
| I/O, TCK | P5 | P7 | P7 | P7 | C1 | D3 | 161 |
| I/O | - | - | P8 | P8 | D1 | E2 | 164 |
| I/O | - | - | P9 | P9 | E3 | E4 | 167 |
| I/O | - | - | P10 | P10 | E2 | E1 | 170 |
| I/O | - | - | P11 | P11 | E1 | F5 | 173 |
| I/O | - | - | P12 | P12 | F3 | F3 | 176 |
| I/O | - | - | - | P13 | F2 | F2 | 179 |
| GND | - | P8 | P13 | P14 | GND[4] | GND[4] | - |
| I/O | - | P9 | P14 | P15 | G3 | F4 | 182 |
| I/O | - | P10 | P15 | P16 | G2 | F1 | 185 |
| I/O, TMS | P6 | P11 | P16 | P17 | G1 | G3 | 188 |
| I/O | P7 | P12 | P17 | P18 | H3 | G2 | 191 |
| VCC | - | - | P18 | P19 | VCC[4] | G1 | - |
| I/O | - | - | - | P20 | H2 | G4 | 194 |
| I/O | - | - | - | P21 | H1 | H1 | 197 |
| I/O | - | - | P19 | P23 | J2 | H4 | 200 |
| I/O | - | - | P20 | P24 | J1 | J1 | 203 |
| I/O | - | P13 | P21 | P25 | K2 | J2 | 206 |
| I/O | P8 | P14 | P22 | P26 | K3 | J3 | 209 |
| I/O | P9 | P15 | P23 | P27 | K1 | J4 | 212 |
| I/O | P10 | P16 | P24 | P28 | L1 | K1 | 215 |
| GND | P11 | P17 | P25 | P29 | GND[4] | GND[4] | - |
| VCC | P12 | P18 | P26 | P30 | VCC[4] | K2 | - |
| I/O | P13 | P19 | P27 | P31 | L2 | K3 | 218 |
| I/O | P14 | P20 | P28 | P32 | L3 | K4 | 221 |
| I/O | P15 | P21 | P29 | P33 | L4 | K5 | 224 |
| I/O | - | P22 | P30 | P34 | M1 | L1 | 227 |
| I/O | - | - | P31 | P35 | M2 | L2 | 230 |
| I/O | - | - | P32 | P36 | M3 | L3 | 233 |
| I/O | - | - | - | P38 | N1 | M2 | 236 |
| I/O | - | - | - | P39 | N2 | M3 | 239 |
| VCC | - | - | P33 | P40 | VCC[4] | M4 | - |
| I/O | P16 | P23 | P34 | P41 | P1 | N1 | 242 |
| I/O | P17 | P24 | P35 | P42 | P2 | N2 | 245 |
| I/O | - | P25 | P36 | P43 | R1 | N3 | 248 |
| I/O | - | P26 | P37 | P44 | P3 | N4 | 251 |
| GND | - | P27 | P38 | P45 | GND[4] | GND[4] | - |
| I/O | - | - | - | P46 | T1 | P1 | 254 |
| I/O | - | - | P39 | P47 | R3 | P2 | 257 |
| I/O | - | - | P40 | P48 | T2 | P3 | 260 |
| I/O | - | - | P41 | P49 | U1 | P4 | 263 |
| I/O | - | - | P42 | P50 | T3 | P5 | 266 |
| I/O | - | - | P43 | P51 | U2 | R1 | 269 |

**CS280**

| VCC Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E7 | E8 | E9 | E11 | E12 |
| E13 | G5 | G15 | H5 | H15 | J5 |
| J15 | L5 | L15 | M5 | M15 | N5 |
| N15 | R7 | R8 | R9 | R11 | R12 |
| R13 | - | - | - | - | - |
| **Not Connected Pins** | | | | | |
| A4 | A12 | C8 | C12 | C15 | D1 |
| D2 | D5 | D8 | D17 | D18 | E15 |
| H2 | H3 | H18 | H19 | L4 | M1 |
| M16 | M18 | R2 | R4 | R5 | R15 |
| R17 | T8 | T15 | U5 | V8 | V12 |
| W12 | W16 | - | - | - | - |
| **Not Connected Pins (VCC in XCS40XL)** | | | | | |
| B5 | B15 | E3 | E18 | R3 | R18 |
| V5 | V15 | - | - | - | - |

5/21/02

## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| VCC | P183 | P212 | VCC(4) | VCC(4) | - |
| I/O | P184 | P213 | C10 | D10 | 86 |
| I/O | P185 | P214 | D10 | E10 | 89 |
| I/O | P186 | P215 | A9 | A9 | 92 |
| I/O | P187 | P216 | B9 | B9 | 95 |
| I/O | P188 | P217 | C9 | C9 | 98 |
| I/O | P189 | P218 | D9 | D9 | 101 |
| I/O | P190 | P220 | A8 | A8 | 104 |
| I/O | P191 | P221 | B8 | B8 | 107 |
| I/O | - | - | C8 | C8 | 110 |
| I/O | - | - | A7 | D8 | 113 |
| VCC | P192 | P222 | VCC(4) | VCC(4) | - |
| I/O | - | P223 | A6 | B7 | 116 |
| I/O | - | P224 | C7 | C7 | 119 |
| I/O | P193 | P225 | B6 | D7 | 122 |
| I/O | P194 | P226 | A5 | A6 | 125 |
| GND | P195 | P227 | GND(4) | GND(4) | - |
| I/O | P196 | P228 | C6 | B6 | 128 |
| I/O | P197 | P229 | B5 | C6 | 131 |
| I/O | P198 | P230 | A4 | D6 | 134 |
| I/O | P199 | P231 | C5 | E6 | 137 |

## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| I/O | P200 | P232 | B4 | A5 | 140 |
| I/O | P201 | P233 | A3 | C5 | 143 |
| I/O | - | - | - | D5 | 146 |
| I/O | - | - | - | A4 | 149 |
| I/O | P202 | P234 | D5 | B4 | 152 |
| I/O | P203 | P235 | C4 | C4 | 155 |
| I/O | P204 | P236 | B3 | A3 | 158 |
| I/O | P205 | P237 | B2 | A2 | 161 |
| I/O | P206 | P238 | A2 | B3 | 164 |
| I/O, SGCK1(1), GCK8(2) | P207 | P239 | C3 | B2 | 167 |
| VCC | P208 | P240 | VCC(4) | VCC(4) | - |
| GND | P1 | P1 | GND(4) | GND(4) | - |
| I/O, PGCK1(1), GCK1(2) | P2 | P2 | B1 | C3 | 170 |
| I/O | P3 | P3 | C2 | C2 | 173 |
| I/O | P4 | P4 | D2 | B1 | 176 |
| I/O | P5 | P5 | D3 | C1 | 179 |
| I/O, TDI | P6 | P6 | E4 | D4 | 182 |
| I/O, TCK | P7 | P7 | C1 | D3 | 185 |
| I/O | - | - | - | D2 | 188 |
| I/O | - | - | - | D1 | 191 |
| I/O | P8 | P8 | D1 | E2 | 194 |
| I/O | P9 | P9 | E3 | E4 | 197 |
| I/O | P10 | P10 | E2 | E1 | 200 |
| I/O | P11 | P11 | E1 | F5 | 203 |
| I/O | P12 | P12 | F3 | F3 | 206 |
| I/O | - | P13 | F2 | F2 | 209 |
| GND | P13 | P14 | GND(4) | GND(4) | - |
| I/O | P14 | P15 | G3 | F4 | 212 |
| I/O | P15 | P16 | G2 | F1 | 215 |
| I/O, TMS | P16 | P17 | G1 | G3 | 218 |
| I/O | P17 | P18 | H3 | G2 | 221 |
| VCC | P18 | P19 | VCC(4) | VCC(4) | - |
| I/O | - | P20 | H2 | G4 | 224 |
| I/O | - | P21 | H1 | H1 | 227 |
| I/O | - | - | J4 | H3 | 230 |
| I/O | - | - | J3 | H2 | 233 |
| I/O | P19 | P23 | J2 | H4 | 236 |
| I/O | P20 | P24 | J1 | J1 | 239 |
| I/O | P21 | P25 | K2 | J2 | 242 |
| I/O | P22 | P26 | K3 | J3 | 245 |
| I/O | P23 | P27 | K1 | J4 | 248 |
| I/O | P24 | P28 | L1 | K1 | 251 |

## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| GND | P25 | P29 | GND(4) | GND(4) | - |
| VCC | P26 | P30 | VCC(4) | VCC(4) | - |
| I/O | P27 | P31 | L2 | K3 | 254 |
| I/O | P28 | P32 | L3 | K4 | 257 |
| I/O | P29 | P33 | L4 | K5 | 260 |
| I/O | P30 | P34 | M1 | L1 | 263 |
| I/O | P31 | P35 | M2 | L2 | 266 |
| I/O | P32 | P36 | M3 | L3 | 269 |
| I/O | - | - | M4 | L4 | 272 |
| I/O | - | - | - | M1 | 275 |
| I/O | - | P38 | N1 | M2 | 278 |
| I/O | - | P39 | N2 | M3 | 281 |
| VCC | P33 | P40 | VCC(4) | VCC(4) | - |
| I/O | P34 | P41 | P1 | N1 | 284 |
| I/O | P35 | P42 | P2 | N2 | 287 |
| I/O | P36 | P43 | R1 | N3 | 290 |
| I/O | P37 | P44 | P3 | N4 | 293 |
| GND | P38 | P45 | GND(4) | GND(4) | - |
| I/O | - | P46 | T1 | P1 | 296 |
| I/O | P39 | P47 | R3 | P2 | 299 |
| I/O | P40 | P48 | T2 | P3 | 302 |
| I/O | P41 | P49 | U1 | P4 | 305 |
| I/O | P42 | P50 | T3 | P5 | 308 |
| I/O | P43 | P51 | U2 | R1 | 311 |
| I/O | - | - | - | R2 | 314 |
| I/O | - | - | - | R4 | 317 |
| I/O | P44 | P52 | V1 | T1 | 320 |
| I/O | P45 | P53 | T4 | T2 | 323 |
| I/O | P46 | P54 | U3 | T3 | 326 |
| I/O | P47 | P55 | V2 | U1 | 329 |
| I/O | P48 | P56 | W1 | V1 | 332 |
| I/O, SGCK2(1), GCK2 (2) | P49 | P57 | V3 | U2 | 335 |
| Not Connected(1) M1(2) | P50 | P58 | W2 | V2 | 338 |
| GND | P51 | P59 | GND(4) | GND(4) | - |
| MODE(1), M0(2) | P52 | P60 | Y1 | W1 | 341 |
| VCC | P53 | P61 | VCC(4) | VCC(4) | - |
| Not Connected(1) $\overline{\text{PWRDWN}}$(2) | P54 | P62 | W3 | V3 | 342(1) |
| I/O, PGCK2(1), GCK3(2) | P55 | P63 | Y2 | W2 | 343 (3) |

## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| I/O (HDC) | P56 | P64 | W4 | W3 | 346 (3) |
| I/O | P57 | P65 | V4 | T4 | 349 (3) |
| I/O | P58 | P66 | U5 | U4 | 352 (3) |
| I/O | P59 | P67 | Y3 | V4 | 355 (3) |
| I/O ($\overline{\text{LDC}}$) | P60 | P68 | Y4 | W4 | 358 (3) |
| I/O | - | - | - | R5 | 361 (3) |
| I/O | - | - | - | U5 | 364 (3) |
| I/O | P61 | P69 | V5 | T5 | 367 (3) |
| I/O | P62 | P70 | W5 | W5 | 370 (3) |
| I/O | P63 | P71 | Y5 | R6 | 373 (3) |
| I/O | P64 | P72 | V6 | U6 | 376 (3) |
| I/O | P65 | P73 | W6 | V6 | 379 (3) |
| I/O | - | P74 | Y6 | T6 | 382 (3) |
| GND | P66 | P75 | GND(4) | GND(4) | - |
| I/O | P67 | P76 | W7 | W6 | 385 (3) |
| I/O | P68 | P77 | Y7 | U7 | 388 (3) |
| I/O | P69 | P78 | V8 | V7 | 391 (3) |
| I/O | P70 | P79 | W8 | W7 | 394 (3) |
| VCC | P71 | P80 | VCC(4) | VCC(4) | - |
| I/O | P72 | P81 | Y8 | W8 | 397 (3) |
| I/O | P73 | P82 | U9 | U8 | 400 (3) |
| I/O | - | - | V9 | V8 | 403 (3) |
| I/O | - | - | W9 | T8 | 406 (3) |
| I/O | - | P84 | Y9 | W9 | 409 (3) |
| I/O | - | P85 | W10 | V9 | 412 (3) |
| I/O | P74 | P86 | V10 | U9 | 415 (3) |
| I/O | P75 | P87 | Y10 | T9 | 418 (3) |
| I/O | P76 | P88 | Y11 | W10 | 421 (3) |
| I/O ($\overline{\text{INIT}}$) | P77 | P89 | W11 | V10 | 424 (3) |
| VCC | P78 | P90 | VCC(4) | VCC(4) | VCC(4) |
| GND | P79 | P91 | GND(4) | GND(4) | - |
| I/O | P80 | P92 | V11 | T10 | 427 (3) |
| I/O | P81 | P93 | U11 | R10 | 430 (3) |
| I/O | P82 | P94 | Y12 | W11 | 433 (3) |
| I/O | P83 | P95 | W12 | V11 | 436 (3) |
| I/O | P84 | P96 | V12 | U11 | 439 (3) |
| I/O | P85 | P97 | U12 | T11 | 442 (3) |
| I/O | - | - | Y13 | W12 | 445 (3) |
| I/O | - | - | W13 | V12 | 448 (3) |
| I/O | - | P99 | V13 | U12 | 451 (3) |
| I/O | - | P100 | Y14 | T12 | 454 (3) |
| VCC | P86 | P101 | VCC(4) | VCC(4) | - |
| I/O | P87 | P102 | Y15 | V13 | 457 (3) |
| I/O | P88 | P103 | V14 | U13 | 460 (3) |
| I/O | P89 | P104 | W15 | T13 | 463 (3) |

## Revision History

The following table shows the revision history for this document.

| Date | Version | Description |
|---|---|---|
| 11/20/98 | 1.3 | Added Spartan-XL specs and Power Down. |
| 01/06/99 | 1.4 | All Spartan-XL -4 specs designated Preliminary with no changes. |
| 03/02/00 | 1.5 | Added CS package, updated Spartan-XL specs to Final. |
| 09/19/01 | 1.6 | Reformatted, updated power specs, clarified configuration information. Removed $T_{SOL}$ soldering information from Absolute Maximum Ratings table. Changed Figure 26: Slave Serial Mode Characteristics: $T_{CCH}$, $T_{CCL}$ from 45 to 40 ns. Changed Master Mode Configuration Switching Characteristics: $T_{CCLK}$ min. from 80 to 100 ns. Added Total Dist. RAM Bits to Table 1; added **Start-Up**, page 36 characteristics. |
| 06/27/02 | 1.7 | Clarified Express Mode pseudo daisy chain. Added new Industrial options. Clarified XCS30XL CS280 $V_{CC}$ pinout. |
| 06/26/08 | 1.8 | Noted that PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, are discontinued by **PDN2004-01**. Extended description of recommended maximum delay of reconfiguration in **Delaying Configuration After Power-Up**, page 35. Added reference to Pb-free package options and provided link to **Package Specifications**, page 81. Updated links. |
| 03/01/13 | 2.0 | The products listed in this data sheet are obsolete. See **XCN10016** and **XCN11010** for further information. |