# AMD Xilinx - XCS30-4VQ100C Datasheet

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 576 |
| Number of Logic Elements/Cells | 1368 |
| Total RAM Bits | 18432 |
| Number of I/O | 77 |
| Number of Gates | 30000 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcs30-4vq100c |

## General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in Figure 1. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.

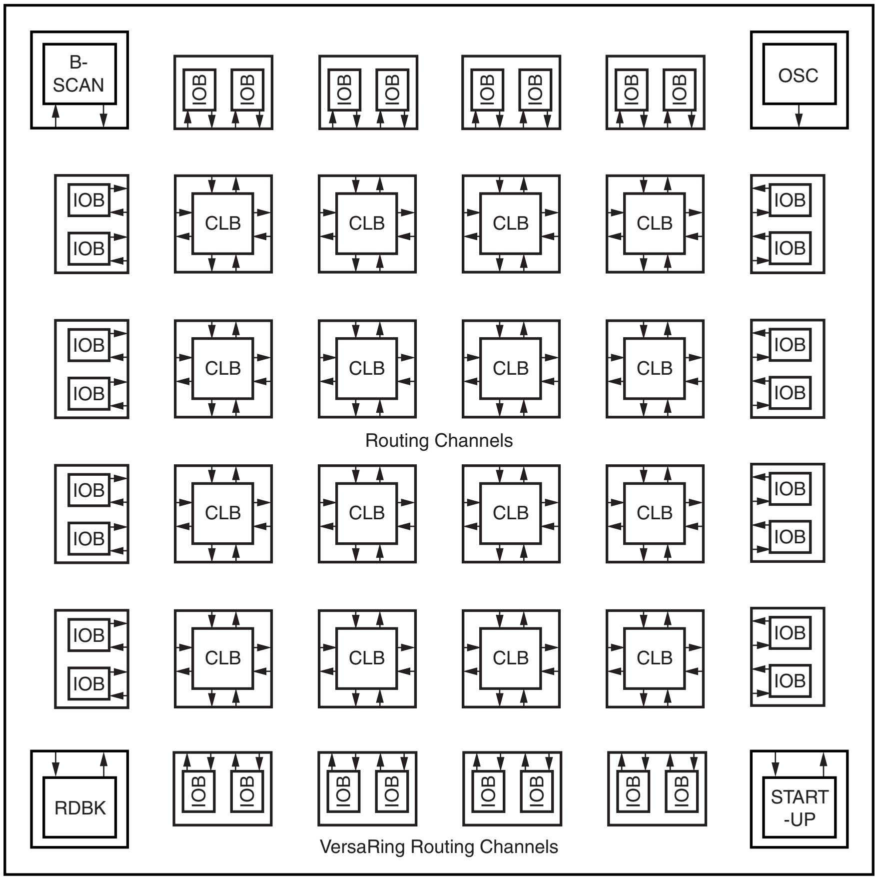

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*Figure 1:* **Basic FPGA Block Diagram**

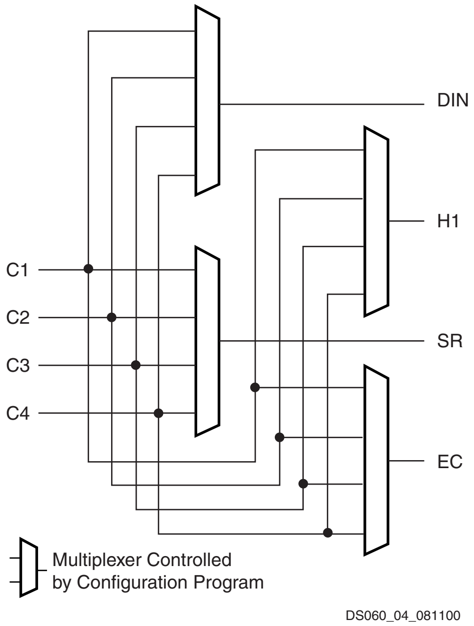


*Figure 4:* **CLB Control Signal Interface**

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

## Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

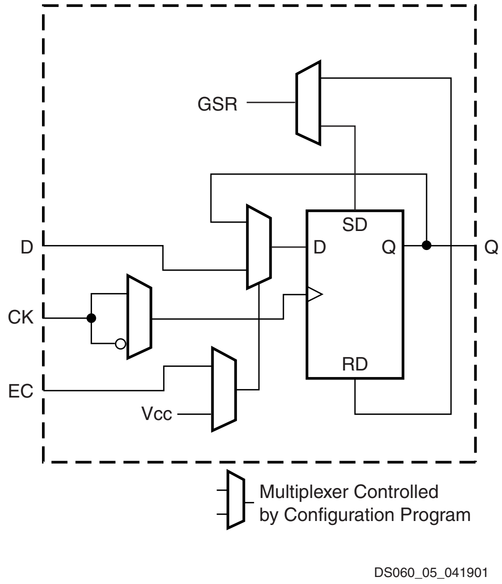


*Figure 5:* **IOB Flip-Flop/Latch Functional Block Diagram**

### IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

*Table 3:* **Input Register Functionality**

| Mode | CK | EC | D | Q |
|---|---|---|---|---|
| Power-Up or GSR | X | X | X | SR |
| Flip-Flop | ↑ | 1* | D | D |
| | 0 | X | X | Q |
| Latch | 1 | 1* | X | Q |
| | 0 | 1* | D | D |
| Both | X | 0 | X | Q |

**Legend:**

| | |
|---|---|
| X | Don't care. |
| ↑ | Rising edge (clock not inverted). |
| SR | Set or Reset value. Reset is default. |
| 0* | Input is Low or unconnected (default value) |
| 1* | Input is High or unconnected (default value) |

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds, using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the $V_{CC}$ is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V $V_{CC}$ can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.

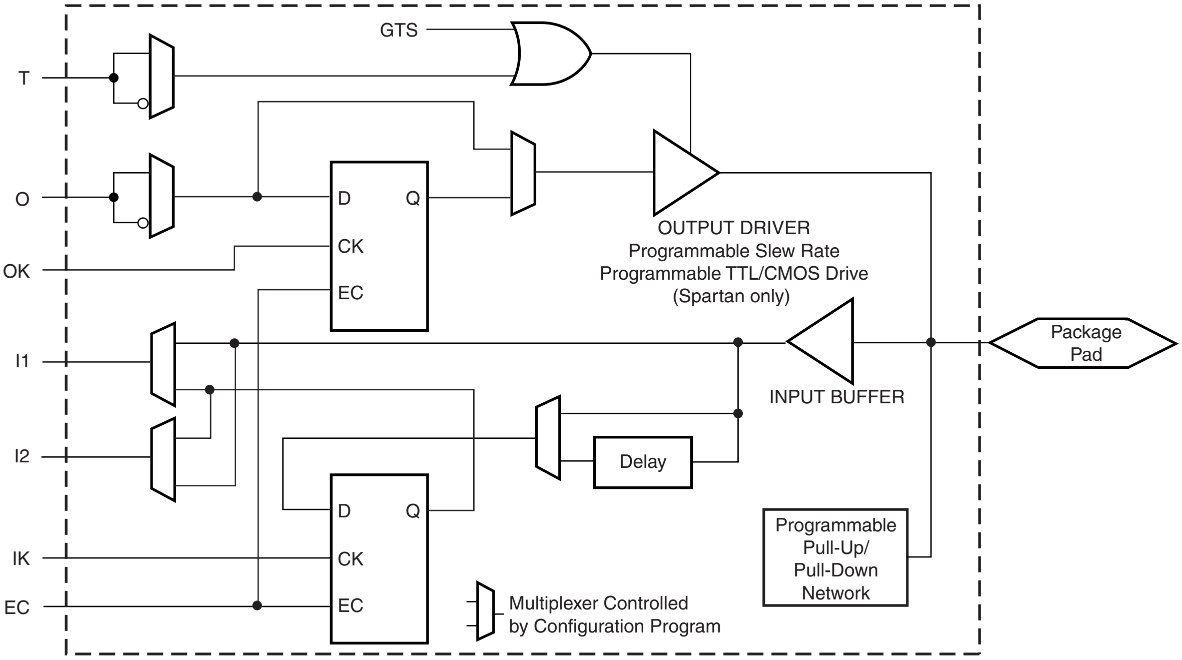


*Figure 6:* **Simplified Spartan/XL IOB Block Diagram**

- The 16 x 1 single-port configuration contains a RAM array with 16 locations, each one-bit wide. One 4-bit address decoder determines the RAM location for write and read operations. There is one input for writing data and one output for reading data, all at the selected address.
- The (16 x 1) x 2 single-port configuration combines two 16 x 1 single-port configurations (each according to the preceding description). There is one data input, one data output and one address decoder for each array. These arrays can be addressed independently.
- The 32 x 1 single-port configuration contains a RAM array with 32 locations, each one-bit wide. There is one data input, one data output, and one 5-bit address decoder.
- The dual-port mode 16 x 1 configuration contains a RAM array with 16 locations, each one-bit wide. There are two 4-bit address decoders, one for each port. One port consists of an input for writing and an output for reading, all at a selected address. The other port consists of one output for reading from an independently selected address.

The appropriate choice of RAM configuration mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Selection criteria include the following: Whereas the 32 x 1 single-port, the (16 x 1) x 2 single-port, and the 16 x 1 dual-port configurations each use one entire CLB, the 16 x 1 single-port configuration uses only one half of a CLB. Due to its simultaneous read/write capability, the dual-port RAM can transfer twice as much data as the single-port RAM, which permits only one data operation at any given time.

CLB memory configuration options are selected by using the appropriate library symbol in the design entry.

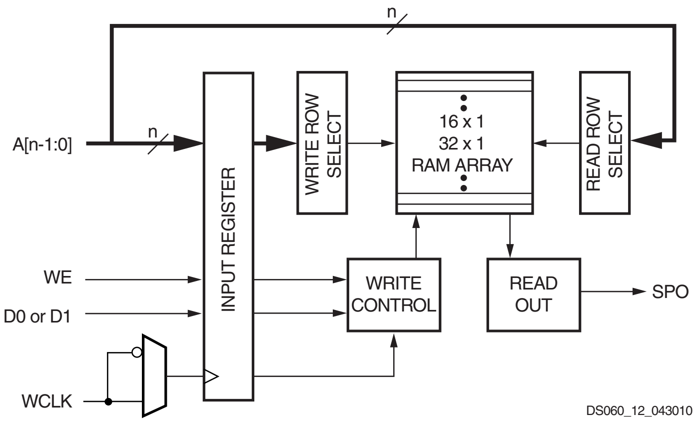
### Single-Port Mode

There are three CLB memory configurations for the single-port RAM: 16 x 1, (16 x 1) x 2, and 32 x 1, the functional organization of which is shown in Figure 12.

The single-port RAM signals and the CLB signals (Figure 2, page 4) from which they are originally derived are shown in Table 9.

*Table 9:* **Single-Port RAM Signals**

| RAM Signal | Function | CLB Signal |
|---|---|---|
| D0 or D1 | Data In | DIN or H1 |
| A[3:0] | Address | F[4:1] or G[4:1] |
| A4 (32 x 1 only) | Address | H1 |
| WE | Write Enable | SR |
| WCLK | Clock | K |
| SPO | Single Port Out (Data Out) | $F_{OUT}$ or $G_{OUT}$ |



**Notes:**

1. The (16 x 1) x 2 configuration combines two 16 x 1 single-port RAMs, each with its own independent address bus and data input. The same WE and WCLK signals are connected to both RAMs.
2. n = 4 for the 16 x 1 and (16 x 1) x 2 configurations. n = 5 for the 32 x 1 configuration.

*Figure 12:* **Logic Diagram for the Single-Port RAM**

Writing data to the single-port RAM is essentially the same as writing to a data register. It is an edge-triggered (synchronous) operation performed by applying an address to the A inputs and data to the D input during the active edge of WCLK while WE is High.

The timing relationships are shown in Figure 13. The High logic level on WE enables the input data register for writing. The active edge of WCLK latches the address, input data, and WE signals. Then, an internal write pulse is generated that loads the data into the memory cell.

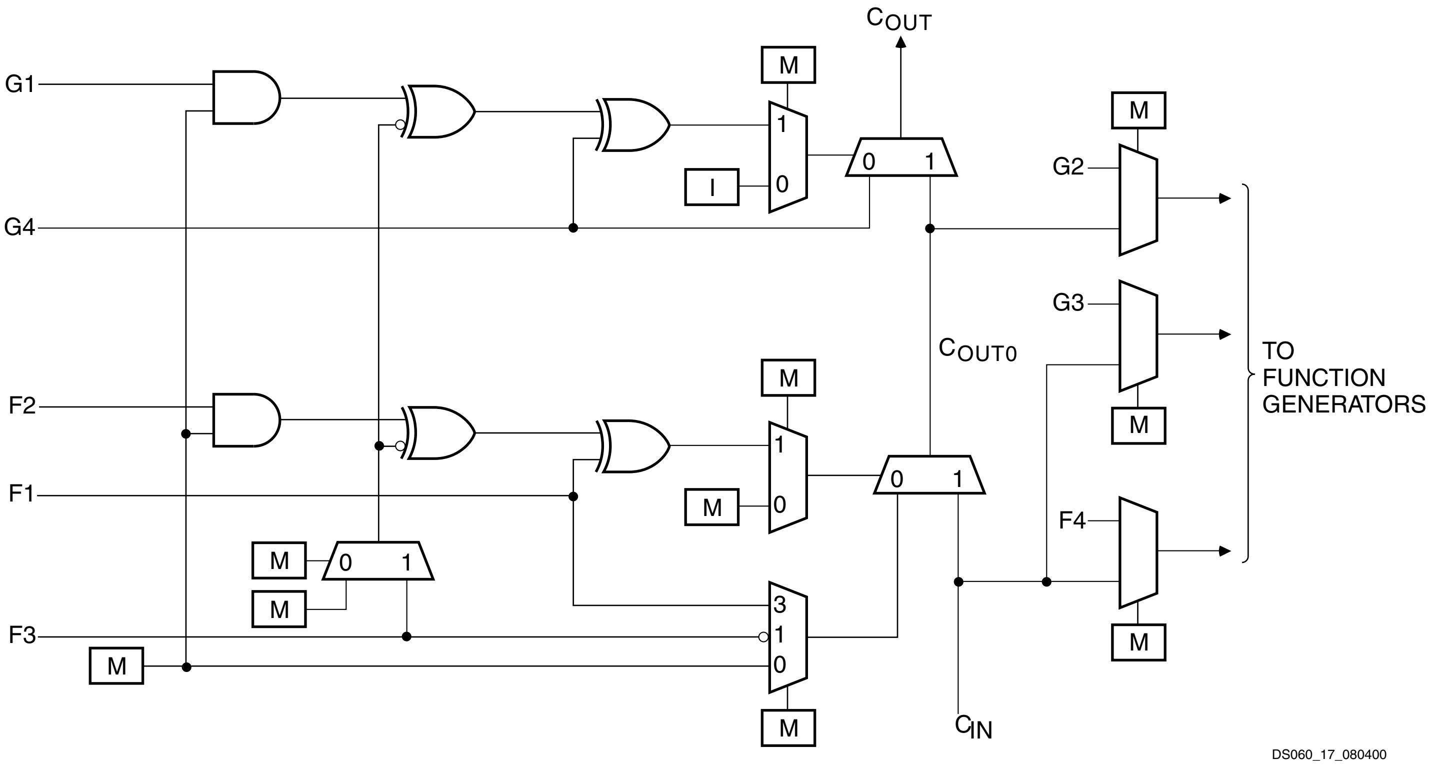


*Figure 17:* **Detail of Spartan/XL Dedicated Carry Logic**

## 3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

### Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

*Table 11:* **Three-State Buffer Functionality**

| IN | T | OUT |
|---|---|---|
| X | 1 | Z |
| IN | 0 | IN |

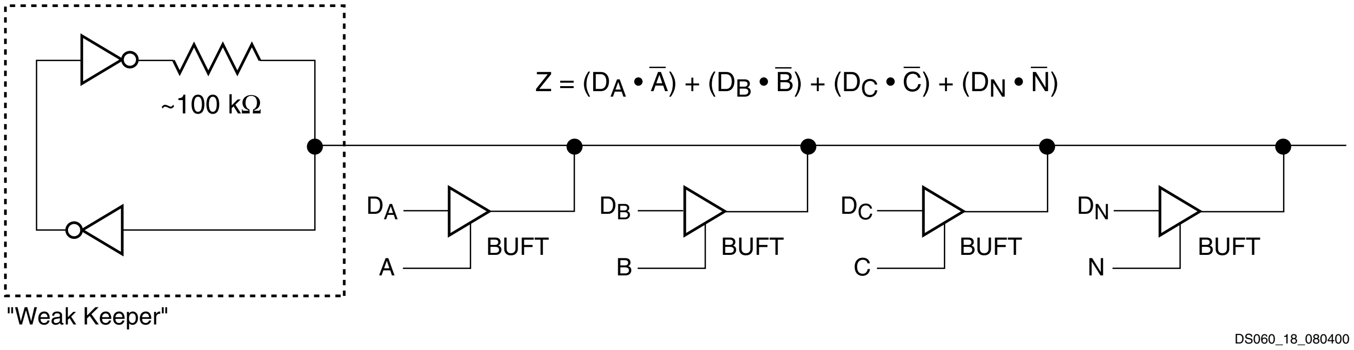


*Figure 18:* **3-state Buffers Implement a Multiplexer**

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

### *Data Registers*

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. $\overline{\text{PROGRAM}}$, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

### *Instruction Set*

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.

# Spartan Family Detailed Specifications

## Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

## Spartan Family Absolute Maximum Ratings(1)

| Symbol | Description | | Value | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND | | –0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage relative to GND(2,3) | | –0.5 to $V_{CC}$ +0.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output(2,3) | | –0.5 to $V_{CC}$ +0.5 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | °C |
| $T_J$ | Junction temperature | Plastic packages | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot (above $V_{CC}$) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Package Information on the Xilinx website.

## Spartan Family Recommended Operating Conditions

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND, $T_J$ = 0°C to +85°C | Commercial | 4.75 | 5.25 | V |
| | Supply voltage relative to GND, $T_J$ = –40°C to +100°C(1) | Industrial | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage(2) | TTL inputs | 2.0 | $V_{CC}$ | V |
| | | CMOS inputs | 70% | 100% | $V_{CC}$ |
| $V_{IL}$ | Low-level input voltage(2) | TTL inputs | 0 | 0.8 | V |
| | | CMOS inputs | 0 | 20% | $V_{CC}$ |
| $T_{IN}$ | Input signal transition time | | - | 250 | ns |

**Notes:**

1. At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

# Spartan-XL Family Detailed Specifications

## Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.
**Preliminary:** Based on preliminary characterization. Further changes are not expected.
**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

## Spartan-XL Family Absolute Maximum Ratings[1]

| Symbol | Description | | Value | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND | | –0.5 to 4.0 | V |
| $V_{IN}$ | Input voltage relative to GND | 5V Tolerant I/O Checked[2, 3] | –0.5 to 5.5 | V |
| | | Not 5V Tolerant I/Os[4, 5] | –0.5 to $V_{CC}$ + 0.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output | 5V Tolerant I/O Checked[2, 3] | –0.5 to 5.5 | V |
| | | Not 5V Tolerant I/Os[4, 5] | –0.5 to $V_{CC}$ + 0.5 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | °C |
| $T_J$ | Junction temperature | Plastic packages | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
5. Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0V or overshoot to $V_{CC}$ + 2.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Package Information on the Xilinx website.

## Spartan-XL Family Recommended Operating Conditions

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND, $T_J$ = 0°C to +85°C | Commercial | 3.0 | 3.6 | V |
| | Supply voltage relative to GND, $T_J$ = –40°C to +100°C[1] | Industrial | 3.0 | 3.6 | V |
| $V_{IH}$ | High-level input voltage[2] | | 50% of $V_{CC}$ | 5.5 | V |
| $V_{IL}$ | Low-level input voltage[2] | | 0 | 30% of $V_{CC}$ | V |
| $T_{IN}$ | Input signal transition time | | - | 250 | ns |

**Notes:**

1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold is ~50% of $V_{CC}$.

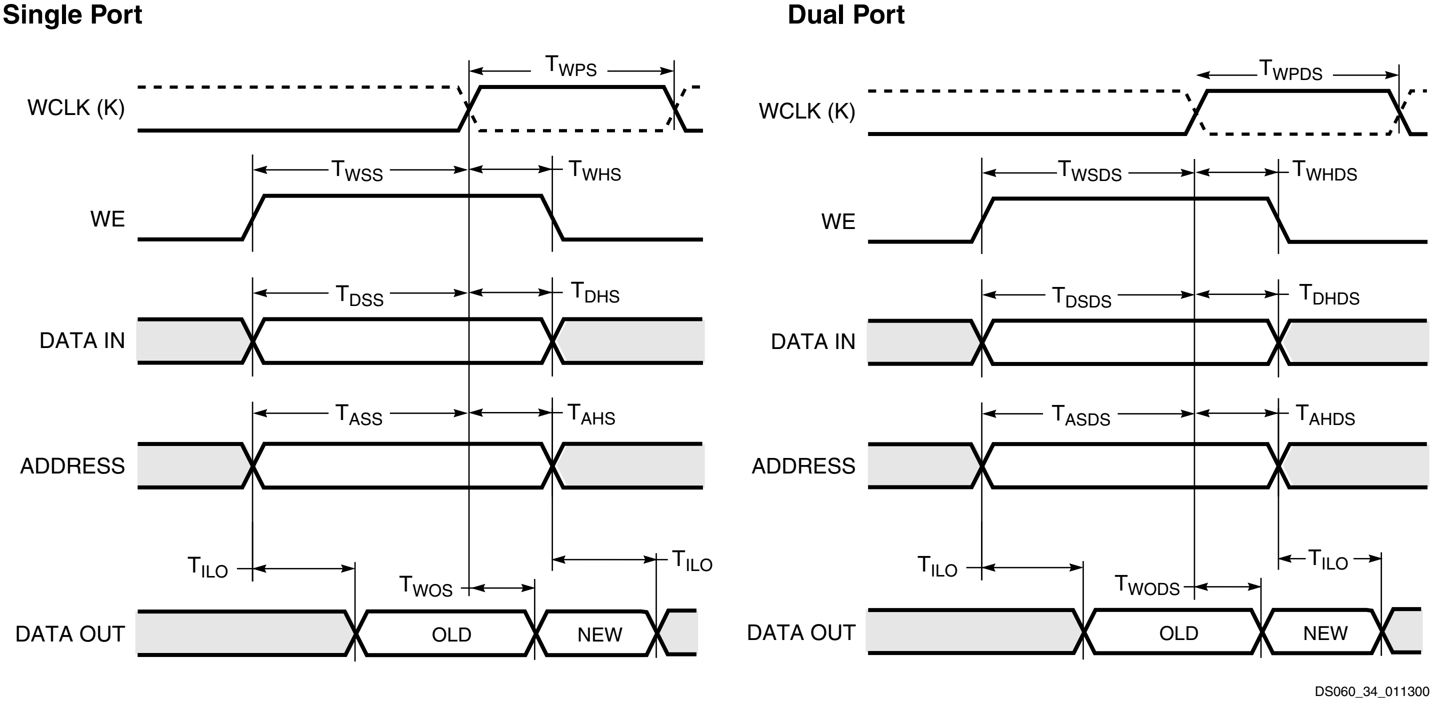
## Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

| Symbol | Dual Port RAM | Size | -5 | | -4 | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| **Write Operation[1]** | | | | | | | |
| $T_{WCDS}$ | Address write cycle time (clock K period) | 16x1 | 7.7 | - | 8.4 | - | ns |
| $T_{WPDS}$ | Clock K pulse width (active edge) | 16x1 | 3.1 | - | 3.6 | - | ns |
| $T_{ASDS}$ | Address setup time before clock K | 16x1 | 1.3 | - | 1.5 | - | ns |
| $T_{DSDS}$ | DIN setup time before clock K | 16x1 | 1.7 | - | 2.0 | - | ns |
| $T_{WSDS}$ | WE setup time before clock K | 16x1 | 1.4 | - | 1.6 | - | ns |
| | All hold times after clock K | 16x1 | 0 | - | 0 | - | ns |
| $T_{WODS}$ | Data valid after clock K | 16x1 | - | 5.2 | - | 6.1 | ns |

**Notes:**
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

## Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing



## Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

### *Spartan-XL Family Setup and Hold*

| Symbol | Description | Device | Speed Grade -5 Max | Speed Grade -4 Max | Units |
|---|---|---|---|---|---|
| **Input Setup/Hold Times Using Global Clock and IFF** | | | | | |
| $T_{SUF}/T_{HF}$ | No Delay | XCS05XL | 1.1/2.0 | 1.6/2.6 | ns |
| | | XCS10XL | 1.0/2.2 | 1.5/2.8 | ns |
| | | XCS20XL | 0.9/2.4 | 1.4/3.0 | ns |
| | | XCS30XL | 0.8/2.6 | 1.3/3.2 | ns |
| | | XCS40XL | 0.7/2.8 | 1.2/3.4 | ns |
| $T_{SU}/T_H$ | Full Delay | XCS05XL | 3.9/0.0 | 5.1/0.0 | ns |
| | | XCS10XL | 4.1/0.0 | 5.3/0.0 | ns |
| | | XCS20XL | 4.3/0.0 | 5.5/0.0 | ns |
| | | XCS30XL | 4.5/0.0 | 5.7/0.0 | ns |
| | | XCS40XL | 4.7/0.0 | 5.9/0.0 | ns |

**Notes:**

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

### Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

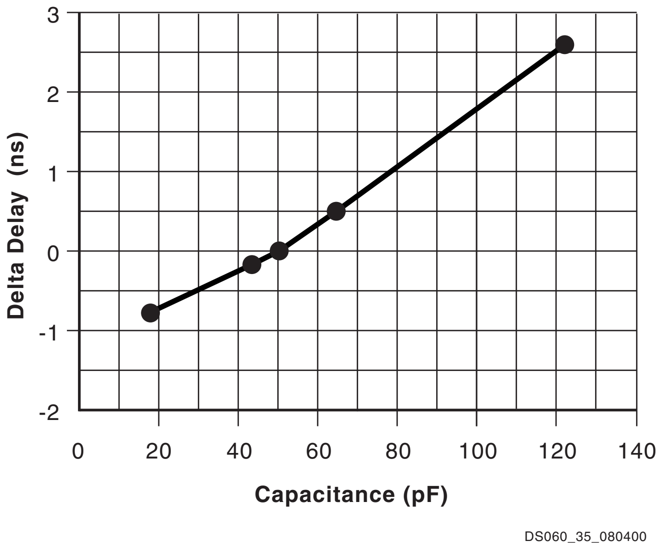


*Figure 35:* **Delay Factor at Various Capacitive Loads**

*Table 18:* **Pin Descriptions *(Continued)***

| Pin Name | I/O During Config. | I/O After Config. | Pin Description |
|---|---|---|---|
| PWRDWN | I | I | PWRDWN is an active Low input that forces the FPGA into the Power Down state and reduces power consumption. When PWRDWN is Low, the FPGA disables all I/O and initializes all flip-flops. All inputs are interpreted as Low independent of their actual level. VCC must be maintained, and the configuration data is maintained. PWRDWN halts configuration if asserted before or during configuration, and re-starts configuration when removed. When PWRDWN returns High, the FPGA becomes operational by first enabling the inputs and flip-flops and then enabling the outputs. PWRDWN has a default internal pull-up resistor. |
| **User I/O Pins That Can Have Special Functions** | | | |
| TDO | O | O | If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed.<br>To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used. |
| TDI, TCK, TMS | I | I/O or I (JTAG) | If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed.<br>If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used. |
| HDC | O | I/O | High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin. |
| LDC | O | I/O | Low During Configuration (LDC) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, LDC is a user-programmable I/O pin. |
| INIT | I/O | I/O | Before and during configuration, INIT is a bidirectional signal. A 1 kΩ to 10 kΩ external pull-up resistor is recommended.<br>As an active Low open-drain output, INIT is held Low during the power stabilization and internal clearing of the configuration memory. As an active Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after INIT has gone High.<br>During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, INIT is a user-programmable I/O pin. |
| PGCK1 - PGCK4 (Spartan) | Weak Pull-up | I or I/O | Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O.<br>The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins. |

## XCS05 and XCS05XL Device Pinouts

| XCS05/XL Pad Name | PC84(4) | VQ100 | Bndry Scan |
|---|---|---|---|
| I/O | P70 | P71 | 238(3) |
| I/O (D0(2), DIN) | P71 | P72 | 241(3) |
| I/O, SGCK4(1), GCK6(2) (DOUT) | P72 | P73 | 244(3) |
| CCLK | P73 | P74 | - |
| VCC | P74 | P75 | - |
| O, TDO | P75 | P76 | 0 |
| GND | P76 | P77 | - |
| I/O | P77 | P78 | 2 |
| I/O, PGCK4(1), GCK7(2) | P78 | P79 | 5 |
| I/O (CS1(2)) | P79 | P80 | 8 |
| I/O | P80 | P81 | 11 |
| I/O | P81 | P82 | 14 |
| I/O | P82 | P83 | 17 |
| I/O | - | P84 | 20 |
| I/O | - | P85 | 23 |
| I/O | P83 | P86 | 26 |
| I/O | P84 | P87 | 29 |
| GND | P1 | P88 | - |

**Notes:**

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS05XL is not part of the Boundary Scan chain. For the XCS05XL, subtract 1 from all Boundary Scan numbers from GCK3 on (127 and higher).
4. PC84 package discontinued by PDN2004-01

## XCS10 and XCS10XL Device Pinouts

| XCS10/XL Pad Name | PC84(4) | VQ100 | CS144(2,4) | TQ144 | Bndry Scan |
|---|---|---|---|---|---|
| VCC | P2 | P89 | D7 | P128 | - |
| I/O | P3 | P90 | A6 | P129 | 44 |
| I/O | P4 | P91 | B6 | P130 | 47 |
| I/O | - | P92 | C6 | P131 | 50 |
| I/O | - | P93 | D6 | P132 | 53 |
| I/O | P5 | P94 | A5 | P133 | 56 |
| I/O | P6 | P95 | B5 | P134 | 59 |
| I/O | - | - | C5 | P135 | 62 |
| I/O | - | - | D5 | P136 | 65 |
| GND | - | - | A4 | P137 | - |
| I/O | P7 | P96 | B4 | P138 | 68 |
| I/O | P8 | P97 | C4 | P139 | 71 |
| I/O | - | - | A3 | P140 | 74 |
| I/O | - | - | B3 | P141 | 77 |
| I/O | P9 | P98 | C3 | P142 | 80 |

## XCS10 and XCS10XL Device Pinouts

| XCS10/XL Pad Name | PC84(4) | VQ100 | CS144(2,4) | TQ144 | Bndry Scan |
|---|---|---|---|---|---|
| I/O, SGCK1(1) GCK8(2) | P10 | P99 | A2 | P143 | 83 |
| VCC | P11 | P100 | B2 | P144 | - |
| GND | P12 | P1 | A1 | P1 | - |
| I/O, PGCK1(1) GCK1(2) | P13 | P2 | B1 | P2 | 86 |
| I/O | P14 | P3 | C2 | P3 | 89 |
| I/O | - | - | C1 | P4 | 92 |
| I/O | - | - | D4 | P5 | 95 |
| I/O, TDI | P15 | P4 | D3 | P6 | 98 |
| I/O, TCK | P16 | P5 | D2 | P7 | 101 |
| GND | - | - | D1 | P8 | - |
| I/O | - | - | E4 | P9 | 104 |
| I/O | - | - | E3 | P10 | 107 |
| I/O, TMS | P17 | P6 | E2 | P11 | 110 |
| I/O | P18 | P7 | E1 | P12 | 113 |
| I/O | - | - | F4 | P13 | 116 |
| I/O | - | P8 | F3 | P14 | 119 |
| I/O | P19 | P9 | F2 | P15 | 122 |
| I/O | P20 | P10 | F1 | P16 | 125 |
| GND | P21 | P11 | G2 | P17 | - |
| VCC | P22 | P12 | G1 | P18 | - |
| I/O | P23 | P13 | G3 | P19 | 128 |
| I/O | P24 | P14 | G4 | P20 | 131 |
| I/O | - | P15 | H1 | P21 | 134 |
| I/O | - | - | H2 | P22 | 137 |
| I/O | P25 | P16 | H3 | P23 | 140 |
| I/O | P26 | P17 | H4 | P24 | 143 |
| I/O | - | - | J1 | P25 | 146 |
| I/O | - | - | J2 | P26 | 149 |
| GND | - | - | J3 | P27 | - |
| I/O | P27 | P18 | J4 | P28 | 152 |
| I/O | - | P19 | K1 | P29 | 155 |
| I/O | - | - | K2 | P30 | 158 |
| I/O | - | - | K3 | P31 | 161 |
| I/O | P28 | P20 | L1 | P32 | 164 |
| I/O, SGCK2(1) GCK2(2) | P29 | P21 | L2 | P33 | 167 |
| Not Connected(1) M1(2) | P30 | P22 | L3 | P34 | 170 |
| GND | P31 | P23 | M1 | P35 | - |
| MODE(1), M0(2) | P32 | P24 | M2 | P36 | 173 |

## XCS10 and XCS10XL Device Pinouts

| XCS10/XL Pad Name | PC84(4) | VQ100 | CS144(2,4) | TQ144 | Bndry Scan |
|---|---|---|---|---|---|
| VCC | P33 | P25 | N1 | P37 | - |
| Not Connected(1)<br>$\overline{\text{PWRDWN}}$(2) | P34 | P26 | N2 | P38 | 174 (1) |
| I/O, PGCK2(1) GCK3(2) | P35 | P27 | M3 | P39 | 175(3) |
| I/O (HDC) | P36 | P28 | N3 | P40 | 178 (3) |
| I/O | - | - | K4 | P41 | 181 (3) |
| I/O | - | - | L4 | P42 | 184 (3) |
| I/O | - | P29 | M4 | P43 | 187 (3) |
| I/O ($\overline{\text{LDC}}$) | P37 | P30 | N4 | P44 | 190 (3) |
| GND | - | - | K5 | P45 | - |
| I/O | - | - | L5 | P46 | 193 (3) |
| I/O | - | - | M5 | P47 | 196 (3) |
| I/O | P38 | P31 | N5 | P48 | 199 (3) |
| I/O | P39 | P32 | K6 | P49 | 202 (3) |
| I/O | - | P33 | L6 | P50 | 205 (3) |
| I/O | - | P34 | M6 | P51 | 208 (3) |
| I/O | P40 | P35 | N6 | P52 | 211 (3) |
| I/O ($\overline{\text{INIT}}$) | P41 | P36 | M7 | P53 | 214 (3) |
| VCC | P42 | P37 | N7 | P54 | - |
| GND | P43 | P38 | L7 | P55 | - |
| I/O | P44 | P39 | K7 | P56 | 217 (3) |
| I/O | P45 | P40 | N8 | P57 | 220 (3) |
| I/O | - | P41 | M8 | P58 | 223 (3) |
| I/O | - | P42 | L8 | P59 | 226 (3) |
| I/O | P46 | P43 | K8 | P60 | 229 (3) |
| I/O | P47 | P44 | N9 | P61 | 232 (3) |
| I/O | - | - | M9 | P62 | 235 (3) |
| I/O | - | - | L9 | P63 | 238 (3) |
| GND | - | - | K9 | P64 | - |
| I/O | P48 | P45 | N10 | P65 | 241 (3) |
| I/O | P49 | P46 | M10 | P66 | 244 (3) |
| I/O | - | - | L10 | P67 | 247 (3) |
| I/O | - | - | N11 | P68 | 250 (3) |
| I/O | P50 | P47 | M11 | P69 | 253 (3) |
| I/O, SGCK3(1) GCK4(2) | P51 | P48 | L11 | P70 | 256 (3) |
| GND | P52 | P49 | N12 | P71 | - |
| DONE | P53 | P50 | M12 | P72 | - |
| VCC | P54 | P51 | N13 | P73 | - |
| $\overline{\text{PROGRAM}}$ | P55 | P52 | M13 | P74 | - |
| I/O (D7(2)) | P56 | P53 | L12 | P75 | 259 (3) |

## XCS10 and XCS10XL Device Pinouts

| XCS10/XL Pad Name | PC84(4) | VQ100 | CS144(2,4) | TQ144 | Bndry Scan |
|---|---|---|---|---|---|
| I/O, PGCK3(1) GCK5(2) | P57 | P54 | L13 | P76 | 262 (3) |
| I/O | - | - | K10 | P77 | 265 (3) |
| I/O | - | - | K11 | P78 | 268 (3) |
| I/O (D6(2)) | P58 | P55 | K12 | P79 | 271 (3) |
| I/O | - | P56 | K13 | P80 | 274 (3) |
| GND | - | - | J10 | P81 | - |
| I/O | - | - | J11 | P82 | 277 (3) |
| I/O | - | - | J12 | P83 | 280 (3) |
| I/O (D5(2)) | P59 | P57 | J13 | P84 | 283 (3) |
| I/O | P60 | P58 | H10 | P85 | 286 (3) |
| I/O | - | P59 | H11 | P86 | 289 (3) |
| I/O | - | P60 | H12 | P87 | 292 (3) |
| I/O (D4(2)) | P61 | P61 | H13 | P88 | 295 (3) |
| I/O | P62 | P62 | G12 | P89 | 298 (3) |
| VCC | P63 | P63 | G13 | P90 | - |
| GND | P64 | P64 | G11 | P91 | - |
| I/O (D3(2)) | P65 | P65 | G10 | P92 | 301 (3) |
| I/O | P66 | P66 | F13 | P93 | 304 (3) |
| I/O | - | P67 | F12 | P94 | 307 (3) |
| I/O | - | - | F11 | P95 | 310 (3) |
| I/O (D2(2)) | P67 | P68 | F10 | P96 | 313 (3) |
| I/O | P68 | P69 | E13 | P97 | 316 (3) |
| I/O | - | - | E12 | P98 | 319 (3) |
| I/O | - | - | E11 | P99 | 322 (3) |
| GND | - | - | E10 | P100 | - |
| I/O (D1(2)) | P69 | P70 | D13 | P101 | 325 (3) |
| I/O | P70 | P71 | D12 | P102 | 328 (3) |
| I/O | - | - | D11 | P103 | 331 (3) |
| I/O | - | - | C13 | P104 | 334 (3) |
| I/O (D0(2), DIN) | P71 | P72 | C12 | P105 | 337 (3) |
| I/O, SGCK4(1) GCK6(2) (DOUT) | P72 | P73 | C11 | P106 | 340 (3) |
| CCLK | P73 | P74 | B13 | P107 | - |
| VCC | P74 | P75 | B12 | P108 | - |
| O, TDO | P75 | P76 | A13 | P109 | 0 |
| GND | P76 | P77 | A12 | P110 | - |
| I/O | P77 | P78 | B11 | P111 | 2 |
| I/O, PGCK4(1) GCK7(2) | P78 | P79 | A11 | P112 | 5 |
| I/O | - | - | D10 | P113 | 8 |
| I/O | - | - | C10 | P114 | 11 |
| I/O (CS1(2)) | P79 | P80 | B10 | P115 | 14 |

## XCS20 and XCS20XL Device Pinouts

| XCS20/XL Pad Name | VQ100 | CS144(2,4) | TQ144 | PQ208 | Bndry Scan |
|---|---|---|---|---|---|
| I/O | - | F4 | P13 | P21 | 170 |
| I/O | P8 | F3 | P14 | P22 | 173 |
| I/O | P9 | F2 | P15 | P23 | 176 |
| I/O | P10 | F1 | P16 | P24 | 179 |
| GND | P11 | G2 | P17 | P25 | - |
| VCC | P12 | G1 | P18 | P26 | - |
| I/O | P13 | G3 | P19 | P27 | 182 |
| I/O | P14 | G4 | P20 | P28 | 185 |
| I/O | P15 | H1 | P21 | P29 | 188 |
| I/O | - | H2 | P22 | P30 | 191 |
| I/O | - | - | - | P31 | 194 |
| I/O | - | - | - | P32 | 197 |
| VCC(2) | - | - | - | P33 | - |
| I/O | P16 | H3 | P23 | P34 | 200 |
| I/O | P17 | H4 | P24 | P35 | 203 |
| I/O | - | J1 | P25 | P36 | 206 |
| I/O | - | J2 | P26 | P37 | 209 |
| GND | - | J3 | P27 | P38 | - |
| I/O | - | - | - | P40 | 212 |
| I/O | - | - | - | P41 | 215 |
| I/O | - | - | - | P42 | 218 |
| I/O | - | - | - | P43 | 221 |
| I/O | P18 | J4 | P28 | P44 | 224 |
| I/O | P19 | K1 | P29 | P45 | 227 |
| I/O | - | K2 | P30 | P46 | 230 |
| I/O | - | K3 | P31 | P47 | 233 |
| I/O | P20 | L1 | P32 | P48 | 236 |
| I/O, SGCK2(1), GCK2(2) | P21 | L2 | P33 | P49 | 239 |
| Not Connected(1) M1(2) | P22 | L3 | P34 | P50 | 242 |
| GND | P23 | M1 | P35 | P51 | - |
| MODE(1), M0(2) | P24 | M2 | P36 | P52 | 245 |
| VCC | P25 | N1 | P37 | P53 | - |
| Not Connected(1) $\overline{\text{PWRDWN}}$(2) | P26 | N2 | P38 | P54 | 246 (1) |
| I/O, PGCK2(1), GCK3(2) | P27 | M3 | P39 | P55 | 247 (3) |
| I/O (HDC) | P28 | N3 | P40 | P56 | 250 (3) |
| I/O | - | K4 | P41 | P57 | 253 (3) |
| I/O | - | L4 | P42 | P58 | 256 (3) |
| I/O | P29 | M4 | P43 | P59 | 259 (3) |

## XCS20 and XCS20XL Device Pinouts

| XCS20/XL Pad Name | VQ100 | CS144(2,4) | TQ144 | PQ208 | Bndry Scan |
|---|---|---|---|---|---|
| I/O ($\overline{\text{LDC}}$) | P30 | N4 | P44 | P60 | 262 (3) |
| I/O | - | - | - | P61 | 265 (3) |
| I/O | - | - | - | P62 | 268 (3) |
| I/O | - | - | - | P63 | 271 (3) |
| I/O | - | - | - | P64 | 274 (3) |
| GND | - | K5 | P45 | P66 | - |
| I/O | - | L5 | P46 | P67 | 277 (3) |
| I/O | - | M5 | P47 | P68 | 280 (3) |
| I/O | P31 | N5 | P48 | P69 | 283 (3) |
| I/O | P32 | K6 | P49 | P70 | 286 (3) |
| VCC(2) | - | - | - | P71 | - |
| I/O | - | - | - | P72 | 289 (3) |
| I/O | - | - | - | P73 | 292 (3) |
| I/O | P33 | L6 | P50 | P74 | 295 (3) |
| I/O | P34 | M6 | P51 | P75 | 298 (3) |
| I/O | P35 | N6 | P52 | P76 | 301 (3) |
| I/O ($\overline{\text{INIT}}$) | P36 | M7 | P53 | P77 | 304 (3) |
| VCC | P37 | N7 | P54 | P78 | - |
| GND | P38 | L7 | P55 | P79 | - |
| I/O | P39 | K7 | P56 | P80 | 307 (3) |
| I/O | P40 | N8 | P57 | P81 | 310 (3) |
| I/O | P41 | M8 | P58 | P82 | 313 (3) |
| I/O | P42 | L8 | P59 | P83 | 316 (3) |
| I/O | - | - | - | P84 | 319 (3) |
| I/O | - | - | - | P85 | 322 (3) |
| VCC(2) | - | - | - | P86 | - |
| I/O | P43 | K8 | P60 | P87 | 325 (3) |
| I/O | P44 | N9 | P61 | P88 | 328 (3) |
| I/O | - | M9 | P62 | P89 | 331 (3) |
| I/O | - | L9 | P63 | P90 | 334 (3) |
| GND | - | K9 | P64 | P91 | - |
| I/O | - | - | - | P93 | 337 (3) |
| I/O | - | - | - | P94 | 340 (3) |
| I/O | - | - | - | P95 | 343 (3) |
| I/O | - | - | - | P96 | 346 (3) |
| I/O | P45 | N10 | P65 | P97 | 349 (3) |
| I/O | P46 | M10 | P66 | P98 | 352 (3) |
| I/O | - | L10 | P67 | P99 | 355 (3) |
| I/O | - | N11 | P68 | P100 | 358 (3) |
| I/O | P47 | M11 | P69 | P101 | 361 (3) |
| I/O, SGCK3(1), GCK4(2) | P48 | L11 | P70 | P102 | 364 (3) |
| GND | P49 | N12 | P71 | P103 | - |
| DONE | P50 | M12 | P72 | P104 | - |
| VCC | P51 | N13 | P73 | P105 | - |

## XCS20 and XCS20XL Device Pinouts

| XCS20/XL Pad Name | VQ100 | CS144(2,4) | TQ144 | PQ208 | Bndry Scan |
|---|---|---|---|---|---|
| PROGRAM | P52 | M13 | P74 | P106 | - |
| I/O (D7(2)) | P53 | L12 | P75 | P107 | 367 (3) |
| I/O, PGCK3(1), GCK5(2) | P54 | L13 | P76 | P108 | 370 (3) |
| I/O | - | K10 | P77 | P109 | 373 (3) |
| I/O | - | K11 | P78 | P110 | 376 (3) |
| I/O (D6(2)) | P55 | K12 | P79 | P112 | 379 (3) |
| I/O | P56 | K13 | P80 | P113 | 382 (3) |
| I/O | - | - | - | P114 | 385 (3) |
| I/O | - | - | - | P115 | 388 (3) |
| I/O | - | - | - | P116 | 391 (3) |
| I/O | - | - | - | P117 | 394 (3) |
| GND | - | J10 | P81 | P118 | - |
| I/O | - | J11 | P82 | P119 | 397 (3) |
| I/O | - | J12 | P83 | P120 | 400 (3) |
| VCC(2) | - | - | - | P121 | - |
| I/O (D5(2)) | P57 | J13 | P84 | P122 | 403 (3) |
| I/O | P58 | H10 | P85 | P123 | 406 (3) |
| I/O | - | - | - | P124 | 409 (3) |
| I/O | - | - | - | P125 | 412 (3) |
| I/O | P59 | H11 | P86 | P126 | 415 (3) |
| I/O | P60 | H12 | P87 | P127 | 418 (3) |
| I/O (D4(2)) | P61 | H13 | P88 | P128 | 421 (3) |
| I/O | P62 | G12 | P89 | P129 | 424 (3) |
| VCC | P63 | G13 | P90 | P130 | - |
| GND | P64 | G11 | P91 | P131 | - |
| I/O (D3(2)) | P65 | G10 | P92 | P132 | 427 (3) |
| I/O | P66 | F13 | P93 | P133 | 430 (3) |
| I/O | P67 | F12 | P94 | P134 | 433 (3) |
| I/O | - | F11 | P95 | P135 | 436 (3) |
| I/O | - | - | - | P136 | 439 (3) |
| I/O | - | - | - | P137 | 442 (3) |
| I/O (D2(2)) | P68 | F10 | P96 | P138 | 445 (3) |
| I/O | P69 | E13 | P97 | P139 | 448 (3) |
| VCC(2) | - | - | - | P140 | - |
| I/O | - | E12 | P98 | P141 | 451 (3) |
| I/O | - | E11 | P99 | P142 | 454 (3) |
| GND | - | E10 | P100 | P143 | - |
| I/O | - | - | - | P145 | 457 (3) |
| I/O | - | - | - | P146 | 460 (3) |
| I/O | - | - | - | P147 | 463 (3) |
| I/O | - | - | - | P148 | 466 (3) |
| I/O (D1(2)) | P70 | D13 | P101 | P149 | 469 (3) |
| I/O | P71 | D12 | P102 | P150 | 472 (3) |
| I/O | - | D11 | P103 | P151 | 475 (3) |

## XCS20 and XCS20XL Device Pinouts

| XCS20/XL Pad Name | VQ100 | CS144(2,4) | TQ144 | PQ208 | Bndry Scan |
|---|---|---|---|---|---|
| I/O | - | C13 | P104 | P152 | 478 (3) |
| I/O (D0(2), DIN) | P72 | C12 | P105 | P153 | 481 (3) |
| I/O, SGCK4(1), GCK6(2) (DOUT) | P73 | C11 | P106 | P154 | 484 (3) |
| CCLK | P74 | B13 | P107 | P155 | - |
| VCC | P75 | B12 | P108 | P156 | - |
| O, TDO | P76 | A13 | P109 | P157 | 0 |
| GND | P77 | A12 | P110 | P158 | - |
| I/O | P78 | B11 | P111 | P159 | 2 |
| I/O, PGCK4(1), GCK7(2) | P79 | A11 | P112 | P160 | 5 |
| I/O | - | D10 | P113 | P161 | 8 |
| I/O | - | C10 | P114 | P162 | 11 |
| I/O (CS1(2)) | P80 | B10 | P115 | P163 | 14 |
| I/O | P81 | A10 | P116 | P164 | 17 |
| I/O | - | D9 | P117 | P166 | 20 |
| I/O | - | - | - | P167 | 23 |
| I/O | - | - | - | P168 | 26 |
| I/O | - | - | - | P169 | 29 |
| GND | - | C9 | P118 | P170 | - |
| I/O | - | B9 | P119 | P171 | 32 |
| I/O | - | A9 | P120 | P172 | 35 |
| VCC(2) | - | - | - | P173 | - |
| I/O | P82 | D8 | P121 | P174 | 38 |
| I/O | P83 | C8 | P122 | P175 | 41 |
| I/O | - | - | - | P176 | 44 |
| I/O | - | - | - | P177 | 47 |
| I/O | P84 | B8 | P123 | P178 | 50 |
| I/O | P85 | A8 | P124 | P179 | 53 |
| I/O | P86 | B7 | P125 | P180 | 56 |
| I/O | P87 | A7 | P126 | P181 | 59 |
| GND | P88 | C7 | P127 | P182 | - |

2/8/00

## XCS30 and XCS30XL Device Pinouts *(Continued)*

| XCS30/XL Pad Name | VQ100(5) | TQ144 | PQ208 | PQ240 | BG256(5) | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|---|---|
| I/O | - | - | P124 | P144 | M20 | L19 | 493 (3) |
| I/O | - | - | P125 | P145 | L19 | L18 | 496 (3) |
| I/O | P59 | P86 | P126 | P146 | L18 | L17 | 499 (3) |
| I/O | P60 | P87 | P127 | P147 | L20 | L16 | 502 (3) |
| I/O (D4(2)) | P61 | P88 | P128 | P148 | K20 | K19 | 505 (3) |
| I/O | P62 | P89 | P129 | P149 | K19 | K18 | 508 (3) |
| VCC | P63 | P90 | P130 | P150 | VCC(4) | K17 | - |
| GND | P64 | P91 | P131 | P151 | GND(4) | GND(4) | - |
| I/O (D3(2)) | P65 | P92 | P132 | P152 | K18 | K16 | 511 (3) |
| I/O | P66 | P93 | P133 | P153 | K17 | K15 | 514 (3) |
| I/O | P67 | P94 | P134 | P154 | J20 | J19 | 517 (3) |
| I/O | - | P95 | P135 | P155 | J19 | J18 | 520 (3) |
| I/O | - | - | P136 | P156 | J18 | J17 | 523 (3) |
| I/O | - | - | P137 | P157 | J17 | J16 | 526 (3) |
| I/O (D2(2)) | P68 | P96 | P138 | P159 | H19 | H17 | 529 (3) |
| I/O | P69 | P97 | P139 | P160 | H18 | H16 | 532 (3) |
| VCC | - | - | P140 | P161 | VCC(4) | G19 | - |
| I/O | - | P98 | P141 | P162 | G19 | G18 | 535 (3) |
| I/O | - | P99 | P142 | P163 | F20 | G17 | 538 (3) |
| I/O | - | - | - | P164 | G18 | G16 | 541 (3) |
| I/O | - | - | - | P165 | F19 | F19 | 544 (3) |
| GND | - | P100 | P143 | P166 | GND(4) | GND(4) | - |
| I/O | - | - | - | P167 | F18 | F18 | 547 (3) |
| I/O | - | - | P144 | P168 | E19 | F17 | 550 (3) |
| I/O | - | - | P145 | P169 | D20 | F16 | 553 (3) |
| I/O | - | - | P146 | P170 | E18 | F15 | 556 (3) |
| I/O | - | - | P147 | P171 | D19 | E19 | 559 (3) |
| I/O | - | - | P148 | P172 | C20 | E17 | 562 (3) |
| I/O (D1(2)) | P70 | P101 | P149 | P173 | E17 | E16 | 565 (3) |
| I/O | P71 | P102 | P150 | P174 | D18 | D19 | 568 (3) |
| I/O | - | P103 | P151 | P175 | C19 | C19 | 571 (3) |
| I/O | - | P104 | P152 | P176 | B20 | B19 | 574 (3) |
| I/O (D0(2), DIN) | P72 | P105 | P153 | P177 | C18 | C18 | 577 (3) |
| I/O, SGCK4(1), GCK6(2) (DOUT) | P73 | P106 | P154 | P178 | B19 | B18 | 580 (3) |
| CCLK | P74 | P107 | P155 | P179 | A20 | A19 | - |
| VCC | P75 | P108 | P156 | P180 | VCC(4) | C17 | - |
| O, TDO | P76 | P109 | P157 | P181 | A19 | B17 | 0 |
| GND | P77 | P110 | P158 | P182 | GND(4) | GND(4) | - |
| I/O | P78 | P111 | P159 | P183 | B18 | A18 | 2 |
| I/O, PGCK4(1), GCK7(2) | P79 | P112 | P160 | P184 | B17 | A17 | 5 |
| I/O | - | P113 | P161 | P185 | C17 | D16 | 8 |
| I/O | - | P114 | P162 | P186 | D16 | C16 | 11 |
| I/O (CS1)(2) | P80 | P115 | P163 | P187 | A18 | B16 | 14 |
| I/O | P81 | P116 | P164 | P188 | A17 | A16 | 17 |
| I/O | - | - | P165 | P189 | C16 | D15 | 20 |

## XCS30 and XCS30XL Device Pinouts *(Continued)*

| XCS30/XL Pad Name | VQ100(5) | TQ144 | PQ208 | PQ240 | BG256(5) | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|---|---|
| I/O | - | - | - | P190 | B16 | A15 | 23 |
| I/O | - | P117 | P166 | P191 | A16 | E14 | 26 |
| I/O | - | - | P167 | P192 | C15 | C14 | 29 |
| I/O | - | - | P168 | P193 | B15 | B14 | 32 |
| I/O | - | - | P169 | P194 | A15 | D14 | 35 |
| GND | - | P118 | P170 | P196 | GND(4) | GND(4) | - |
| I/O | - | P119 | P171 | P197 | B14 | A14 | 38 |
| I/O | - | P120 | P172 | P198 | A14 | C13 | 41 |
| I/O | - | - | - | P199 | C13 | B13 | 44 |
| I/O | - | - | - | P200 | B13 | A13 | 47 |
| VCC | - | - | P173 | P201 | VCC(4) | D13 | - |
| I/O | P82 | P121 | P174 | P202 | C12 | B12 | 50 |
| I/O | P83 | P122 | P175 | P203 | B12 | D12 | 53 |
| I/O | - | - | P176 | P205 | A12 | A11 | 56 |
| I/O | - | - | P177 | P206 | B11 | B11 | 59 |
| I/O | P84 | P123 | P178 | P207 | C11 | C11 | 62 |
| I/O | P85 | P124 | P179 | P208 | A11 | D11 | 65 |
| I/O | P86 | P125 | P180 | P209 | A10 | A10 | 68 |
| I/O | P87 | P126 | P181 | P210 | B10 | B10 | 71 |
| GND | P88 | P127 | P182 | P211 | GND(4) | GND(4) | - |

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**Notes:**

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND(4) or $V_{CC}$(4) are internally bonded to Ground or $V_{CC}$ planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01

### *Additional XCS30/XL Package Pins*

**PQ240**

| GND Pins | | | | | |
|---|---|---|---|---|---|
| P22 | P37 | P83 | P98 | P143 | P158 |
| P204 | P219 | - | - | - | - |
| **Not Connected Pins** | | | | | |
| P195 | - | - | - | - | - |

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**BG256**

| VCC Pins | | | | | |
|---|---|---|---|---|---|
| C14 | D6 | D7 | D11 | D14 | D15 |
| E20 | F1 | F4 | F17 | G4 | G17 |
| K4 | L17 | P4 | P17 | P19 | R2 |
| R4 | R17 | U6 | U7 | U10 | U14 |
| U15 | V7 | W20 | - | - | - |

| GND Pins | | | | | |
|---|---|---|---|---|---|
| A1 | B7 | D4 | D8 | D13 | D17 |
| G20 | H4 | H17 | N3 | N4 | N17 |
| U4 | U8 | U13 | U17 | W14 | - |
| **Not Connected Pins** | | | | | |
| A7 | A13 | C8 | D12 | H20 | J3 |
| J4 | M4 | M19 | V9 | W9 | W13 |
| Y13 | - | - | - | - | - |

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**CS280**

| VCC Pins | | | | | |
|---|---|---|---|---|---|
| A1 | A7 | C10 | C17 | D13 | G1 |
| G1 | G19 | K2 | K17 | M4 | N16 |
| T7 | U3 | U10 | U17 | W13 | - |
| **GND Pins** | | | | | |

**CS280**

| | | | | | |
|---|---|---|---|---|---|
| **VCC Pins** | | | | | |
| E5 | E7 | E8 | E9 | E11 | E12 |
| E13 | G5 | G15 | H5 | H15 | J5 |
| J15 | L5 | L15 | M5 | M15 | N5 |
| N15 | R7 | R8 | R9 | R11 | R12 |
| R13 | - | - | - | - | - |
| **Not Connected Pins** | | | | | |
| A4 | A12 | C8 | C12 | C15 | D1 |
| D2 | D5 | D8 | D17 | D18 | E15 |
| H2 | H3 | H18 | H19 | L4 | M1 |
| M16 | M18 | R2 | R4 | R5 | R15 |
| R17 | T8 | T15 | U5 | V8 | V12 |
| W12 | W16 | - | - | - | - |
| **Not Connected Pins (VCC in XCS40XL)** | | | | | |
| B5 | B15 | E3 | E18 | R3 | R18 |
| V5 | V15 | - | - | - | - |

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## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| VCC | P183 | P212 | VCC(4) | VCC(4) | - |
| I/O | P184 | P213 | C10 | D10 | 86 |
| I/O | P185 | P214 | D10 | E10 | 89 |
| I/O | P186 | P215 | A9 | A9 | 92 |
| I/O | P187 | P216 | B9 | B9 | 95 |
| I/O | P188 | P217 | C9 | C9 | 98 |
| I/O | P189 | P218 | D9 | D9 | 101 |
| I/O | P190 | P220 | A8 | A8 | 104 |
| I/O | P191 | P221 | B8 | B8 | 107 |
| I/O | - | - | C8 | C8 | 110 |
| I/O | - | - | A7 | D8 | 113 |
| VCC | P192 | P222 | VCC(4) | VCC(4) | - |
| I/O | - | P223 | A6 | B7 | 116 |
| I/O | - | P224 | C7 | C7 | 119 |
| I/O | P193 | P225 | B6 | D7 | 122 |
| I/O | P194 | P226 | A5 | A6 | 125 |
| GND | P195 | P227 | GND(4) | GND(4) | - |
| I/O | P196 | P228 | C6 | B6 | 128 |
| I/O | P197 | P229 | B5 | C6 | 131 |
| I/O | P198 | P230 | A4 | D6 | 134 |
| I/O | P199 | P231 | C5 | E6 | 137 |
| I/O | P200 | P232 | B4 | A5 | 140 |
| I/O | P201 | P233 | A3 | C5 | 143 |
| I/O | - | - | - | D5 | 146 |
| I/O | - | - | - | A4 | 149 |
| I/O | P202 | P234 | D5 | B4 | 152 |
| I/O | P203 | P235 | C4 | C4 | 155 |
| I/O | P204 | P236 | B3 | A3 | 158 |
| I/O | P205 | P237 | B2 | A2 | 161 |
| I/O | P206 | P238 | A2 | B3 | 164 |
| I/O, SGCK1(1), GCK8(2) | P207 | P239 | C3 | B2 | 167 |
| VCC | P208 | P240 | VCC(4) | VCC(4) | - |
| GND | P1 | P1 | GND(4) | GND(4) | - |
| I/O, PGCK1(1), GCK1(2) | P2 | P2 | B1 | C3 | 170 |
| I/O | P3 | P3 | C2 | C2 | 173 |
| I/O | P4 | P4 | D2 | B1 | 176 |
| I/O | P5 | P5 | D3 | C1 | 179 |
| I/O, TDI | P6 | P6 | E4 | D4 | 182 |
| I/O, TCK | P7 | P7 | C1 | D3 | 185 |
| I/O | - | - | - | D2 | 188 |
| I/O | - | - | - | D1 | 191 |
| I/O | P8 | P8 | D1 | E2 | 194 |
| I/O | P9 | P9 | E3 | E4 | 197 |
| I/O | P10 | P10 | E2 | E1 | 200 |
| I/O | P11 | P11 | E1 | F5 | 203 |
| I/O | P12 | P12 | F3 | F3 | 206 |
| I/O | - | P13 | F2 | F2 | 209 |
| GND | P13 | P14 | GND(4) | GND(4) | - |
| I/O | P14 | P15 | G3 | F4 | 212 |
| I/O | P15 | P16 | G2 | F1 | 215 |
| I/O, TMS | P16 | P17 | G1 | G3 | 218 |
| I/O | P17 | P18 | H3 | G2 | 221 |
| VCC | P18 | P19 | VCC(4) | VCC(4) | - |
| I/O | - | P20 | H2 | G4 | 224 |
| I/O | - | P21 | H1 | H1 | 227 |
| I/O | - | - | J4 | H3 | 230 |
| I/O | - | - | J3 | H2 | 233 |
| I/O | P19 | P23 | J2 | H4 | 236 |
| I/O | P20 | P24 | J1 | J1 | 239 |
| I/O | P21 | P25 | K2 | J2 | 242 |
| I/O | P22 | P26 | K3 | J3 | 245 |
| I/O | P23 | P27 | K1 | J4 | 248 |
| I/O | P24 | P28 | L1 | K1 | 251 |

## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| GND | P25 | P29 | GND(4) | GND(4) | - |
| VCC | P26 | P30 | VCC(4) | VCC(4) | - |
| I/O | P27 | P31 | L2 | K3 | 254 |
| I/O | P28 | P32 | L3 | K4 | 257 |
| I/O | P29 | P33 | L4 | K5 | 260 |
| I/O | P30 | P34 | M1 | L1 | 263 |
| I/O | P31 | P35 | M2 | L2 | 266 |
| I/O | P32 | P36 | M3 | L3 | 269 |
| I/O | - | - | M4 | L4 | 272 |
| I/O | - | - | - | M1 | 275 |
| I/O | - | P38 | N1 | M2 | 278 |
| I/O | - | P39 | N2 | M3 | 281 |
| VCC | P33 | P40 | VCC(4) | VCC(4) | - |
| I/O | P34 | P41 | P1 | N1 | 284 |
| I/O | P35 | P42 | P2 | N2 | 287 |
| I/O | P36 | P43 | R1 | N3 | 290 |
| I/O | P37 | P44 | P3 | N4 | 293 |
| GND | P38 | P45 | GND(4) | GND(4) | - |
| I/O | - | P46 | T1 | P1 | 296 |
| I/O | P39 | P47 | R3 | P2 | 299 |
| I/O | P40 | P48 | T2 | P3 | 302 |
| I/O | P41 | P49 | U1 | P4 | 305 |
| I/O | P42 | P50 | T3 | P5 | 308 |
| I/O | P43 | P51 | U2 | R1 | 311 |
| I/O | - | - | - | R2 | 314 |
| I/O | - | - | - | R4 | 317 |
| I/O | P44 | P52 | V1 | T1 | 320 |
| I/O | P45 | P53 | T4 | T2 | 323 |
| I/O | P46 | P54 | U3 | T3 | 326 |
| I/O | P47 | P55 | V2 | U1 | 329 |
| I/O | P48 | P56 | W1 | V1 | 332 |
| I/O, SGCK2(1), GCK2 (2) | P49 | P57 | V3 | U2 | 335 |
| Not Connected(1) M1(2) | P50 | P58 | W2 | V2 | 338 |
| GND | P51 | P59 | GND(4) | GND(4) | - |
| MODE(1), M0(2) | P52 | P60 | Y1 | W1 | 341 |
| VCC | P53 | P61 | VCC(4) | VCC(4) | - |
| Not Connected(1) $\overline{\text{PWRDWN}}$(2) | P54 | P62 | W3 | V3 | 342(1) |
| I/O, PGCK2(1), GCK3(2) | P55 | P63 | Y2 | W2 | 343 (3) |

## XCS40 and XCS40XL Device Pinouts

| XCS40/XL Pad Name | PQ208 | PQ240 | BG256 | CS280(2,5) | Bndry Scan |
|---|---|---|---|---|---|
| I/O (HDC) | P56 | P64 | W4 | W3 | 346 (3) |
| I/O | P57 | P65 | V4 | T4 | 349 (3) |
| I/O | P58 | P66 | U5 | U4 | 352 (3) |
| I/O | P59 | P67 | Y3 | V4 | 355 (3) |
| I/O ($\overline{\text{LDC}}$) | P60 | P68 | Y4 | W4 | 358 (3) |
| I/O | - | - | - | R5 | 361 (3) |
| I/O | - | - | - | U5 | 364 (3) |
| I/O | P61 | P69 | V5 | T5 | 367 (3) |
| I/O | P62 | P70 | W5 | W5 | 370 (3) |
| I/O | P63 | P71 | Y5 | R6 | 373 (3) |
| I/O | P64 | P72 | V6 | U6 | 376 (3) |
| I/O | P65 | P73 | W6 | V6 | 379 (3) |
| I/O | - | P74 | Y6 | T6 | 382 (3) |
| GND | P66 | P75 | GND(4) | GND(4) | - |
| I/O | P67 | P76 | W7 | W6 | 385 (3) |
| I/O | P68 | P77 | Y7 | U7 | 388 (3) |
| I/O | P69 | P78 | V8 | V7 | 391 (3) |
| I/O | P70 | P79 | W8 | W7 | 394 (3) |
| VCC | P71 | P80 | VCC(4) | VCC(4) | - |
| I/O | P72 | P81 | Y8 | W8 | 397 (3) |
| I/O | P73 | P82 | U9 | U8 | 400 (3) |
| I/O | - | - | V9 | V8 | 403 (3) |
| I/O | - | - | W9 | T8 | 406 (3) |
| I/O | - | P84 | Y9 | W9 | 409 (3) |
| I/O | - | P85 | W10 | V9 | 412 (3) |
| I/O | P74 | P86 | V10 | U9 | 415 (3) |
| I/O | P75 | P87 | Y10 | T9 | 418 (3) |
| I/O | P76 | P88 | Y11 | W10 | 421 (3) |
| I/O ($\overline{\text{INIT}}$) | P77 | P89 | W11 | V10 | 424 (3) |
| VCC | P78 | P90 | VCC(4) | VCC(4) | VCC(4) |
| GND | P79 | P91 | GND(4) | GND(4) | - |
| I/O | P80 | P92 | V11 | T10 | 427 (3) |
| I/O | P81 | P93 | U11 | R10 | 430 (3) |
| I/O | P82 | P94 | Y12 | W11 | 433 (3) |
| I/O | P83 | P95 | W12 | V11 | 436 (3) |
| I/O | P84 | P96 | V12 | U11 | 439 (3) |
| I/O | P85 | P97 | U12 | T11 | 442 (3) |
| I/O | - | - | Y13 | W12 | 445 (3) |
| I/O | - | - | W13 | V12 | 448 (3) |
| I/O | - | P99 | V13 | U12 | 451 (3) |
| I/O | - | P100 | Y14 | T12 | 454 (3) |
| VCC | P86 | P101 | VCC(4) | VCC(4) | - |
| I/O | P87 | P102 | Y15 | V13 | 457 (3) |
| I/O | P88 | P103 | V14 | U13 | 460 (3) |
| I/O | P89 | P104 | W15 | T13 | 463 (3) |

## Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

*Table 19:* **Component Availability Chart for Spartan/XL FPGAs**

| Device | Pins | 84 | 100 | 144 | 144 | 208 | 240 | 256 | 280 |
|---|---|---|---|---|---|---|---|---|---|
| | Type | Plastic PLCC | Plastic VQFP | Chip Scale | Plastic TQFP | Plastic PQFP | Plastic PQFP | Plastic BGA | Chip Scale |
| | Code | PC84(3) | VQ100(3) | CS144(3) | TQ144 | PQ208 | PQ240 | BG256(3) | CS280(3) |
| XCS05 | -3 | C(3) | C, I | - | - | - | - | - | - |
| | -4 | C(3) | C | - | - | - | - | - | - |
| XCS10 | -3 | C(3) | C, I | - | C | - | - | - | - |
| | -4 | C(3) | C | - | C | - | - | - | - |
| XCS20 | -3 | - | C | - | C, I | C, I | - | - | - |
| | -4 | - | C | - | C | C | - | - | - |
| XCS30 | -3 | - | C(3) | - | C, I | C, I | C | C(3) | - |
| | -4 | - | C(3) | - | C | C | C | C(3) | - |
| XCS40 | -3 | - | - | - | - | C, I | C | C | - |
| | -4 | - | - | - | - | C | C | C | - |
| XCS05XL | -4 | C(3) | C, I | - | - | - | - | - | - |
| | -5 | C(3) | C | - | - | - | - | - | - |
| XCS10XL | -4 | C(3) | C, I | C(3) | C | - | - | - | - |
| | -5 | C(3) | C | C(3) | C | - | - | - | - |
| XCS20XL | -4 | - | C, I | C(3) | C, I | C, I | - | - | - |
| | -5 | - | C | C(3) | C | C | - | - | - |
| XCS30XL | -4 | - | C, I | - | C, I | C, I | C | C | C(3) |
| | -5 | - | C | - | C | C | C | C | C(3) |
| XCS40XL | -4 | - | - | - | - | C, I | C | C, I | C(3) |
| | -5 | - | - | - | - | C | C | C | C(3) |

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**Notes:**

1. C = Commercial $T_J = 0°$ to $+85°C$
2. I = Industrial $T_J = –40°C$ to $+100°C$
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by **PDN2004-01**
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

### *Package Specifications*

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

**www.xilinx.com/support/documentation/spartan-xl.htm#19687**

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

**www.xilinx.com/cgi-bin/thermal/thermal.pl**