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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	576
Number of Logic Elements/Cells	1368
Total RAM Bits	18432
Number of I/O	169
Number of Gates	30000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcs30xl-4pq208i">https://www.e-xfl.com/product-detail/xilinx/xcs30xl-4pq208i</a>

Spartan and Spartan-XL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In addition to the conventional benefit of high volume programmable logic solutions, Spartan series FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan/XL families leverage the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA process developments.

## Logic Functional Description

The Spartan series uses a standard FPGA structure as shown in [Figure 1, page 2](#). The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

## Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in [Figure 2](#). There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the [Advanced Features Description, page 13](#).

### Function Generators

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box "A" of [Figure 2](#)). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.

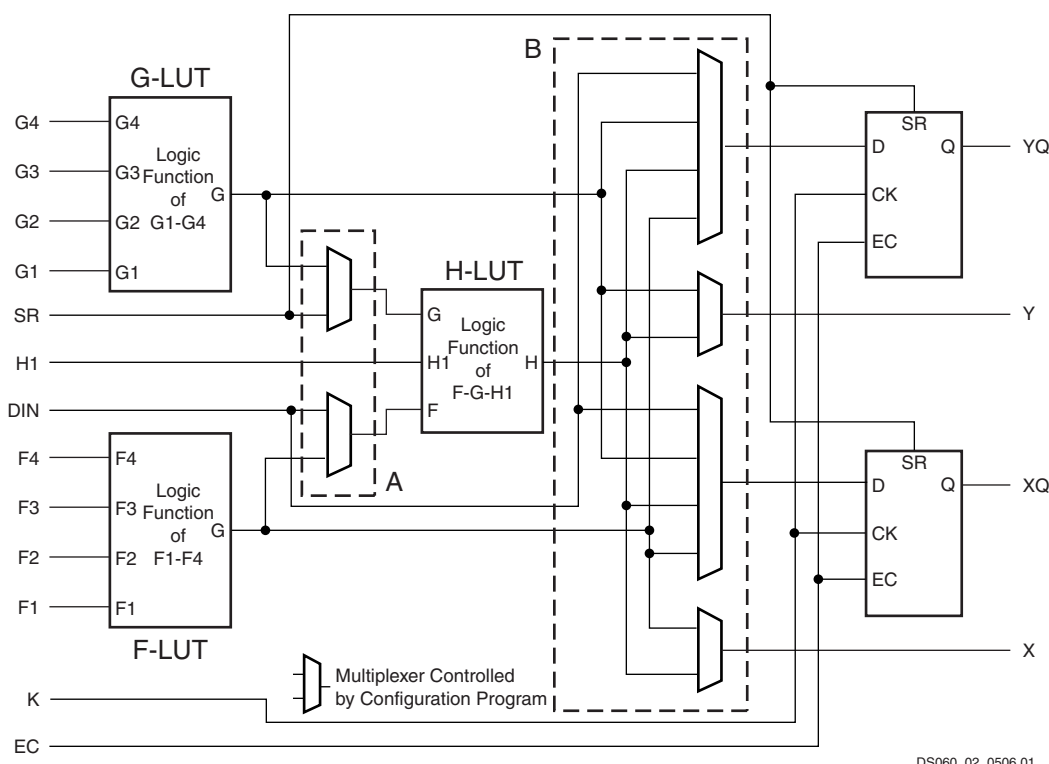


Figure 2: Spartan/XL Simplified CLB Logic Diagram (some features not shown)

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

**Note:** When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

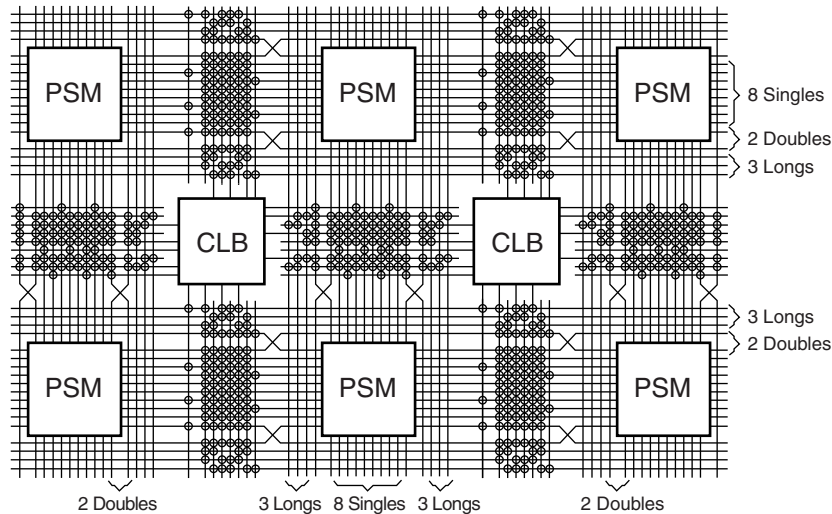
### Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.

### Latches (Spartan-XL Family Only)

The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.

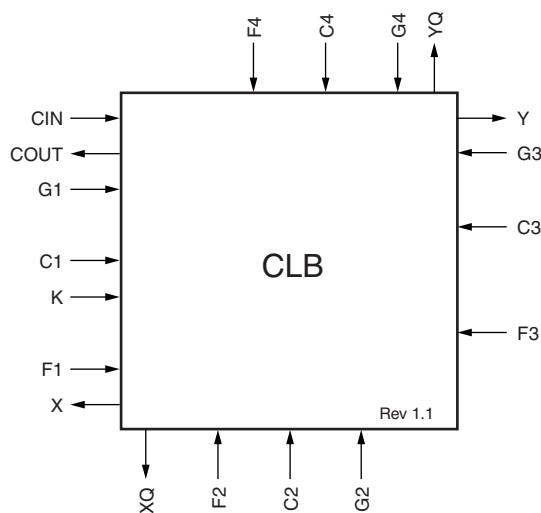


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Figure 8: Spartan/XL CLB Routing Channels and Interface Block Diagram

### CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.



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Figure 9: CLB Interconnect Signals

### Programmable Switch Matrices

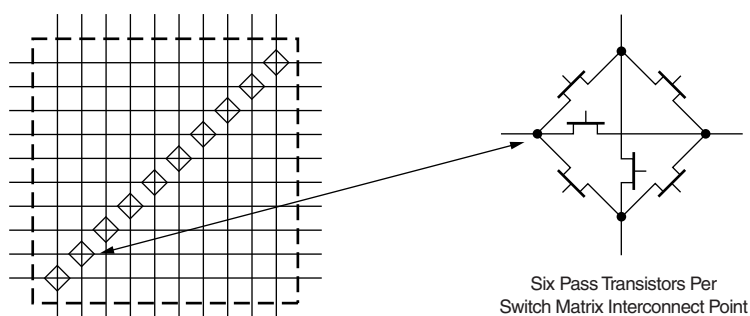
The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

### Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs. Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.



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Figure 10: Programmable Switch Matrix

### Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 8).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

### Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 8. The longlines also interface to some 3-state buffers which is described later in **3-State Long Line Drivers**, page 19.

### I/O Routing

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

### Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 11. In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.

CLB signals from which they are originally derived are shown in Table 10.

Table 10: Dual-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F <sub>OUT</sub>
DPO	Dual Port Out (addressed by DPRA[3:0])	G <sub>OUT</sub>

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

#### Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

#### More Information on Using RAM Inside CLBs

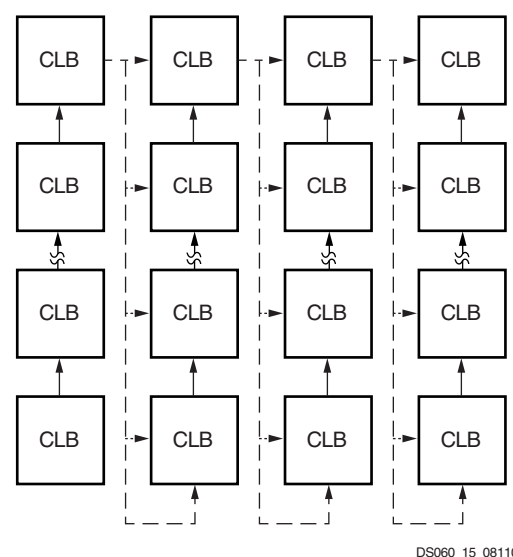
Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both the Spartan and the Spartan-XL families.

#### Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in micro-processor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan



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Figure 15: Available Spartan/XL Carry Propagation Paths

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

### Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

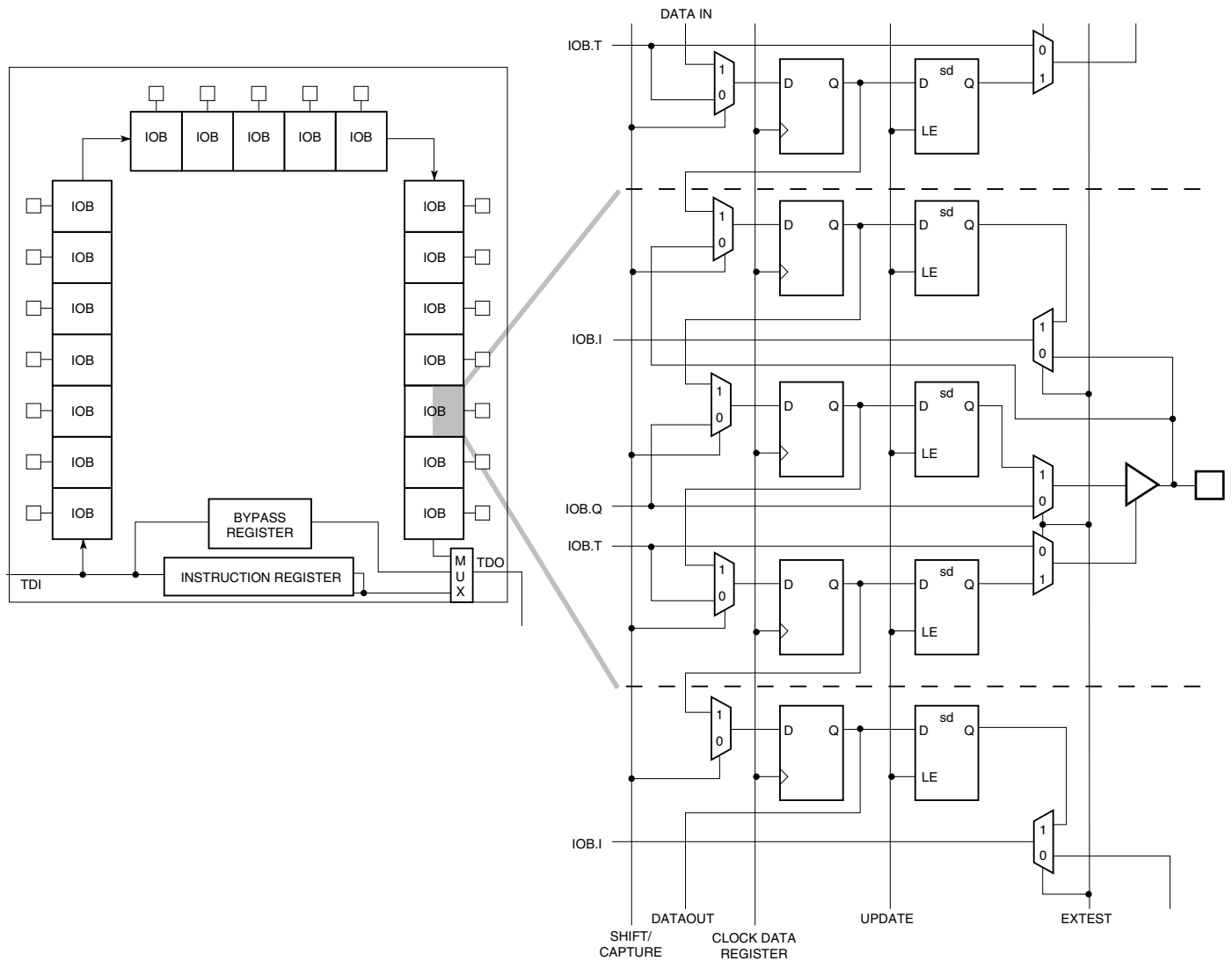
The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

### Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.





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Figure 20: Spartan/XL Boundary Scan Logic



## Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is –50% to +25%.

In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

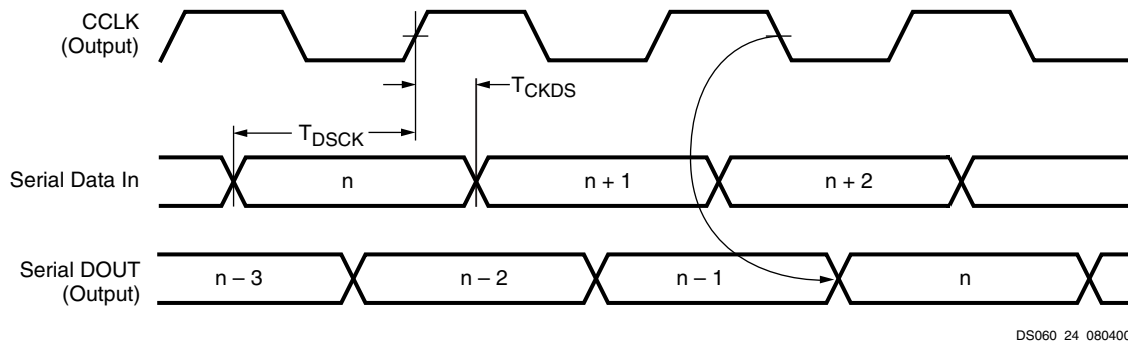
When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the

falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in [Figure 24](#).

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Earlier families such as the XC3000 series do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either  $\overline{\text{LDC}}$  or DONE. Using  $\overline{\text{LDC}}$  avoids potential contention on the DIN pin, if this pin is configured as user I/O, but  $\overline{\text{LDC}}$  is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

[Figure 25](#) shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Symbol	Description	Min	Units
CCLK	$T_{\text{DSCK}}$	DIN setup	20	ns
	$T_{\text{CKDS}}$	DIN hold	0	ns

### Notes:

1. At power-up,  $V_{\text{CC}}$  must rise from 2.0V to  $V_{\text{CC}}$  min in less than 25 ms, otherwise delay configuration by pulling  $\overline{\text{PROGRAM}}$  Low until  $V_{\text{CC}}$  is valid.
2. Master Serial mode timing is based on testing in slave mode.

**Figure 24: Master Serial Mode Programming Switching Characteristics**

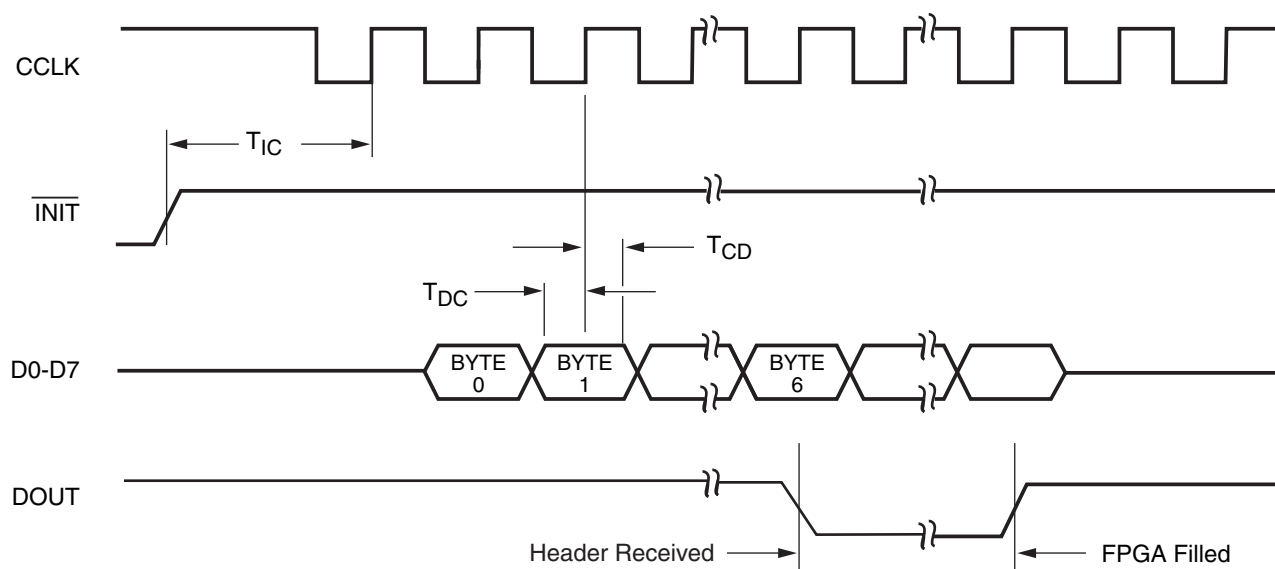
## Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

[Figure 25](#) shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.



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Symbol		Description	Min	Max	Units
$T_{IC}$	CCLK	$\overline{INIT}$ (High) setup time	5	-	$\mu s$
$T_{DC}$		D0-D7 setup time	20	-	ns
$T_{CD}$		D0-D7 hold time	0	-	ns
$T_{CCH}$		CCLK High time	45	-	ns
$T_{CCL}$		CCLK Low time	45	-	ns
$F_{CC}$		CCLK Frequency	-	10	MHz

**Notes:**

1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: Express Mode Programming Switching Characteristics

## Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

## Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right.

Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

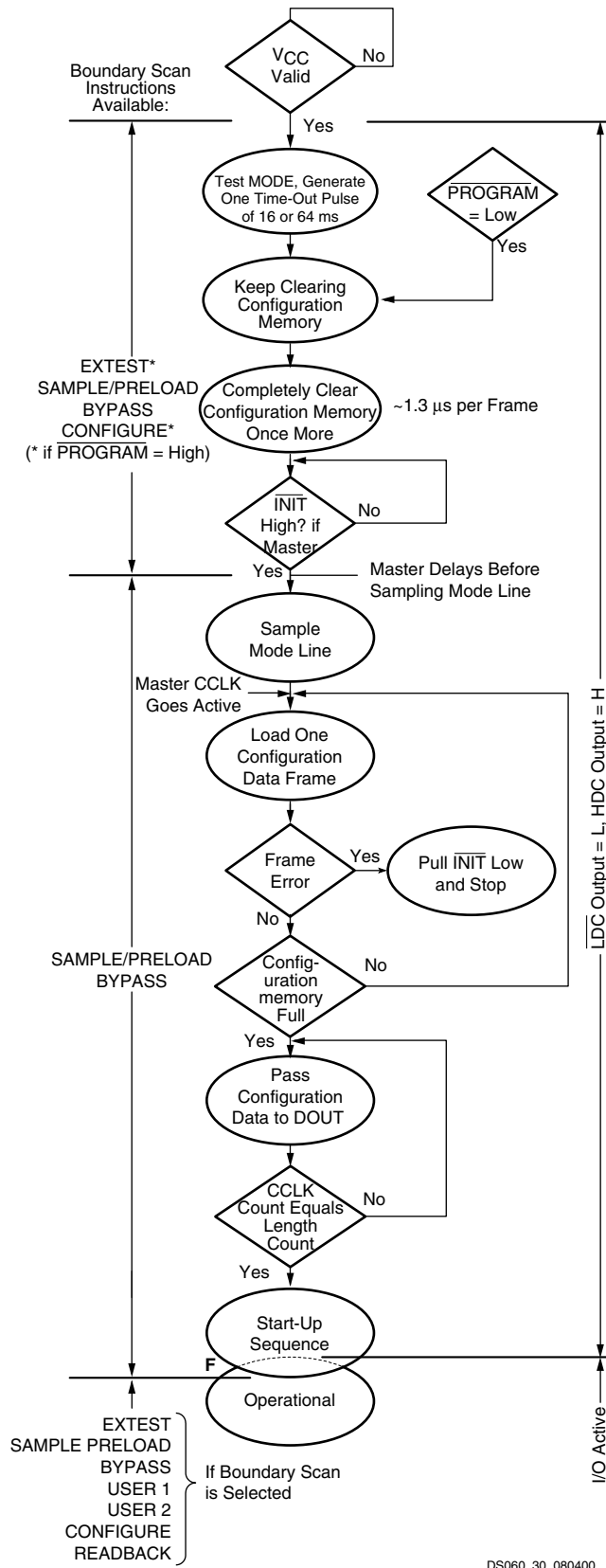


Figure 30: Power-up Configuration Sequence

## Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count for serial modes. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Spartan-XL family Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain  $\overline{\text{INIT}}$  pin Low. After all configuration frames have been loaded into an FPGA using a serial mode, DOUT again follows the input data so that the remaining data is passed on to the next device. In Spartan-XL family Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

## Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the  $\overline{\text{PROGRAM}}$  input, or pull the bidirectional  $\overline{\text{INIT}}$  pin Low, using an open-collector (open-drain) driver. (See Figure 30.)

A Low on the  $\overline{\text{PROGRAM}}$  input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as  $\overline{\text{PROGRAM}}$  is Low, the FPGA keeps clearing its configuration memory. When  $\overline{\text{PROGRAM}}$  goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the  $\overline{\text{INIT}}$  input is not externally held Low. Note that a Low on the  $\overline{\text{PROGRAM}}$  input automatically forces a Low on the  $\overline{\text{INIT}}$  output. The Spartan/XL FPGA  $\overline{\text{PROGRAM}}$  pin has a permanent weak pull-up.

Avoid holding  $\overline{\text{PROGRAM}}$  Low for more than 500  $\mu\text{s}$ . The 500  $\mu\text{s}$  maximum limit is only a recommendation, not a requirement. The only effect of holding  $\overline{\text{PROGRAM}}$  Low for more than 500  $\mu\text{s}$  is an increase in current, measured at about 40 mA in the XCS40XL. This increased current cannot damage the device. This applies only during reconfiguration, not during power-up. The  $\overline{\text{INIT}}$  pin can also be held Low to delay reconfiguration, and the same characteristics apply as for the  $\overline{\text{PROGRAM}}$  pin.

Using an open-collector or open-drain driver to hold  $\overline{\text{INIT}}$  Low before the beginning of configuration causes the FPGA

## Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

## Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

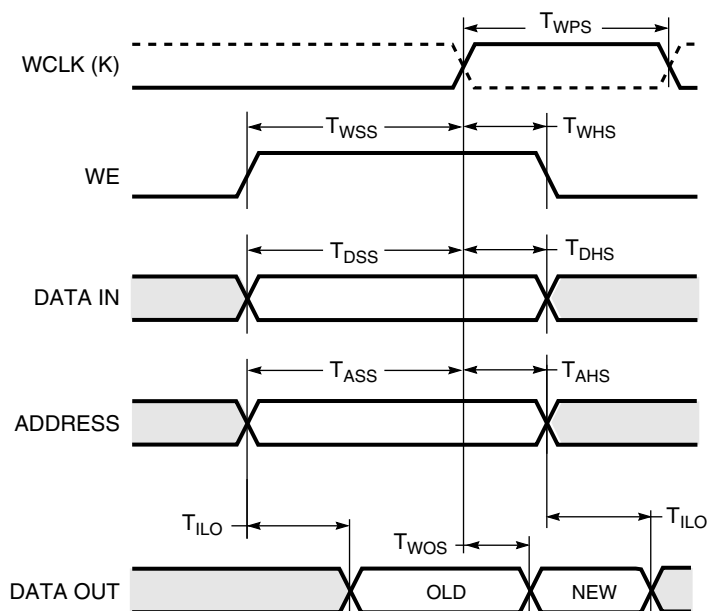
Symbol	Dual Port RAM	Size <sup>(1)</sup>	-4		-3		Units
			Min	Max	Min	Max	
Write Operation							
T <sub>WCDS</sub>	Address write cycle time (clock K period)	16x1	8.0	-	11.6	-	ns
T <sub>WPDS</sub>	Clock K pulse width (active edge)	16x1	4.0	-	5.8	-	ns
T <sub>ASDS</sub>	Address setup time before clock K	16x1	1.5	-	2.1	-	ns
T <sub>AHDS</sub>	Address hold time after clock K	16x1	0	-	0	-	ns
T <sub>DSDS</sub>	DIN setup time before clock K	16x1	1.5	-	1.6	-	ns
T <sub>DHDS</sub>	DIN hold time after clock K	16x1	0	-	0	-	ns
T <sub>WSDS</sub>	WE setup time before clock K	16x1	1.5	-	1.6	-	ns
T <sub>WHDS</sub>	WE hold time after clock K	16x1	0	-	0	-	ns
T <sub>WODS</sub>	Data valid after clock K	16x1	-	6.5	-	7.0	ns

### Notes:

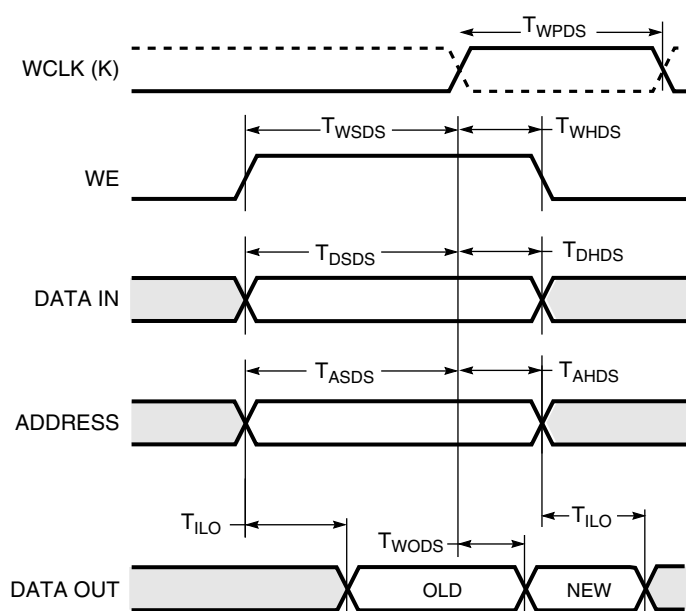
- Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

## Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Timing

### Single Port



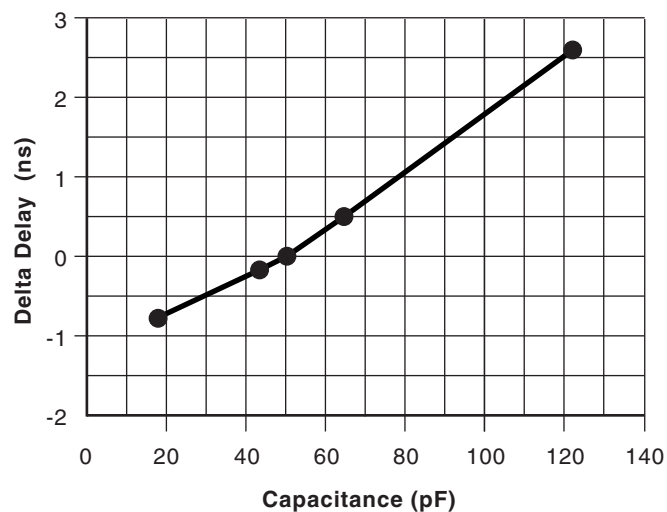
### Dual Port



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### Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



DS060\_35\_080400

Figure 34: Delay Factor at Various Capacitive Loads

### Spartan Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to

the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Clocks							
T <sub>CH</sub>	Clock High	All devices	3.0	-	4.0	-	ns
T <sub>CL</sub>	Clock Low	All devices	3.0	-	4.0	-	ns
Propagation Delays - TTL Outputs <sup>(1,2)</sup>							
T <sub>OKPOF</sub>	Clock (OK) to Pad, fast	All devices	-	3.3	-	4.5	ns
T <sub>OKPOS</sub>	Clock (OK) to Pad, slew-rate limited	All devices	-	6.9	-	7.0	ns
T <sub>OPF</sub>	Output (O) to Pad, fast	All devices	-	3.6	-	4.8	ns
T <sub>OPS</sub>	Output (O) to Pad, slew-rate limited	All devices	-	7.2	-	7.3	ns
T <sub>TSHZ</sub>	3-state to Pad High-Z (slew-rate independent)	All devices	-	3.0	-	3.8	ns
T <sub>TSONF</sub>	3-state to Pad active and valid, fast	All devices	-	6.0	-	7.3	ns
T <sub>TSONS</sub>	3-state to Pad active and valid, slew-rate limited	All devices	-	9.6	-	9.8	ns
Setup and Hold Times							
T <sub>OOK</sub>	Output (O) to clock (OK) setup time	All devices	2.5	-	3.8	-	ns
T <sub>OKO</sub>	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T <sub>ECOK</sub>	Clock Enable (EC) to clock (OK) setup time	All devices	2.0	-	2.7	-	ns
T <sub>OKEC</sub>	Clock Enable (EC) to clock (OK) hold time	All devices	0.0	-	0.5	-	ns
Global Set/Reset							
T <sub>MRW</sub>	Minimum GSR pulse width	All devices	11.5		13.5		ns
T <sub>RPO</sub>	Delay from GSR input to any Pad	XCS05	-	12.0	-	15.0	ns
		XCS10	-	12.5	-	15.7	ns
		XCS20	-	13.0	-	16.2	ns
		XCS30	-	13.5	-	16.9	ns
		XCS40	-	14.0	-	17.5	ns

#### Notes:

1. Delay adder for CMOS Outputs option (with fast slew rate option): for -3 speed grade, add 1.0 ns; for -4 speed grade, add 0.8 ns.
2. Delay adder for CMOS Outputs option (with slow slew rate option): for -3 speed grade, add 2.0 ns; for -4 speed grade, add 1.5 ns.
3. Output timing is measured at ~50%  $V_{CC}$  threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
4. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

### Spartan-XL Family Setup and Hold

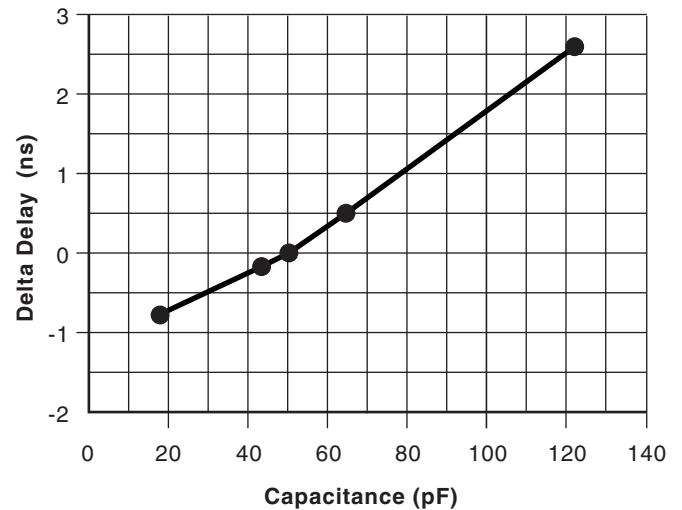
Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Input Setup/Hold Times Using Global Clock and IFF					
T <sub>SUF</sub> /T <sub>HF</sub>	No Delay	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
T <sub>SU</sub> /T <sub>H</sub>	Full Delay	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

#### Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

### Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



DS060\_35\_080400

Figure 35: Delay Factor at Various Capacitive Loads



Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	<p>Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin.</p> <p>The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.</p>
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	<p>Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin.</p> <p>The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.</p>
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	<p>During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input.</p> <p>In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices.</p> <p>After configuration, DOUT is a user-programmable I/O pin.</p>
<b>Unrestricted User-Programmable I/O Pins</b>			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

### Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and Spartan-XL device. They follow the pad locations around the die, and include boundary scan register locations.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

#### XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	Bndry Scan
VCC	P2	P89	-
I/O	P3	P90	32
I/O	P4	P91	35
I/O	-	P92	38
I/O	-	P93	41
I/O	P5	P94	44
I/O	P6	P95	47
I/O	P7	P96	50
I/O	P8	P97	53
I/O	P9	P98	56
I/O, SGCK1 <sup>(1)</sup> , GCK8 <sup>(2)</sup>	P10	P99	59
VCC	P11	P100	-
GND	P12	P1	-
I/O, PGCK1 <sup>(1)</sup> , GCK1 <sup>(2)</sup>	P13	P2	62
I/O	P14	P3	65
I/O, TDI	P15	P4	68
I/O, TCK	P16	P5	71
I/O, TMS	P17	P6	74
I/O	P18	P7	77
I/O	-	P8	83
I/O	P19	P9	86
I/O	P20	P10	89
GND	P21	P11	-
VCC	P22	P12	-
I/O	P23	P13	92
I/O	P24	P14	95
I/O	-	P15	98
I/O	P25	P16	104
I/O	P26	P17	107
I/O	P27	P18	110
I/O	-	P19	113
I/O	P28	P20	116
I/O, SGCK2 <sup>(1)</sup> , GCK2 <sup>(2)</sup>	P29	P21	119
Not Connected <sup>(1)</sup> , M1 <sup>(2)</sup>	P30	P22	122
GND	P31	P23	-
MODE <sup>(1)</sup> , M0 <sup>(2)</sup>	P32	P24	125
VCC	P33	P25	-

#### XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	Bndry Scan
Not Connected <sup>(1)</sup> , PWRDWN <sup>(2)</sup>	P34	P26	126 <sup>(1)</sup>
I/O, PGCK2 <sup>(1)</sup> , GCK3 <sup>(2)</sup>	P35	P27	127 <sup>(3)</sup>
I/O (HDC)	P36	P28	130 <sup>(3)</sup>
I/O	-	P29	133 <sup>(3)</sup>
I/O (LDC)	P37	P30	136 <sup>(3)</sup>
I/O	P38	P31	139 <sup>(3)</sup>
I/O	P39	P32	142 <sup>(3)</sup>
I/O	-	P33	145 <sup>(3)</sup>
I/O	-	P34	148 <sup>(3)</sup>
I/O	P40	P35	151 <sup>(3)</sup>
I/O (INIT)	P41	P36	154 <sup>(3)</sup>
VCC	P42	P37	-
GND	P43	P38	-
I/O	P44	P39	157 <sup>(3)</sup>
I/O	P45	P40	160 <sup>(3)</sup>
I/O	-	P41	163 <sup>(3)</sup>
I/O	-	P42	166 <sup>(3)</sup>
I/O	P46	P43	169 <sup>(3)</sup>
I/O	P47	P44	172 <sup>(3)</sup>
I/O	P48	P45	175 <sup>(3)</sup>
I/O	P49	P46	178 <sup>(3)</sup>
I/O	P50	P47	181 <sup>(3)</sup>
I/O, SGCK3 <sup>(1)</sup> , GCK4 <sup>(2)</sup>	P51	P48	184 <sup>(3)</sup>
GND	P52	P49	-
DONE	P53	P50	-
VCC	P54	P51	-
PROGRAM	P55	P52	-
I/O (D7 <sup>(2)</sup> )	P56	P53	187 <sup>(3)</sup>
I/O, PGCK3 <sup>(1)</sup> , GCK5 <sup>(2)</sup>	P57	P54	190 <sup>(3)</sup>
I/O (D6 <sup>(2)</sup> )	P58	P55	193 <sup>(3)</sup>
I/O	-	P56	196 <sup>(3)</sup>
I/O (D5 <sup>(2)</sup> )	P59	P57	199 <sup>(3)</sup>
I/O	P60	P58	202 <sup>(3)</sup>
I/O	-	P59	205 <sup>(3)</sup>
I/O	-	P60	208 <sup>(3)</sup>
I/O (D4 <sup>(2)</sup> )	P61	P61	211 <sup>(3)</sup>
I/O	P62	P62	214 <sup>(3)</sup>
VCC	P63	P63	-
GND	P64	P64	-
I/O (D3 <sup>(2)</sup> )	P65	P65	217 <sup>(3)</sup>
I/O	P66	P66	220 <sup>(3)</sup>
I/O	-	P67	223 <sup>(3)</sup>
I/O (D2 <sup>(2)</sup> )	P67	P68	229 <sup>(3)</sup>
I/O	P68	P69	232 <sup>(3)</sup>
I/O (D1 <sup>(2)</sup> )	P69	P70	235 <sup>(3)</sup>

### XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	Bndry Scan
I/O	P70	P71	238 <sup>(3)</sup>
I/O (D0 <sup>(2)</sup> , DIN)	P71	P72	241 <sup>(3)</sup>
I/O, SGCK4 <sup>(1)</sup> , GCK6 <sup>(2)</sup> (DOUT)	P72	P73	244 <sup>(3)</sup>
CCLK	P73	P74	-
VCC	P74	P75	-
O, TDO	P75	P76	0
GND	P76	P77	-
I/O	P77	P78	2
I/O, PGCK4 <sup>(1)</sup> , GCK7 <sup>(2)</sup>	P78	P79	5
I/O (CS1 <sup>(2)</sup> )	P79	P80	8
I/O	P80	P81	11
I/O	P81	P82	14
I/O	P82	P83	17
I/O	-	P84	20
I/O	-	P85	23
I/O	P83	P86	26
I/O	P84	P87	29
GND	P1	P88	-

**Notes:**

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS05XL is not part of the Boundary Scan chain. For the XCS05XL, subtract 1 from all Boundary Scan numbers from GCK3 on (127 and higher).
4. PC84 package discontinued by [PDN2004-01](#)

### XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	CS144 <sup>(2,4)</sup>	TQ144	Bndry Scan
VCC	P2	P89	D7	P128	-
I/O	P3	P90	A6	P129	44
I/O	P4	P91	B6	P130	47
I/O	-	P92	C6	P131	50
I/O	-	P93	D6	P132	53
I/O	P5	P94	A5	P133	56
I/O	P6	P95	B5	P134	59
I/O	-	-	C5	P135	62
I/O	-	-	D5	P136	65
GND	-	-	A4	P137	-
I/O	P7	P96	B4	P138	68
I/O	P8	P97	C4	P139	71
I/O	-	-	A3	P140	74
I/O	-	-	B3	P141	77
I/O	P9	P98	C3	P142	80

### XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	CS144 <sup>(2,4)</sup>	TQ144	Bndry Scan
I/O, SGCK1 <sup>(1)</sup> GCK8 <sup>(2)</sup>	P10	P99	A2	P143	83
VCC	P11	P100	B2	P144	-
GND	P12	P1	A1	P1	-
I/O, PGCK1 <sup>(1)</sup> GCK1 <sup>(2)</sup>	P13	P2	B1	P2	86
I/O	P14	P3	C2	P3	89
I/O	-	-	C1	P4	92
I/O	-	-	D4	P5	95
I/O, TDI	P15	P4	D3	P6	98
I/O, TCK	P16	P5	D2	P7	101
GND	-	-	D1	P8	-
I/O	-	-	E4	P9	104
I/O	-	-	E3	P10	107
I/O, TMS	P17	P6	E2	P11	110
I/O	P18	P7	E1	P12	113
I/O	-	-	F4	P13	116
I/O	-	P8	F3	P14	119
I/O	P19	P9	F2	P15	122
I/O	P20	P10	F1	P16	125
GND	P21	P11	G2	P17	-
VCC	P22	P12	G1	P18	-
I/O	P23	P13	G3	P19	128
I/O	P24	P14	G4	P20	131
I/O	-	P15	H1	P21	134
I/O	-	-	H2	P22	137
I/O	P25	P16	H3	P23	140
I/O	P26	P17	H4	P24	143
I/O	-	-	J1	P25	146
I/O	-	-	J2	P26	149
GND	-	-	J3	P27	-
I/O	P27	P18	J4	P28	152
I/O	-	P19	K1	P29	155
I/O	-	-	K2	P30	158
I/O	-	-	K3	P31	161
I/O	P28	P20	L1	P32	164
I/O, SGCK2 <sup>(1)</sup> GCK2 <sup>(2)</sup>	P29	P21	L2	P33	167
Not Connected <sup>(1)</sup> M1 <sup>(2)</sup>	P30	P22	L3	P34	170
GND	P31	P23	M1	P35	-
MODE <sup>(1)</sup> , M0 <sup>(2)</sup>	P32	P24	M2	P36	173

### XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	CS144 <sup>(2,4)</sup>	TQ144	Bndry Scan
VCC	P33	P25	N1	P37	-
Not Connect-ed <sup>(1)</sup>	P34	P26	N2	P38	174 <sup>(1)</sup>
PWRDWN <sup>(2)</sup>					
I/O, PGCK2 <sup>(1)</sup> GCK3 <sup>(2)</sup>	P35	P27	M3	P39	175 <sup>(3)</sup>
I/O (HDC)	P36	P28	N3	P40	178 <sup>(3)</sup>
I/O	-	-	K4	P41	181 <sup>(3)</sup>
I/O	-	-	L4	P42	184 <sup>(3)</sup>
I/O	-	P29	M4	P43	187 <sup>(3)</sup>
I/O (LDC)	P37	P30	N4	P44	190 <sup>(3)</sup>
GND	-	-	K5	P45	-
I/O	-	-	L5	P46	193 <sup>(3)</sup>
I/O	-	-	M5	P47	196 <sup>(3)</sup>
I/O	P38	P31	N5	P48	199 <sup>(3)</sup>
I/O	P39	P32	K6	P49	202 <sup>(3)</sup>
I/O	-	P33	L6	P50	205 <sup>(3)</sup>
I/O	-	P34	M6	P51	208 <sup>(3)</sup>
I/O	P40	P35	N6	P52	211 <sup>(3)</sup>
I/O (INIT)	P41	P36	M7	P53	214 <sup>(3)</sup>
VCC	P42	P37	N7	P54	-
GND	P43	P38	L7	P55	-
I/O	P44	P39	K7	P56	217 <sup>(3)</sup>
I/O	P45	P40	N8	P57	220 <sup>(3)</sup>
I/O	-	P41	M8	P58	223 <sup>(3)</sup>
I/O	-	P42	L8	P59	226 <sup>(3)</sup>
I/O	P46	P43	K8	P60	229 <sup>(3)</sup>
I/O	P47	P44	N9	P61	232 <sup>(3)</sup>
I/O	-	-	M9	P62	235 <sup>(3)</sup>
I/O	-	-	L9	P63	238 <sup>(3)</sup>
GND	-	-	K9	P64	-
I/O	P48	P45	N10	P65	241 <sup>(3)</sup>
I/O	P49	P46	M10	P66	244 <sup>(3)</sup>
I/O	-	-	L10	P67	247 <sup>(3)</sup>
I/O	-	-	N11	P68	250 <sup>(3)</sup>
I/O	P50	P47	M11	P69	253 <sup>(3)</sup>
I/O, SGCK3 <sup>(1)</sup> GCK4 <sup>(2)</sup>	P51	P48	L11	P70	256 <sup>(3)</sup>
GND	P52	P49	N12	P71	-
DONE	P53	P50	M12	P72	-
VCC	P54	P51	N13	P73	-
PROGRAM	P55	P52	M13	P74	-
I/O (D7 <sup>(2)</sup> )	P56	P53	L12	P75	259 <sup>(3)</sup>

### XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84 <sup>(4)</sup>	VQ100	CS144 <sup>(2,4)</sup>	TQ144	Bndry Scan
I/O, PGCK3 <sup>(1)</sup> GCK5 <sup>(2)</sup>	P57	P54	L13	P76	262 <sup>(3)</sup>
I/O	-	-	K10	P77	265 <sup>(3)</sup>
I/O	-	-	K11	P78	268 <sup>(3)</sup>
I/O (D6 <sup>(2)</sup> )	P58	P55	K12	P79	271 <sup>(3)</sup>
I/O	-	P56	K13	P80	274 <sup>(3)</sup>
GND	-	-	J10	P81	-
I/O	-	-	J11	P82	277 <sup>(3)</sup>
I/O	-	-	J12	P83	280 <sup>(3)</sup>
I/O (D5 <sup>(2)</sup> )	P59	P57	J13	P84	283 <sup>(3)</sup>
I/O	P60	P58	H10	P85	286 <sup>(3)</sup>
I/O	-	P59	H11	P86	289 <sup>(3)</sup>
I/O	-	P60	H12	P87	292 <sup>(3)</sup>
I/O (D4 <sup>(2)</sup> )	P61	P61	H13	P88	295 <sup>(3)</sup>
I/O	P62	P62	G12	P89	298 <sup>(3)</sup>
VCC	P63	P63	G13	P90	-
GND	P64	P64	G11	P91	-
I/O (D3 <sup>(2)</sup> )	P65	P65	G10	P92	301 <sup>(3)</sup>
I/O	P66	P66	F13	P93	304 <sup>(3)</sup>
I/O	-	P67	F12	P94	307 <sup>(3)</sup>
I/O	-	-	F11	P95	310 <sup>(3)</sup>
I/O (D2 <sup>(2)</sup> )	P67	P68	F10	P96	313 <sup>(3)</sup>
I/O	P68	P69	E13	P97	316 <sup>(3)</sup>
I/O	-	-	E12	P98	319 <sup>(3)</sup>
I/O	-	-	E11	P99	322 <sup>(3)</sup>
GND	-	-	E10	P100	-
I/O (D1 <sup>(2)</sup> )	P69	P70	D13	P101	325 <sup>(3)</sup>
I/O	P70	P71	D12	P102	328 <sup>(3)</sup>
I/O	-	-	D11	P103	331 <sup>(3)</sup>
I/O	-	-	C13	P104	334 <sup>(3)</sup>
I/O (D0 <sup>(2)</sup> , DIN)	P71	P72	C12	P105	337 <sup>(3)</sup>
I/O, SGCK4 <sup>(1)</sup> GCK6 <sup>(2)</sup> (DOUT)	P72	P73	C11	P106	340 <sup>(3)</sup>
CCLK	P73	P74	B13	P107	-
VCC	P74	P75	B12	P108	-
O, TDO	P75	P76	A13	P109	0
GND	P76	P77	A12	P110	-
I/O	P77	P78	B11	P111	2
I/O, PGCK4 <sup>(1)</sup> GCK7 <sup>(2)</sup>	P78	P79	A11	P112	5
I/O	-	-	D10	P113	8
I/O	-	-	C10	P114	11
I/O (CS1 <sup>(2)</sup> )	P79	P80	B10	P115	14

## XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 <sup>(2,4)</sup>	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7 <sup>(2)</sup> )	P53	L12	P75	P107	367 <sup>(3)</sup>
I/O, PGCK3 <sup>(1)</sup> , GCK5 <sup>(2)</sup>	P54	L13	P76	P108	370 <sup>(3)</sup>
I/O	-	K10	P77	P109	373 <sup>(3)</sup>
I/O	-	K11	P78	P110	376 <sup>(3)</sup>
I/O (D6 <sup>(2)</sup> )	P55	K12	P79	P112	379 <sup>(3)</sup>
I/O	P56	K13	P80	P113	382 <sup>(3)</sup>
I/O	-	-	-	P114	385 <sup>(3)</sup>
I/O	-	-	-	P115	388 <sup>(3)</sup>
I/O	-	-	-	P116	391 <sup>(3)</sup>
I/O	-	-	-	P117	394 <sup>(3)</sup>
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 <sup>(3)</sup>
I/O	-	J12	P83	P120	400 <sup>(3)</sup>
VCC <sup>(2)</sup>	-	-	-	P121	-
I/O (D5 <sup>(2)</sup> )	P57	J13	P84	P122	403 <sup>(3)</sup>
I/O	P58	H10	P85	P123	406 <sup>(3)</sup>
I/O	-	-	-	P124	409 <sup>(3)</sup>
I/O	-	-	-	P125	412 <sup>(3)</sup>
I/O	P59	H11	P86	P126	415 <sup>(3)</sup>
I/O	P60	H12	P87	P127	418 <sup>(3)</sup>
I/O (D4 <sup>(2)</sup> )	P61	H13	P88	P128	421 <sup>(3)</sup>
I/O	P62	G12	P89	P129	424 <sup>(3)</sup>
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3 <sup>(2)</sup> )	P65	G10	P92	P132	427 <sup>(3)</sup>
I/O	P66	F13	P93	P133	430 <sup>(3)</sup>
I/O	P67	F12	P94	P134	433 <sup>(3)</sup>
I/O	-	F11	P95	P135	436 <sup>(3)</sup>
I/O	-	-	-	P136	439 <sup>(3)</sup>
I/O	-	-	-	P137	442 <sup>(3)</sup>
I/O (D2 <sup>(2)</sup> )	P68	F10	P96	P138	445 <sup>(3)</sup>
I/O	P69	E13	P97	P139	448 <sup>(3)</sup>
VCC <sup>(2)</sup>	-	-	-	P140	-
I/O	-	E12	P98	P141	451 <sup>(3)</sup>
I/O	-	E11	P99	P142	454 <sup>(3)</sup>
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 <sup>(3)</sup>
I/O	-	-	-	P146	460 <sup>(3)</sup>
I/O	-	-	-	P147	463 <sup>(3)</sup>
I/O	-	-	-	P148	466 <sup>(3)</sup>
I/O (D1 <sup>(2)</sup> )	P70	D13	P101	P149	469 <sup>(3)</sup>
I/O	P71	D12	P102	P150	472 <sup>(3)</sup>
I/O	-	D11	P103	P151	475 <sup>(3)</sup>

## XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 <sup>(2,4)</sup>	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 <sup>(3)</sup>
I/O (D0 <sup>(2)</sup> , DIN)	P72	C12	P105	P153	481 <sup>(3)</sup>
I/O, SGCK4 <sup>(1)</sup> , GCK6 <sup>(2)</sup> (DOUT)	P73	C11	P106	P154	484 <sup>(3)</sup>
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4 <sup>(1)</sup> , GCK7 <sup>(2)</sup>	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1 <sup>(2)</sup> )	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC <sup>(2)</sup>	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

2/8/00

### Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: Component Availability Chart for Spartan/XL FPGAs

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84 <sup>(3)</sup>	VQ100 <sup>(3)</sup>	CS144 <sup>(3)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(3)</sup>	CS280 <sup>(3)</sup>
XCS05	-3	C <sup>(3)</sup>	C, I	-	-	-	-	-	-
	-4	C <sup>(3)</sup>	C	-	-	-	-	-	-
XCS10	-3	C <sup>(3)</sup>	C, I	-	C	-	-	-	-
	-4	C <sup>(3)</sup>	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C <sup>(3)</sup>	-	C, I	C, I	C	C <sup>(3)</sup>	-
	-4	-	C <sup>(3)</sup>	-	C	C	C	C <sup>(3)</sup>	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C <sup>(3)</sup>	C, I	-	-	-	-	-	-
	-5	C <sup>(3)</sup>	C	-	-	-	-	-	-
XCS10XL	-4	C <sup>(3)</sup>	C, I	C <sup>(3)</sup>	C	-	-	-	-
	-5	C <sup>(3)</sup>	C	C <sup>(3)</sup>	C	-	-	-	-
XCS20XL	-4	-	C, I	C <sup>(3)</sup>	C, I	C, I	-	-	-
	-5	-	C	C <sup>(3)</sup>	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C <sup>(3)</sup>
	-5	-	C	-	C	C	C	C	C <sup>(3)</sup>
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C <sup>(3)</sup>
	-5	-	-	-	-	C	C	C	C <sup>(3)</sup>

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#### Notes:

1. C = Commercial  $T_J = 0^\circ$  to  $+85^\circ\text{C}$
2. I = Industrial  $T_J = -40^\circ\text{C}$  to  $+100^\circ\text{C}$
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

### Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

[www.xilinx.com/support/documentation/spartan-xl.htm#19687](http://www.xilinx.com/support/documentation/spartan-xl.htm#19687)

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

[www.xilinx.com/cgi-bin/thermal/thermal.pl](http://www.xilinx.com/cgi-bin/thermal/thermal.pl)