AMD Xilinx - XCS30XL-4TQ144C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	576
Number of Logic Elements/Cells	1368
Total RAM Bits	18432
Number of I/O	113
Number of Gates	30000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs30xl-4tq144c

Spartan and Spartan-XL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In addition to the conventional benefit of high volume programmable logic solutions, Spartan series FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan/XL families leverage the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA process developments.

Logic Functional Description

The Spartan series uses a standard FPGA structure as shown in Figure 1, page 2. The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in Figure 2. There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the **Advanced Features Description**, page 13.

Function Generators

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box "A" of Figure 2). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.

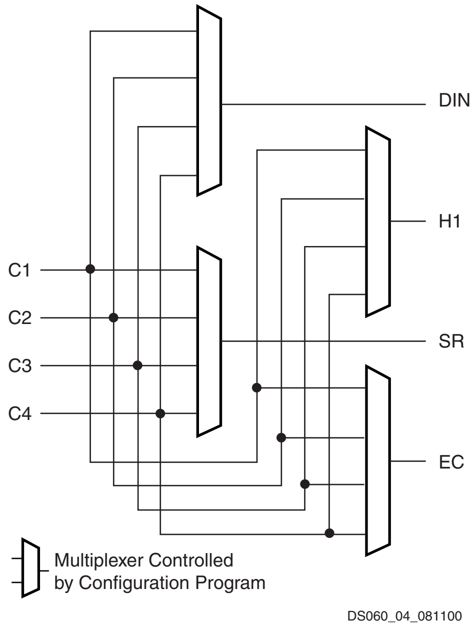


Figure 4: **CLB Control Signal Interface**

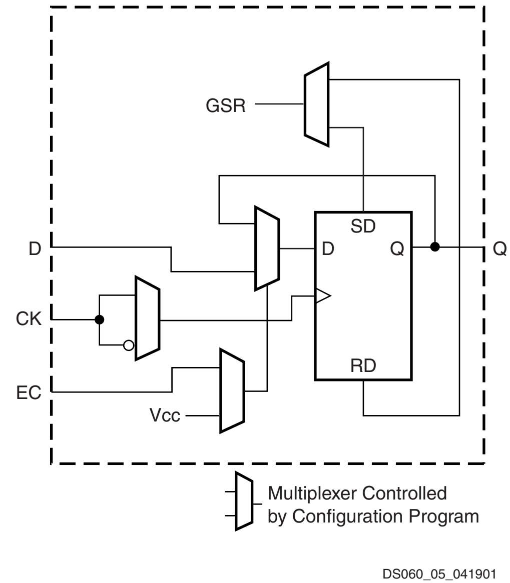


Figure 5: **IOB Flip-Flop/Latch Functional Block Diagram**

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: **Input Register Functionality**

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	_/‾	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care.
_/‾	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

CLB signals from which they are originally derived are shown in Table 10.

Table 10: **Dual-Port RAM Signals**

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F_{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G_{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: *"Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM,"* and *"Synchronous and Asynchronous FIFO Designs."* All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan

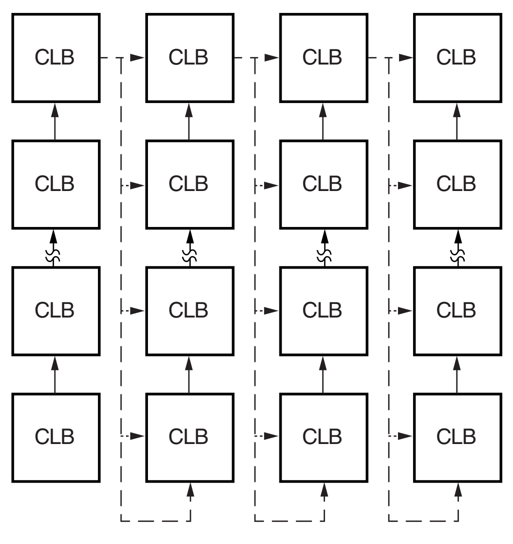


Figure 15: **Available Spartan/XL Carry Propagation Paths**

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.

Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is –50% to +25%.

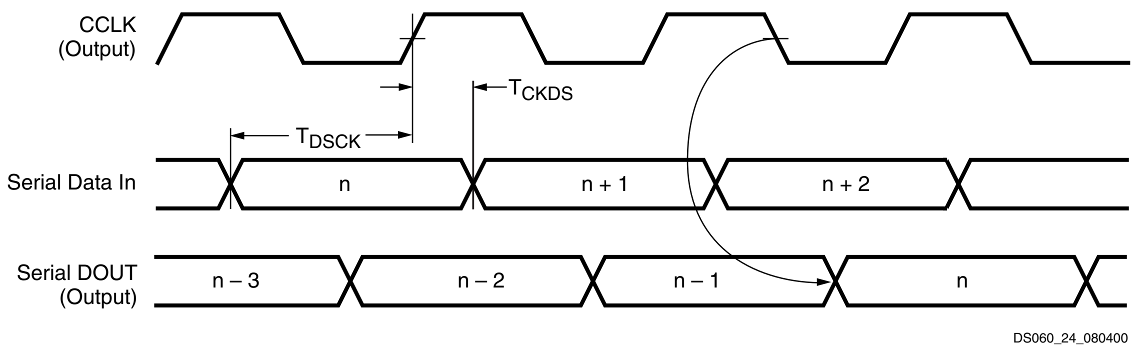
In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in Figure 24.

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Earlier families such as the XC3000 series do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

Figure 25 shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Symbol	Description	Min	Units
CCLK	T_{DSCK}	DIN setup	20	ns
	T_{CKDS}	DIN hold	0	ns

Notes:
1. At power-up, V_{CC} must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 24: **Master Serial Mode Programming Switching Characteristics**

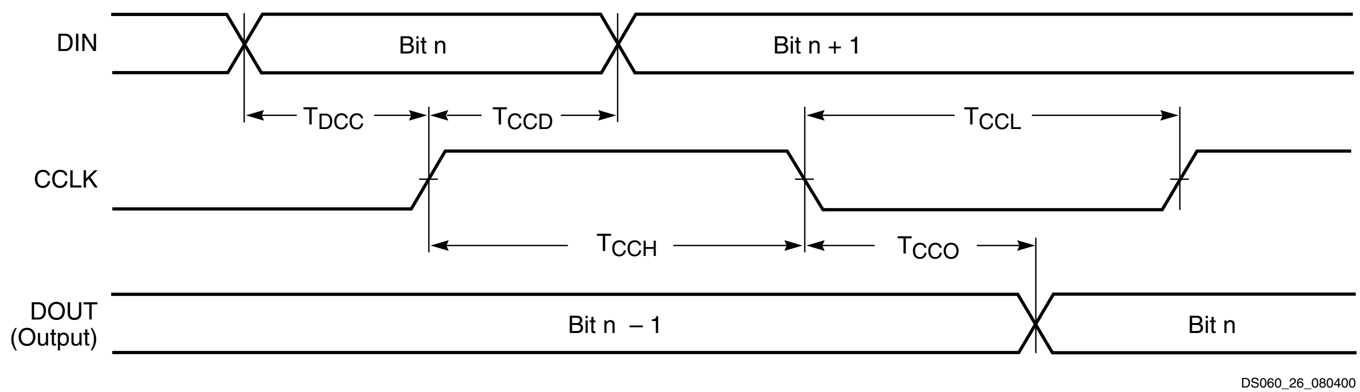
Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 25 shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.



Symbol		Description	Min	Max	Units
T_{DCC}	CCLK	DIN setup	20	-	ns
T_{CCD}		DIN hold	0	-	ns
T_{CCO}		DIN to DOUT	-	30	ns
T_{CCH}		High time	40	-	ns
T_{CCL}		Low time	40	-	ns
F_{CC}		Frequency	-	12.5	MHz

Notes:
1. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

Figure 26: **Slave Serial Mode Programming Switching Characteristics**

Express Mode (Spartan-XL Family Only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

Pseudo Daisy Chain

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.

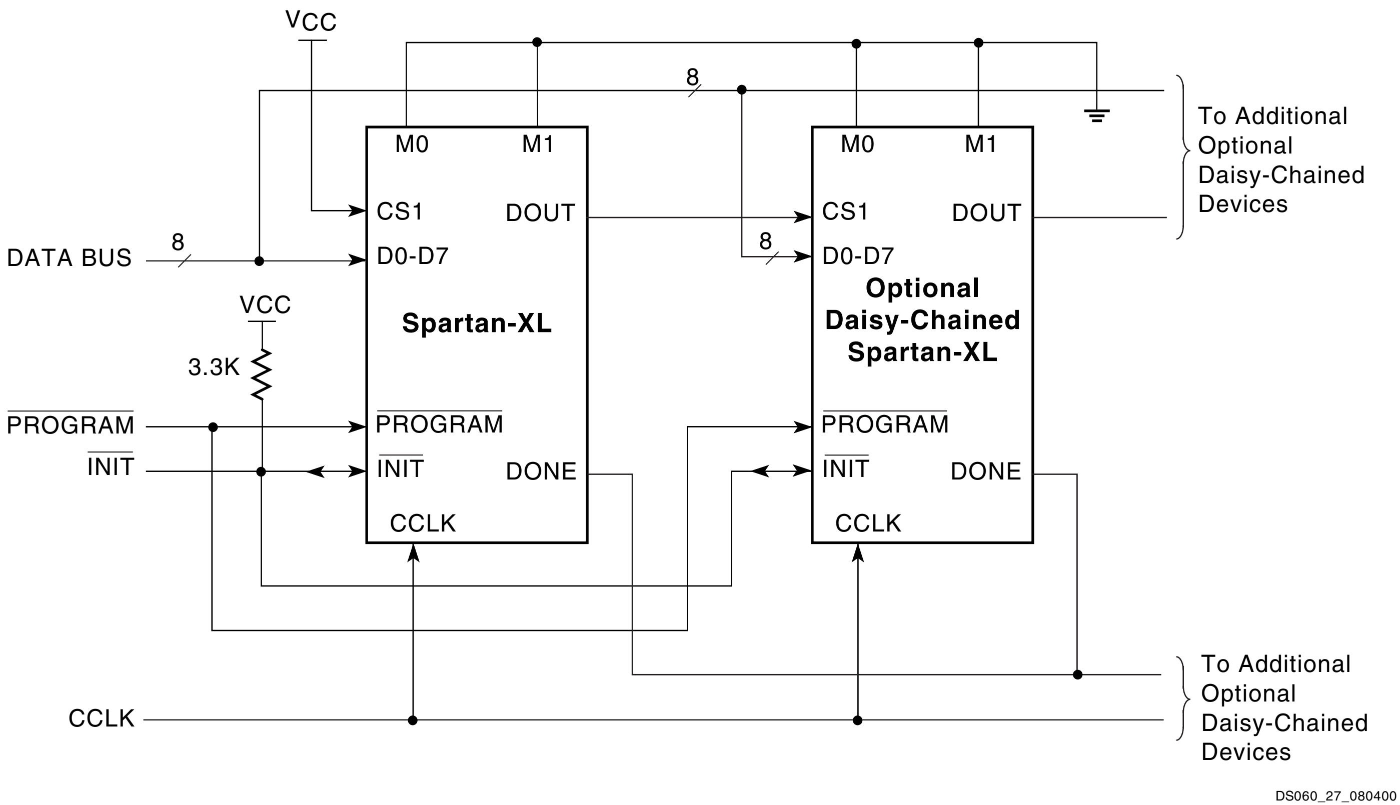


Figure 27: **Express Mode Circuit Diagram**

to wait after completing the configuration memory clear operation. When INIT is no longer held Low externally, the device determines its configuration mode by capturing the state of the Mode pins, and is ready to start the configuration process. A master device waits up to an additional 300 μs to make sure that any slaves in the optional daisy chain have seen that INIT is High.

For more details on Configuration, refer to the Xilinx Application Note "FPGA Configuration Guidelines" (XAPP090).

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user system. Start-up must make sure that the user logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the Global Set/Reset (GSR) at the right time.

Start-Up Initiation

Two conditions have to be met in order for the start-up sequence to begin:

- The chip's internal memory must be full, and
- The configuration length count must be met, exactly.

In all configuration modes except Express mode, Spartan/XL devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

In Express mode, there is no length count. The start-up sequence for each device begins when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

Start-Up Events

The device can be programmed to control three start-up events.

- The release of the open-drain DONE output
- The termination of the Global Three-State and the change of configuration-related pins to the user function, activating all IOBs.
- The termination of the Global Set/Reset initialization of all CLB and IOB storage elements.

Figure 31 describes start-up timing in detail. The three events — DONE going High, the internal GSR being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. This relative timing is selected by options in the bitstream generation software. Heavy lines in Figure 31 show the default timing. The thin lines indicate all other possible timing options. The start-up logic must be clocked until the "F" (Finished) state is reached.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. GSR is then released another clock period later to make sure that user operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 31, but the designer can modify it to meet particular requirements.

Start-Up Clock

Normally, the start-up sequence is controlled by the internal device oscillator (CCLK), which is asynchronous to the system clock. As a configuration option, they can be triggered by an on-chip user net called UCLK. This user net can be accessed by placing the STARTUP library symbol, and the start-up modes are known as UCLK_NOSYNC or UCLK_SYNC. This allows the device to wake up in synchronism with the user system.

DONE Pin

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to the start-up control logic. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK_SYNC or UCLK_SYNC. When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK_NOSYNC or UCLK_NOSYNC. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, while the other configuration modes can use any of the four timing sequences.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

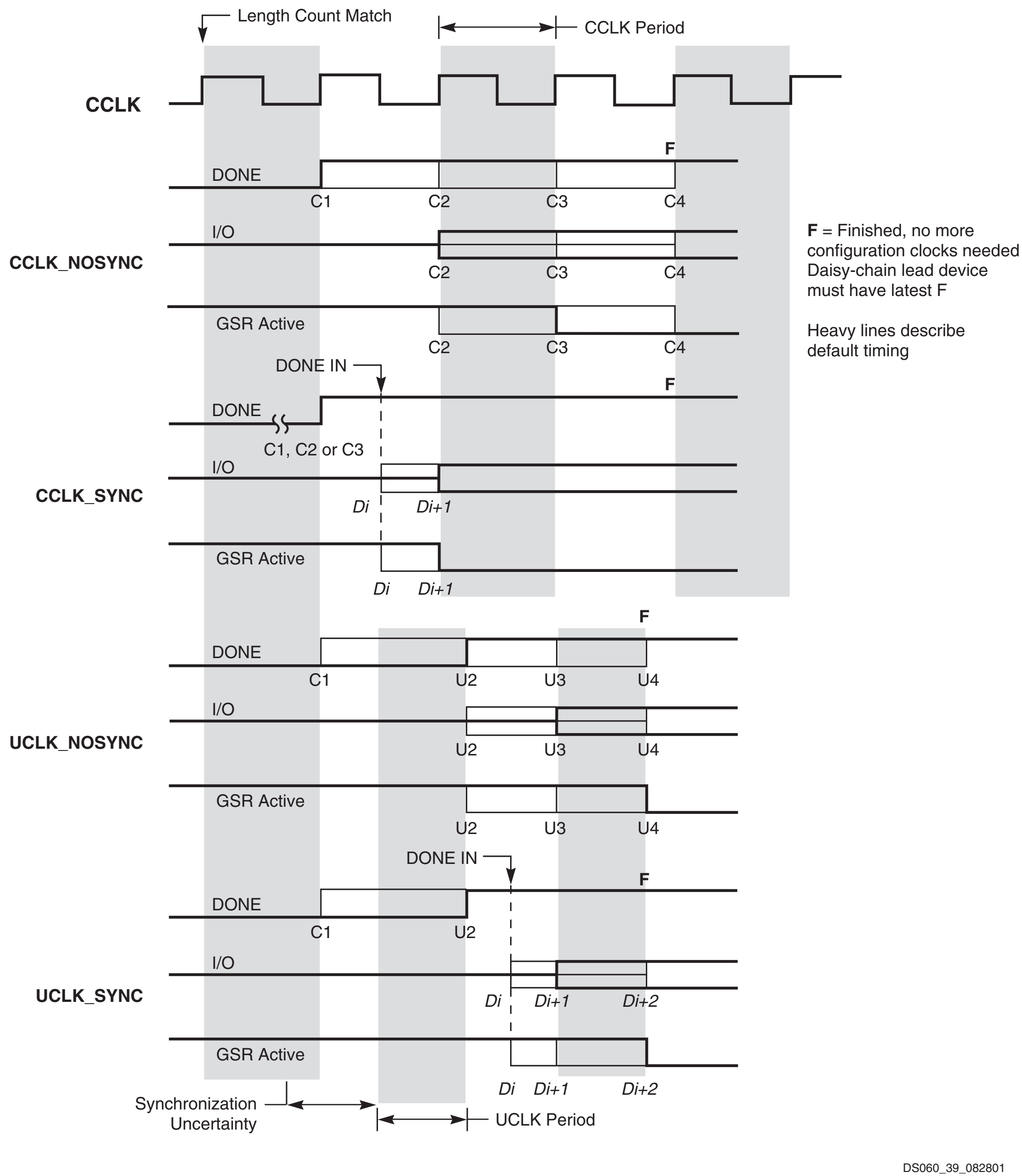


Figure 31: **Start-up Timing**

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input.
- Wait for $\overline{\text{INIT}}$ to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after $\overline{\text{INIT}}$ goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and Spartan-XL devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 32.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

Readback Capture

When the Readback Capture option is selected, the data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.

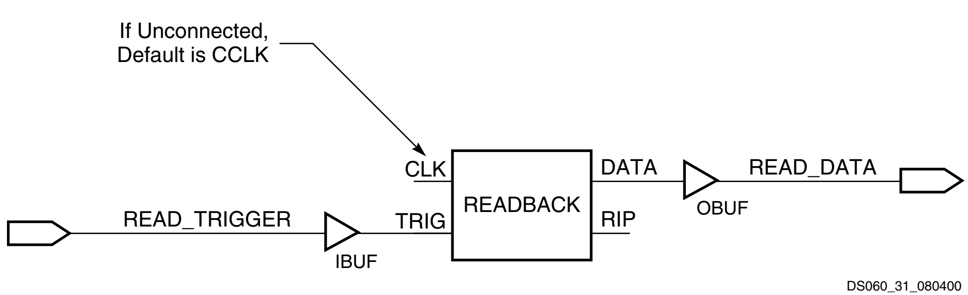
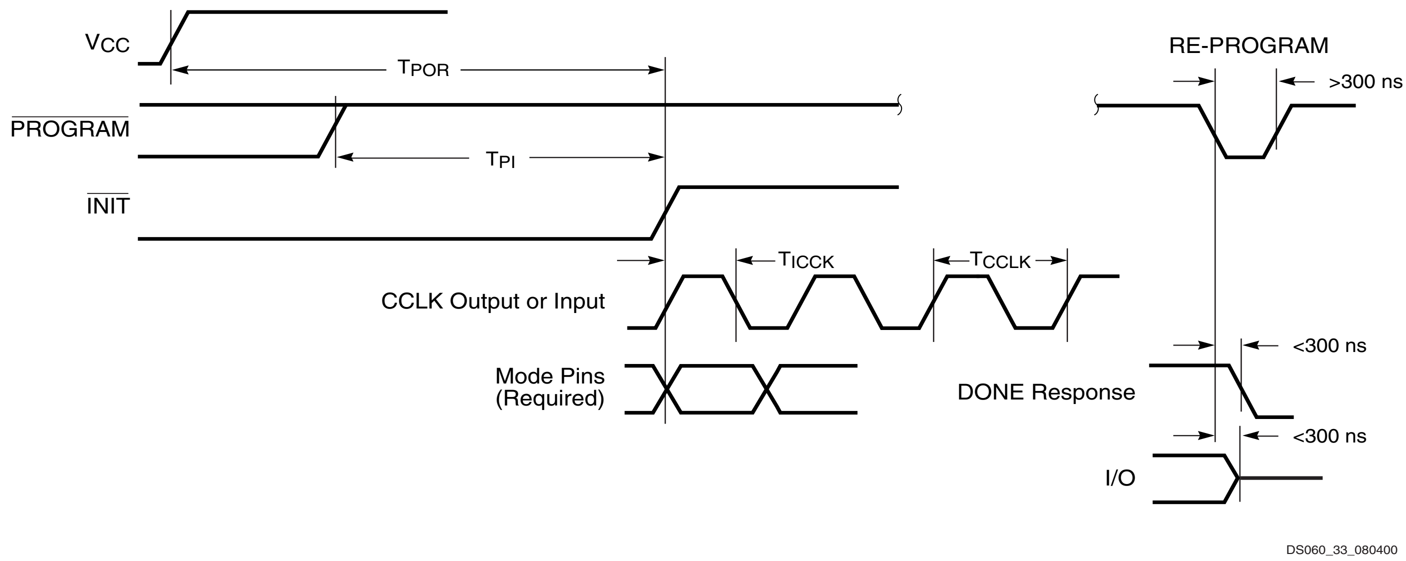


Figure 32: **Readback Example**

Configuration Switching Characteristics



Master Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	40	130	ms
T_{PI}	Program Latency	30	200	µs per CLB column
T_{ICCK}	CCLK (output) delay	40	250	µs
T_{CCLK}	CCLK (output) period, slow	640	2000	ns
T_{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	10	33	ms
T_{PI}	Program latency	30	200	µs per CLB column
T_{ICCK}	CCLK (input) delay (required)	4	-	µs
T_{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-4		-3		
		Min	Max	Min	Max	
Clocks						
T_{CH}	Clock High time	3.0	-	4.0	-	ns
T_{CL}	Clock Low time	3.0	-	4.0	-	ns
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	1.2	-	1.6	ns
T_{IHO}	F/G inputs via H to X/Y outputs	-	2.0	-	2.7	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.7	-	2.2	ns
CLB Fast Carry Logic						
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	1.7	-	2.1	ns
T_{ASCY}	Add/Subtract input (F3) to C_{OUT}	-	2.8	-	3.7	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	1.2	-	1.4	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	2.0	-	2.6	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.5	-	0.6	ns
Sequential Delays						
T_{CKO}	Clock K to Flip-Flop outputs Q	-	2.1	-	2.8	ns
Setup Time before Clock K						
T_{ICK}	F/G inputs	1.8	-	2.4	-	ns
T_{IHCK}	F/G inputs via H	2.9	-	3.9	-	ns
T_{HH1CK}	C inputs via H1 through H	2.3	-	3.3	-	ns
T_{DICK}	C inputs via DIN	1.3	-	2.0	-	ns
T_{ECCK}	C inputs via EC	2.0	-	2.6	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	2.5	-	4.0	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	3.0	-	4.0	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	3.0	-	4.0	ns
Global Set/Reset						
T_{MRW}	Minimum GSR pulse width	11.5	-	13.5	-	ns
T_{MRQ}	Delay from GSR input to any Q	See page 50 for T_{RRI} values per device.				
F_{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	166	-	125	MHz

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size(1)	Speed Grade -4 Min	Speed Grade -4 Max	Speed Grade -3 Min	Speed Grade -3 Max	Units
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T_{WCTS}		32x1	8.0	-	11.6	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T_{WPTS}		32x1	4.0	-	5.8	-	ns
T_{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T_{ASTS}		32x1	1.5	-	2.0	-	ns
T_{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{AHTS}		32x1	0.0	-	0.0	-	ns
T_{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T_{DSTS}		32x1	1.5	-	1.7	-	ns
T_{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{DHTS}		32x1	0.0	-	0.0	-	ns
T_{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T_{WSTS}		32x1	1.5	-	1.6	-	ns
T_{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{WHTS}		32x1	0.0	-	0.0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T_{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T_{RCT}		32x1	3.8	-	3.8	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T_{IHO}		32x1	-	2.0	-	2.7	ns
T_{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T_{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:
1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings[1]

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked[2, 3]	–0.5 to 5.5	V
		Not 5V Tolerant I/Os[4, 5]	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked[2, 3]	–0.5 to 5.5	V
		Not 5V Tolerant I/Os[4, 5]	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
5. Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0V or overshoot to V_{CC} + 2.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C[1]	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage[2]		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage[2]		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold is ~50% of V_{CC}.

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size(1)	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	7.7	-	8.4	-	ns
T_{WCTS}		32x1	7.7	-	8.4	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	3.1	-	3.6	-	ns
T_{WPTS}		32x1	3.1	-	3.6	-	ns
T_{ASS}	Address setup time before clock K	16x2	1.3	-	1.5	-	ns
T_{ASTS}		32x1	1.5	-	1.7	-	ns
T_{DSS}	DIN setup time before clock K	16x2	1.5	-	1.7	-	ns
T_{DSTS}		32x1	1.8	-	2.1	-	ns
T_{WSS}	WE setup time before clock K	16x2	1.4	-	1.6	-	ns
T_{WSTS}		32x1	1.3	-	1.5	-	ns
	All hold times after clock K	16x2	0.0	-	0.0	-	ns
T_{WOS}	Data valid after clock K	32x1	-	4.5	-	5.3	ns
T_{WOTS}		16x2	-	5.4	-	6.3	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	2.6	-	3.1	-	ns
T_{RCT}		32x1	3.8	-	5.5	-	ns
T_{ILO}	Data Valid after address change (no Write Enable)	16x2	-	1.0	-	1.1	ns
T_{IHO}		32x1	-	1.7	-	2.0	ns
T_{ICK}	Address setup time before clock K	16x2	0.6	-	0.7	-	ns
T_{IHCK}		32x1	1.3	-	1.6	-	ns

Notes:
1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Table 18: **Pin Descriptions *(Continued)***

Pin Name	I/O During Config.	I/O After Config.	Pin Description
PWRDWN	I	I	PWRDWN is an active Low input that forces the FPGA into the Power Down state and reduces power consumption. When PWRDWN is Low, the FPGA disables all I/O and initializes all flip-flops. All inputs are interpreted as Low independent of their actual level. VCC must be maintained, and the configuration data is maintained. PWRDWN halts configuration if asserted before or during configuration, and re-starts configuration when removed. When PWRDWN returns High, the FPGA becomes operational by first enabling the inputs and flip-flops and then enabling the outputs. PWRDWN has a default internal pull-up resistor.
User I/O Pins That Can Have Special Functions			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
LDC	O	I/O	Low During Configuration (LDC) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, LDC is a user-programmable I/O pin.
INIT	I/O	I/O	Before and during configuration, INIT is a bidirectional signal. A 1 kΩ to 10 kΩ external pull-up resistor is recommended. As an active Low open-drain output, INIT is held Low during the power stabilization and internal clearing of the configuration memory. As an active Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 μs after INIT has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, INIT is a user-programmable I/O pin.
PGCK1 - PGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.

Table 18: **Pin Descriptions *(Continued)***

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and Spartan-XL device. They follow the pad locations around the die, and include boundary scan register locations.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84(4)	VQ100	Bndry Scan
VCC	P2	P89	-
I/O	P3	P90	32
I/O	P4	P91	35
I/O	-	P92	38
I/O	-	P93	41
I/O	P5	P94	44
I/O	P6	P95	47
I/O	P7	P96	50
I/O	P8	P97	53
I/O	P9	P98	56
I/O, SGCK1(1), GCK8(2)	P10	P99	59
VCC	P11	P100	-
GND	P12	P1	-
I/O, PGCK1(1), GCK1(2)	P13	P2	62
I/O	P14	P3	65
I/O, TDI	P15	P4	68
I/O, TCK	P16	P5	71
I/O, TMS	P17	P6	74
I/O	P18	P7	77
I/O	-	P8	83
I/O	P19	P9	86
I/O	P20	P10	89
GND	P21	P11	-
VCC	P22	P12	-
I/O	P23	P13	92
I/O	P24	P14	95
I/O	-	P15	98
I/O	P25	P16	104
I/O	P26	P17	107
I/O	P27	P18	110
I/O	-	P19	113
I/O	P28	P20	116
I/O, SGCK2(1), GCK2(2)	P29	P21	119
Not Connected(1), M1(2)	P30	P22	122
GND	P31	P23	-
MODE(1), M0 (2)	P32	P24	125
VCC	P33	P25	-

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84(4)	VQ100	Bndry Scan
Not Connected(1), $\overline{\text{PWRDWN}}$(2)	P34	P26	126(1)
I/O, PGCK2(1), GCK3 (2)	P35	P27	127(3)
I/O (HDC)	P36	P28	130(3)
I/O	-	P29	133(3)
I/O ($\overline{\text{LDC}}$)	P37	P30	136(3)
I/O	P38	P31	139(3)
I/O	P39	P32	142(3)
I/O	-	P33	145(3)
I/O	-	P34	148(3)
I/O	P40	P35	151(3)
I/O ($\overline{\text{INIT}}$)	P41	P36	154(3)
VCC	P42	P37	-
GND	P43	P38	-
I/O	P44	P39	157(3)
I/O	P45	P40	160(3)
I/O	-	P41	163(3)
I/O	-	P42	166(3)
I/O	P46	P43	169(3)
I/O	P47	P44	172(3)
I/O	P48	P45	175(3)
I/O	P49	P46	178(3)
I/O	P50	P47	181(3)
I/O, SGCK3(1), GCK4(2)	P51	P48	184(3)
GND	P52	P49	-
DONE	P53	P50	-
VCC	P54	P51	-
$\overline{\text{PROGRAM}}$	P55	P52	-
I/O (D7(2))	P56	P53	187(3)
I/O, PGCK3(1), GCK5(2)	P57	P54	190(3)
I/O (D6(2))	P58	P55	193(3)
I/O	-	P56	196(3)
I/O (D5(2))	P59	P57	199(3)
I/O	P60	P58	202(3)
I/O	-	P59	205(3)
I/O	-	P60	208(3)
I/O (D4(2))	P61	P61	211(3)
I/O	P62	P62	214(3)
VCC	P63	P63	-
GND	P64	P64	-
I/O (D3(2))	P65	P65	217(3)
I/O	P66	P66	220(3)
I/O	-	P67	223(3)
I/O (D2(2))	P67	P68	229(3)
I/O	P68	P69	232(3)
I/O (D1(2))	P69	P70	235(3)

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
O, TDO	P157	P181	A19	B17	0
GND	P158	P182	GND(4)	GND(4)	-
I/O	P159	P183	B18	A18	2
I/O, PGCK4(1), GCK7(2)	P160	P184	B17	A17	5
I/O	P161	P185	C17	D16	8
I/O	P162	P186	D16	C16	11
I/O (CS1(2))	P163	P187	A18	B16	14
I/O	P164	P188	A17	A16	17
I/O	-	-	-	E15	20
I/O	-	-	-	C15	23
I/O	P165	P189	C16	D15	26
I/O	-	P190	B16	A15	29
I/O	P166	P191	A16	E14	32
I/O	P167	P192	C15	C14	35
I/O	P168	P193	B15	B14	38
I/O	P169	P194	A15	D14	41
GND	P170	P196	GND(4)	GND(4)	-
I/O	P171	P197	B14	A14	44
I/O	P172	P198	A14	C13	47
I/O	-	P199	C13	B13	50
I/O	-	P200	B13	A13	53
VCC	P173	P201	VCC(4)	VCC(4)	-
I/O	-	-	A13	A12	56
I/O	-	-	D12	C12	59
I/O	P174	P202	C12	B12	62
I/O	P175	P203	B12	D12	65
I/O	P176	P205	A12	A11	68
I/O	P177	P206	B11	B11	71
I/O	P178	P207	C11	C11	74
I/O	P179	P208	A11	D11	77
I/O	P180	P209	A10	A10	80
I/O	P181	P210	B10	B10	83
GND	P182	P211	GND(4)	GND(4)	-

2/8/00

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS40XL is not part of the Boundary Scan chain. For the XCS40XL, subtract 1 from all Boundary Scan numbers from GCK3 on (343 and higher).
4. Pads labeled GND(4) or V_{CC}(4) are internally bonded to Ground or V_{CC} planes within the package.
5. CS280 package discontinued by PDN2004-01

Additional XCS40/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

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CS280

VCC Pins					
A1	A7	B5	B15	C10	C17
D13	E3	E18	G1	G19	K2
K17	M4	N16	R3	R18	T7
U3	U10	U17	V5	V15	W13
GND Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-

5/19/99

Table 20: **User I/O Chart for Spartan/XL FPGAs**

Device	Max I/O	Package Type							
		PC84[1]	VQ100[1]	CS144[1]	TQ144	PQ208	PQ240	BG256[1]	CS280[1]
XCS05	80	61[1]	77	-	-	-	-	-	-
XCS10	112	61[1]	77	-	112	-	-	-	-
XCS20	160	-	77	-	113	160	-	-	-
XCS30	192	-	77[1]	-	113	169	192	192[1]	-
XCS40	224	-	-	-	-	169	192	205	-
XCS05XL	80	61[1]	77[2]	-	-	-	-	-	-
XCS10XL	112	61[1]	77[2]	112[1]	112[2]	-	-	-	-
XCS20XL	160	-	77[2]	113[1]	113[2]	160[2]	-	-	-
XCS30XL	192	-	77[2]	-	113[2]	169[2]	192[2]	192[2]	192[1]
XCS40XL	224	-	-	-	-	169[2]	192[2]	205[2]	224[1]

6/25/08

Notes:
1. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01
2. These Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Ordering Information

Example: XCS20XL-4 PQ208C

Device Type

Speed Grade
- -3
- -4
- -5

Package Type

Number of Pins

Temperature Range
- C = Commercial (T_J = 0° to +85°C)
- I = Industrial (T_J = –40°C to +100°C)

BG = Ball Grid Array
BGG = Ball Grid Array (Pb-free)
PC = Plastic Lead Chip Carrier
PQ = Plastic Quad Flat Pack
PQG = Plastic Quad Flat Pack (Pb-free)
VQ = Very Thin Quad Flat Pack
VQG = Very Thin Quad Flat Pack (Pb-free)
TQ = Thin Quad Flat Pack
TQG = Thin Quad Flat Pack (Pb-free)
CS = Chip Scale