AMD Xilinx - XCS30XL-4TQG144I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	576
Number of Logic Elements/Cells	1368
Total RAM Bits	18432
Number of I/O	113
Number of Gates	30000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs30xl-4tqg144i

Table 4: **Supported Sources for Spartan/XL Inputs**

Source	Spartan Inputs 5V, TTL	Spartan Inputs 5V, CMOS	Spartan-XL Inputs 3.3V CMOS
Any device, V_{CC} = 3.3V, CMOS outputs	√	Unreliable Data	√
Spartan family, V_{CC} = 5V, TTL outputs	√		√
Any device, V_{CC} = 5V, TTL outputs ($V_{OH} \leq 3.7V$)	√		√
Any device, V_{CC} = 5V, CMOS outputs	√	√	√ (default mode)

Spartan-XL Family V_{CC} Clamping

Spartan-XL FPGAs have an optional clamping diode connected from each I/O to V_{CC}. When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. V_{CC} clamping is a global option affecting all I/O pins.

Spartan-XL devices are fully 5V TTL I/O compatible if V_{CC} clamping is not enabled. With V_{CC} clamping enabled, the Spartan-XL devices will begin to clamp input voltages to one diode voltage drop above V_{CC}. If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

Spartan-XL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 5.

Table 5: **I/O Standards Supported by Spartan-XL FPGAs**

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}
LVCMOS 3V	OK	12/24 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}

Additional Fast Capture Input Latch (Spartan-XL Family Only)

The Spartan-XL family OB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active High input flip-flop. ILFLX is a transparent Low Fast Capture latch followed by a transparent High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 6.

Table 6: **Output Flip-Flop Functionality**

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	↑	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
↑	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

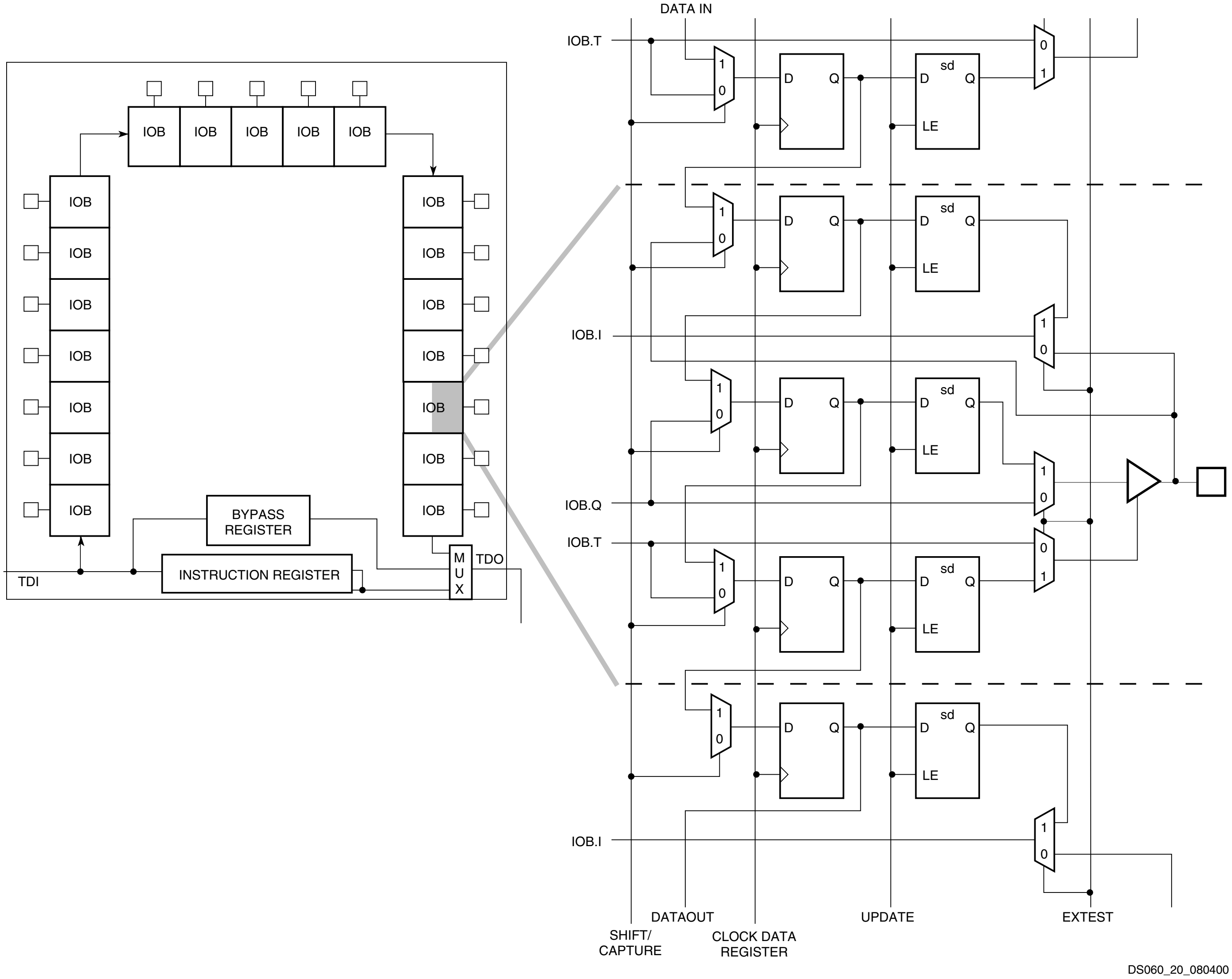


Figure 20: **Spartan/XL Boundary Scan Logic**

Table 12: **Boundary Scan Instructions**

Instruction			Test Selected	TDO Source	I/O Data Source
I2	**I1**	**I0**			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	IDCODE (Spartan-XL only)	IDCODE Register	-
1	1	1	BYPASS	Bypass Register	-

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-state. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 21. The device-specific pinout tables for the Spartan/XL devices include the boundary scan locations for each IOB pin.

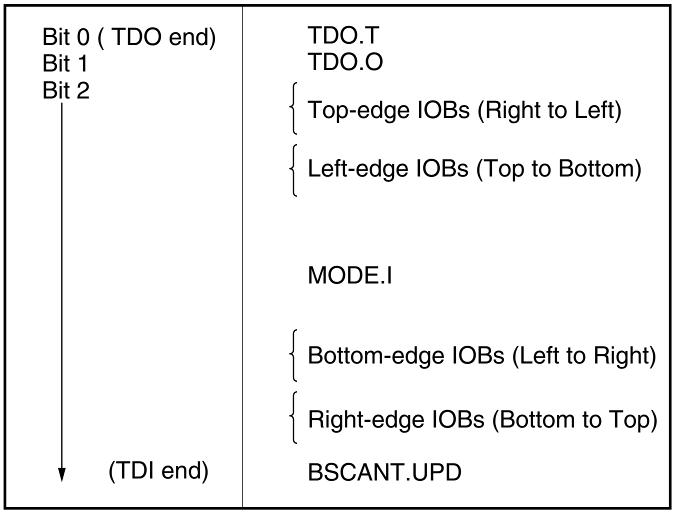


Figure 21: **Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Spartan/XL devices are available on the Xilinx website in the File Download area. Note that the 5V Spartan devices and 3V Spartan-XL devices have different BSDL files.

Including Boundary Scan in a Design

If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 22.

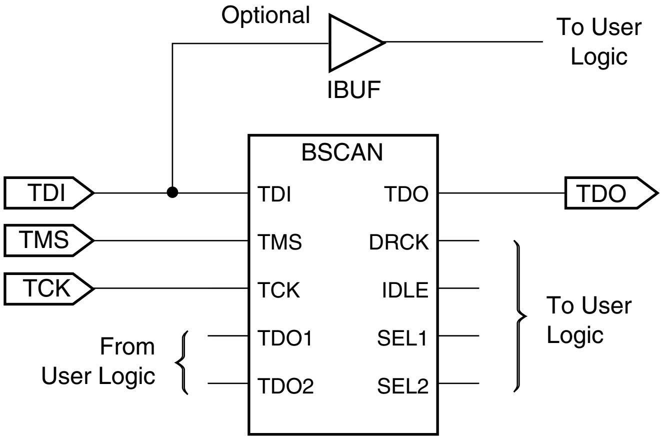


Figure 22: **Boundary Scan Example**

Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is –50% to +25%.

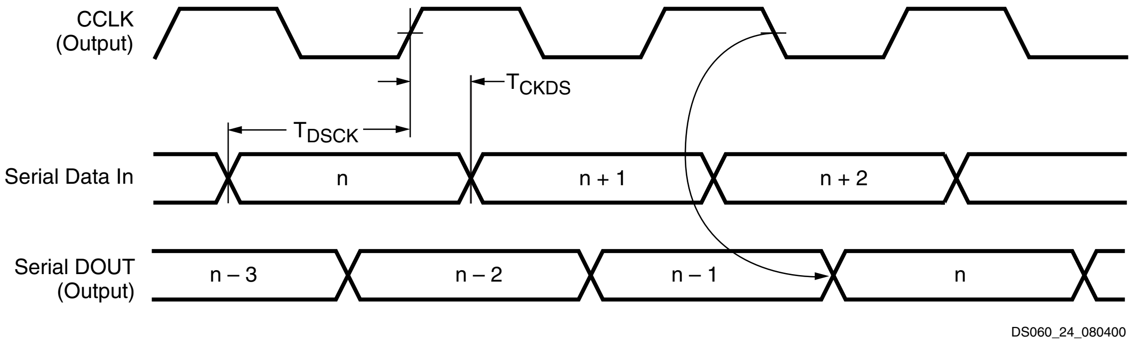
In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in Figure 24.

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Earlier families such as the XC3000 series do not support the Fast Configuration Rate option.

The SPROM $\overline{\text{CE}}$ input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

Figure 25 shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Symbol	Description	Min	Units
CCLK	T_{DSCK}	DIN setup	20	ns
	T_{CKDS}	DIN hold	0	ns

Notes:

1. At power-up, V_{CC} must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 24: **Master Serial Mode Programming Switching Characteristics**

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 25 shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.

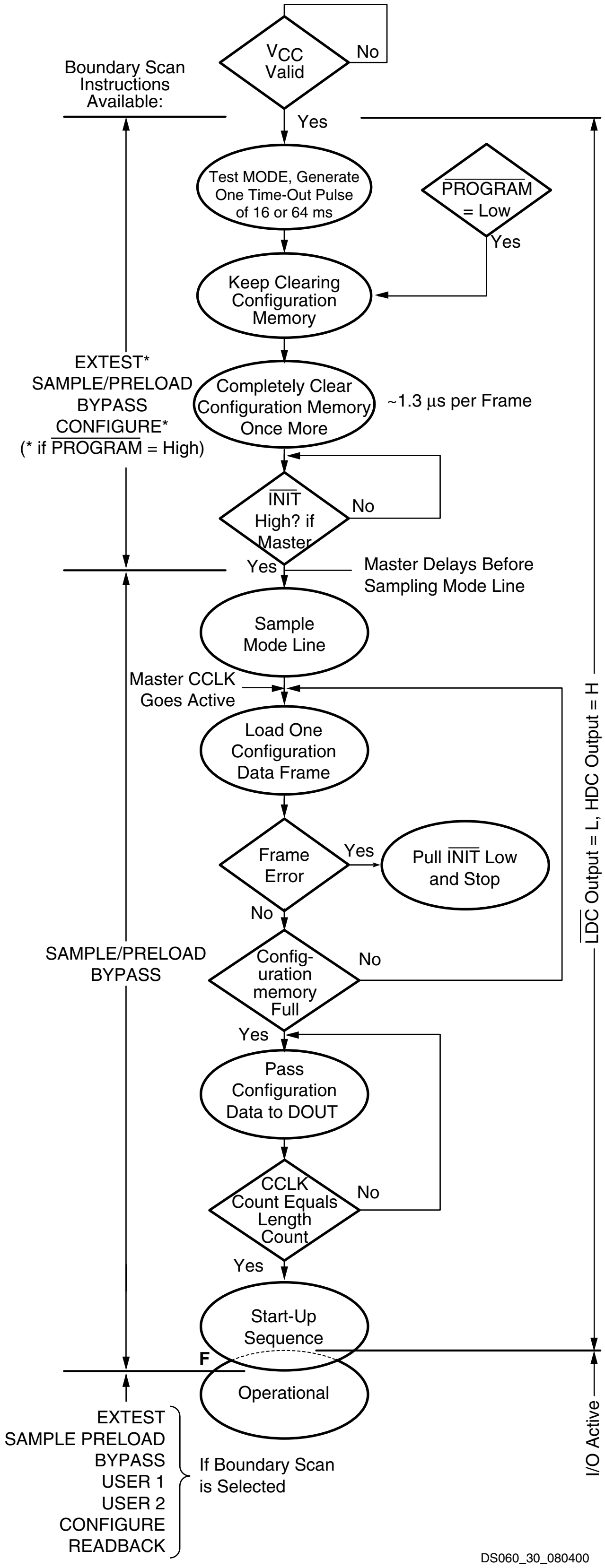


Figure 30: **Power-up Configuration Sequence**

Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count for serial modes. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Spartan-XL family Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain INIT pin Low. After all configuration frames have been loaded into an FPGA using a serial mode, DOUT again follows the input data so that the remaining data is passed on to the next device. In Spartan-XL family Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the PROGRAM input, or pull the bidirectional INIT pin Low, using an open-collector (open-drain) driver. (See Figure 30.)

A Low on the PROGRAM input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as PROGRAM is Low, the FPGA keeps clearing its configuration memory. When PROGRAM goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the PROGRAM input automatically forces a Low on the INIT output. The Spartan/XL FPGA PROGRAM pin has a permanent weak pull-up.

Avoid holding PROGRAM Low for more than 500 µs. The 500 µs maximum limit is only a recommendation, not a requirement. The only effect of holding PROGRAM Low for more than 500 µs is an increase in current, measured at about 40 mA in the XCS40XL. This increased current cannot damage the device. This applies only during reconfiguration, not during power-up. The INIT pin can also be held Low to delay reconfiguration, and the same characteristics apply as for the PROGRAM pin.

Using an open-collector or open-drain driver to hold INIT Low before the beginning of configuration causes the FPGA

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 32.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

Readback Capture

When the Readback Capture option is selected, the data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.

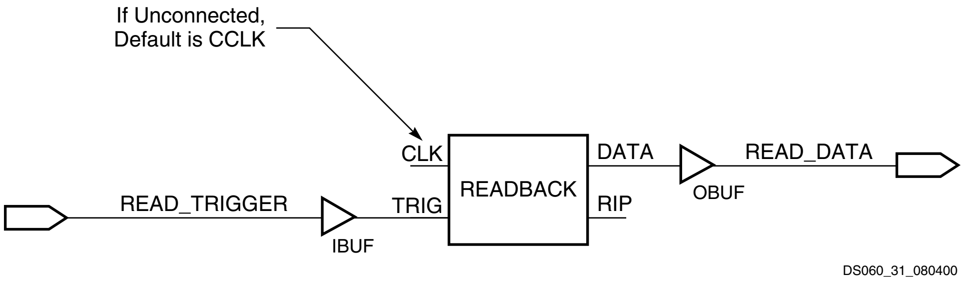


Figure 32: **Readback Example**

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.

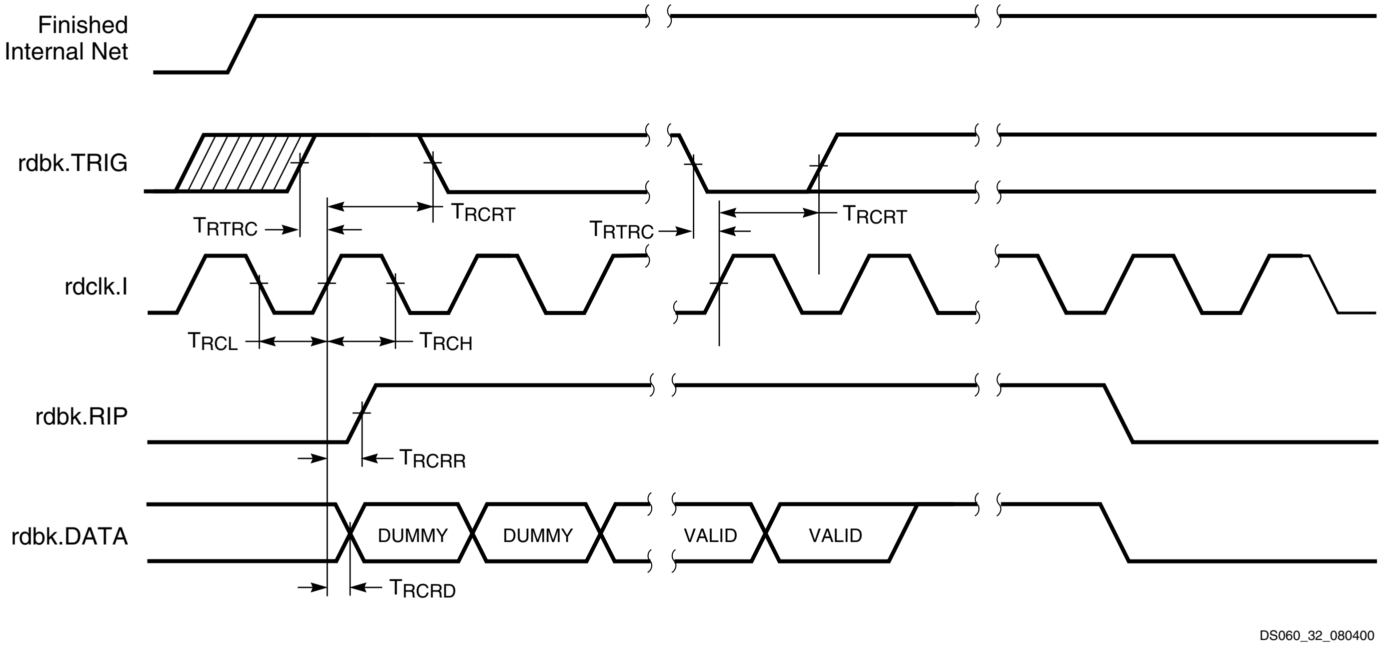


Figure 33: **Spartan and Spartan-XL Readback Timing Diagram**

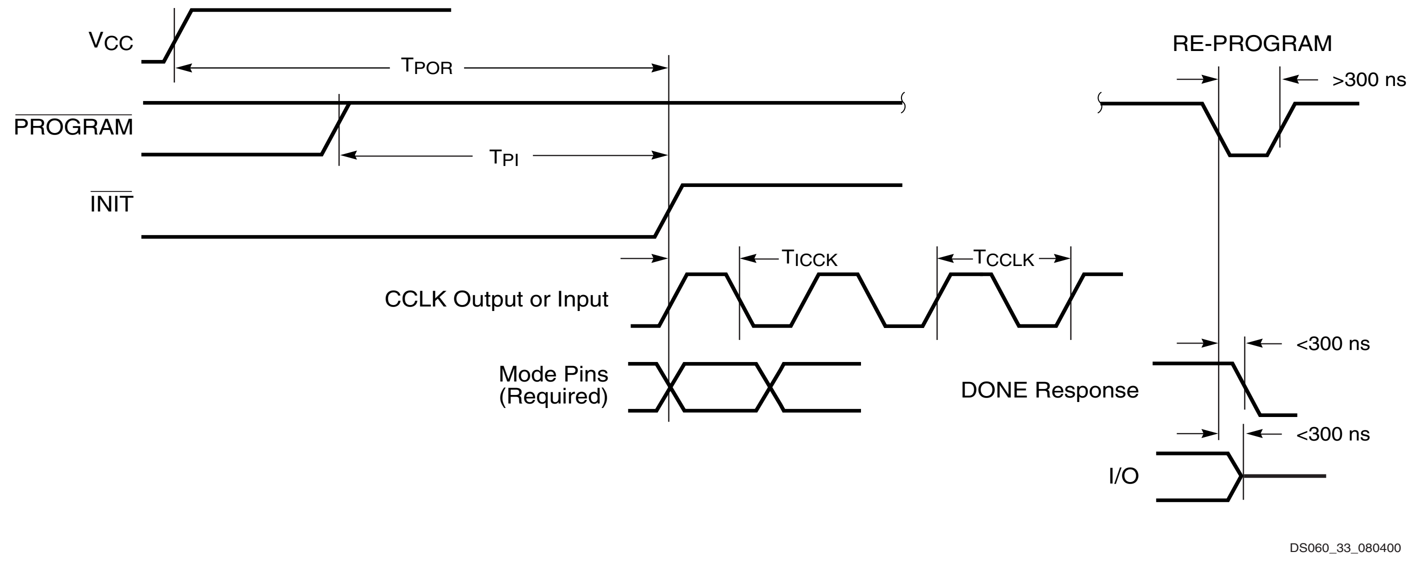
Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:

1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Configuration Switching Characteristics



Master Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	40	130	ms
T_{PI}	Program Latency	30	200	µs per CLB column
T_{ICCK}	CCLK (output) delay	40	250	µs
T_{CCLK}	CCLK (output) period, slow	640	2000	ns
T_{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	10	33	ms
T_{PI}	Program latency	30	200	µs per CLB column
T_{ICCK}	CCLK (input) delay (required)	4	-	µs
T_{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ $I_{OH} = –4.0$ mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage @ $I_{OH} = –1.0$ mA, V_{CC} min	CMOS outputs	$V_{CC} – 0.5$	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min(1)	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		3.0	-	V
I_{CCO}	Quiescent FPGA supply current(2)	Commercial	-	3.0	mA
		Industrial	-	6.0	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)		-	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 5V (sample tested)		0.02	-	mA

Notes:

1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a Tie option.

Spartan Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade -4 Max	Speed Grade -3 Max	Units
T_{PG}	From pad through Primary buffer, to any clock K	XCS05	2.0	4.0	ns
		XCS10	2.4	4.3	ns
		XCS20	2.8	5.4	ns
		XCS30	3.2	5.8	ns
		XCS40	3.5	6.4	ns
T_{SG}	From pad through Secondary buffer, to any clock K	XCS05	2.5	4.4	ns
		XCS10	2.9	4.7	ns
		XCS20	3.3	5.8	ns
		XCS30	3.6	6.2	ns
		XCS40	3.9	6.7	ns

Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-4		-3		
		Min	Max	Min	Max	
Clocks						
T_{CH}	Clock High time	3.0	-	4.0	-	ns
T_{CL}	Clock Low time	3.0	-	4.0	-	ns
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	1.2	-	1.6	ns
T_{IHO}	F/G inputs via H to X/Y outputs	-	2.0	-	2.7	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.7	-	2.2	ns
CLB Fast Carry Logic						
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	1.7	-	2.1	ns
T_{ASCY}	Add/Subtract input (F3) to C_{OUT}	-	2.8	-	3.7	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	1.2	-	1.4	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	2.0	-	2.6	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.5	-	0.6	ns
Sequential Delays						
T_{CKO}	Clock K to Flip-Flop outputs Q	-	2.1	-	2.8	ns
Setup Time before Clock K						
T_{ICK}	F/G inputs	1.8	-	2.4	-	ns
T_{IHCK}	F/G inputs via H	2.9	-	3.9	-	ns
T_{HH1CK}	C inputs via H1 through H	2.3	-	3.3	-	ns
T_{DICK}	C inputs via DIN	1.3	-	2.0	-	ns
T_{ECCK}	C inputs via EC	2.0	-	2.6	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	2.5	-	4.0	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	3.0	-	4.0	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	3.0	-	4.0	ns
Global Set/Reset						
T_{MRW}	Minimum GSR pulse width	11.5	-	13.5	-	ns
T_{MRQ}	Delay from GSR input to any Q	See page 50 for T_{RRI} values per device.				
F_{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	166	-	125	MHz

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size(1)	Speed Grade -4 Min	Speed Grade -4 Max	Speed Grade -3 Min	Speed Grade -3 Max	Units
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T_{WCTS}		32x1	8.0	-	11.6	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T_{WPTS}		32x1	4.0	-	5.8	-	ns
T_{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T_{ASTS}		32x1	1.5	-	2.0	-	ns
T_{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{AHTS}		32x1	0.0	-	0.0	-	ns
T_{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T_{DSTS}		32x1	1.5	-	1.7	-	ns
T_{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{DHTS}		32x1	0.0	-	0.0	-	ns
T_{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T_{WSTS}		32x1	1.5	-	1.6	-	ns
T_{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{WHTS}		32x1	0.0	-	0.0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T_{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T_{RCT}		32x1	3.8	-	3.8	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T_{IHO}		32x1	-	2.0	-	2.7	ns
T_{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T_{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

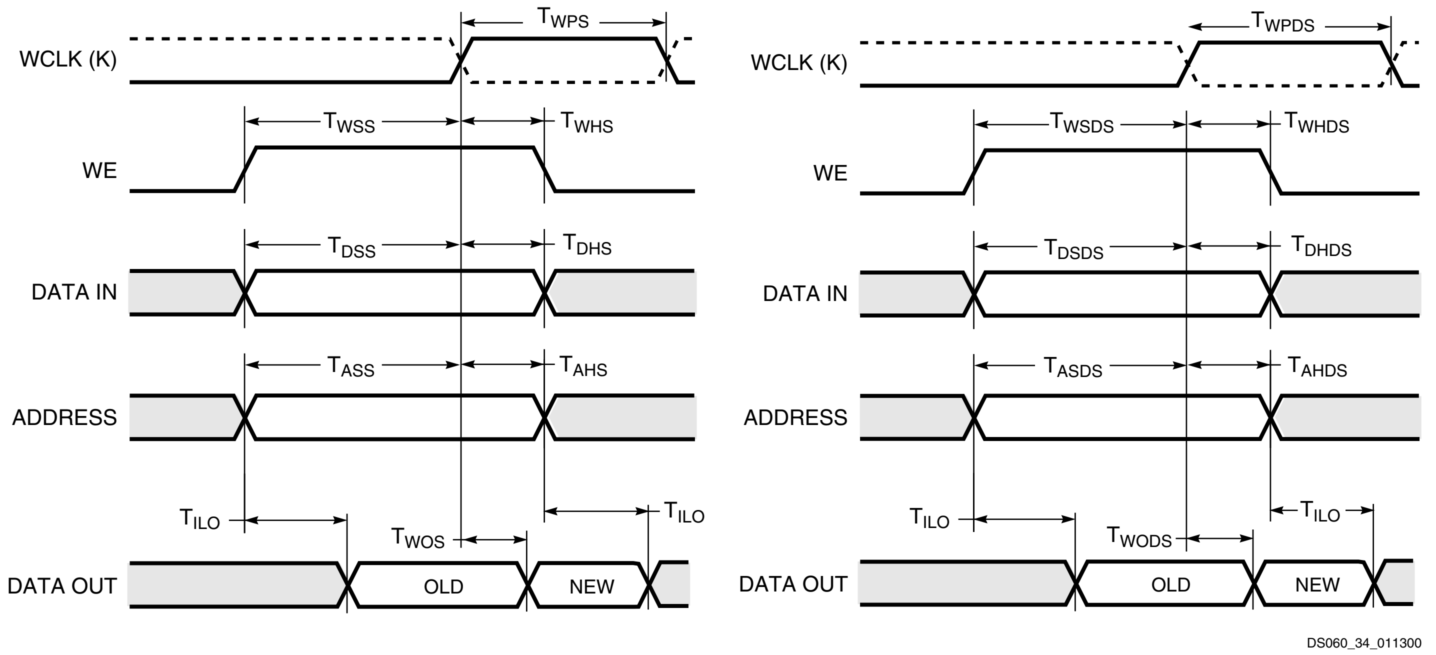
Symbol	Dual Port RAM	Size(1)	-4		-3		Units
			Min	Max	Min	Max	
Write Operation							
T_{WCDS}	Address write cycle time (clock K period)	16x1	8.0	-	11.6	-	ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	4.0	-	5.8	-	ns
T_{ASDS}	Address setup time before clock K	16x1	1.5	-	2.1	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	0	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	1.5	-	1.6	-	ns
T_{DHDS}	DIN hold time after clock K	16x1	0	-	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.5	-	1.6	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	6.5	-	7.0	ns

Notes:

1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port **Dual Port**



Spartan-XL Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
T_{GLS}	From pad through buffer, to any clock K	XCS05XL	1.4	1.5	ns
		XCS10XL	1.7	1.8	ns
		XCS20XL	2.0	2.1	ns
		XCS30XL	2.3	2.5	ns
		XCS40XL	2.6	2.8	ns

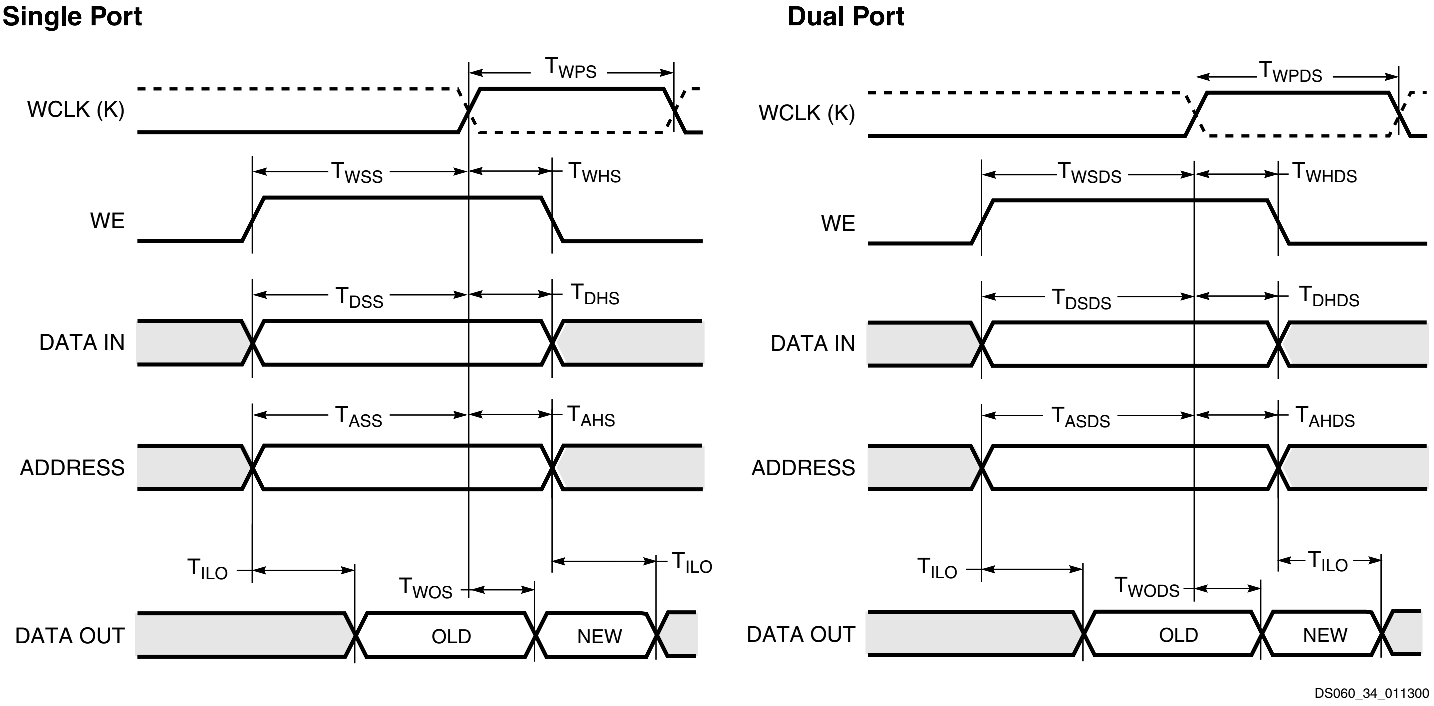
Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation[1]							
T_{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T_{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

Notes:
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing



Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Setup Times							
T_{ECIK}	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T_{PICK}	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T_{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T_{PID}	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T_{Delay}	$T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T_{RRI}	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See **Global Signals: GSR and GTS**, page 20 for more information.

Device pins for Spartan/XL devices are described in Table 18.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

Table 18: **Pin Descriptions**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
V_{CC}	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 –0.1 µF capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See **Violating the Maximum High and Low Time Specification for the Readback Clock**, page 39 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an open-drain output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC(2)	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2(1), GCK2(2)	P21	L2	P33	P49	239
Not Connected(1) M1(2)	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE(1), M0(2)	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected(1) $\overline{\text{PWRDWN}}$(2)	P26	N2	P38	P54	246 (1)
I/O, PGCK2(1), GCK3(2)	P27	M3	P39	P55	247 (3)
I/O (HDC)	P28	N3	P40	P56	250 (3)
I/O	-	K4	P41	P57	253 (3)
I/O	-	L4	P42	P58	256 (3)
I/O	P29	M4	P43	P59	259 (3)

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144(2,4)	TQ144	PQ208	Bndry Scan
I/O ($\overline{\text{LDC}}$)	P30	N4	P44	P60	262 (3)
I/O	-	-	-	P61	265 (3)
I/O	-	-	-	P62	268 (3)
I/O	-	-	-	P63	271 (3)
I/O	-	-	-	P64	274 (3)
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 (3)
I/O	-	M5	P47	P68	280 (3)
I/O	P31	N5	P48	P69	283 (3)
I/O	P32	K6	P49	P70	286 (3)
VCC(2)	-	-	-	P71	-
I/O	-	-	-	P72	289 (3)
I/O	-	-	-	P73	292 (3)
I/O	P33	L6	P50	P74	295 (3)
I/O	P34	M6	P51	P75	298 (3)
I/O	P35	N6	P52	P76	301 (3)
I/O ($\overline{\text{INIT}}$)	P36	M7	P53	P77	304 (3)
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 (3)
I/O	P40	N8	P57	P81	310 (3)
I/O	P41	M8	P58	P82	313 (3)
I/O	P42	L8	P59	P83	316 (3)
I/O	-	-	-	P84	319 (3)
I/O	-	-	-	P85	322 (3)
VCC(2)	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 (3)
I/O	P44	N9	P61	P88	328 (3)
I/O	-	M9	P62	P89	331 (3)
I/O	-	L9	P63	P90	334 (3)
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 (3)
I/O	-	-	-	P94	340 (3)
I/O	-	-	-	P95	343 (3)
I/O	-	-	-	P96	346 (3)
I/O	P45	N10	P65	P97	349 (3)
I/O	P46	M10	P66	P98	352 (3)
I/O	-	L10	P67	P99	355 (3)
I/O	-	N11	P68	P100	358 (3)
I/O	P47	M11	P69	P101	361 (3)
I/O, SGCK3(1), GCK4(2)	P48	L11	P70	P102	364 (3)
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100(5)	TQ144	PQ208	PQ240	BG256(5)	CS280(2,5)	Bndry Scan
I/O	-	-	-	P190	B16	A15	23
I/O	-	P117	P166	P191	A16	E14	26
I/O	-	-	P167	P192	C15	C14	29
I/O	-	-	P168	P193	B15	B14	32
I/O	-	-	P169	P194	A15	D14	35
GND	-	P118	P170	P196	GND(4)	GND(4)	-
I/O	-	P119	P171	P197	B14	A14	38
I/O	-	P120	P172	P198	A14	C13	41
I/O	-	-	-	P199	C13	B13	44
I/O	-	-	-	P200	B13	A13	47
VCC	-	-	P173	P201	VCC(4)	D13	-
I/O	P82	P121	P174	P202	C12	B12	50
I/O	P83	P122	P175	P203	B12	D12	53
I/O	-	-	P176	P205	A12	A11	56
I/O	-	-	P177	P206	B11	B11	59
I/O	P84	P123	P178	P207	C11	C11	62
I/O	P85	P124	P179	P208	A11	D11	65
I/O	P86	P125	P180	P209	A10	A10	68
I/O	P87	P126	P181	P210	B10	B10	71
GND	P88	P127	P182	P211	GND(4)	GND(4)	-

2/8/00

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND(4) or V_{CC}(4) are internally bonded to Ground or V_{CC} planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01

Additional XCS30/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

2/12/98

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

6/4/97

CS280

VCC Pins					
A1	A7	C10	C17	D13	G1
G1	G19	K2	K17	M4	N16
T7	U3	U10	U17	W13	-
GND Pins					

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	P90	P105	Y16	W14	466 (3)
GND	P91	P106	GND(4)	GND(4)	-
I/O	-	P107	V15	V14	469 (3)
I/O	P92	P108	W16	U14	472 (3)
I/O	P93	P109	Y17	T14	475 (3)
I/O	P94	P110	V16	R14	478 (3)
I/O	P95	P111	W17	W15	481 (3)
I/O	P96	P112	Y18	U15	484 (3)
I/O	-	-	-	T15	487 (3)
I/O	-	-	-	W16	490 (3)
I/O	P97	P113	U16	V16	493 (3)
I/O	P98	P114	V17	U16	496 (3)
I/O	P99	P115	W18	W17	499 (3)
I/O	P100	P116	Y19	W18	502 (3)
I/O	P101	P117	V18	V17	505 (3)
I/O, SGCK3(1), GCK4(2)	P102	P118	W19	V18	508 (3)
GND	P103	P119	GND(4)	GND(4)	-
DONE	P104	P120	Y20	W19	-
VCC	P105	P121	VCC(4)	VCC(4)	-
$\overline{\text{PROGRAM}}$	P106	P122	V19	U18	-
I/O (D7(2))	P107	P123	U19	V19	511 (3)
I/O, PGCK3(1), GCK5(2)	P108	P124	U18	U19	514 (3)
I/O	P109	P125	T17	T16	517 (3)
I/O	P110	P126	V20	T17	520 (3)
I/O	-	P127	U20	T18	523 (3)
I/O	P111	P128	T18	T19	526 (3)
I/O	-	-	-	R15	529 (3)
I/O	-	-	-	R17	523 (3)
I/O (D6(2))	P112	P129	T19	R16	535 (3)
I/O	P113	P130	T20	R19	538 (3)
I/O	P114	P131	R18	P15	541 (3)
I/O	P115	P132	R19	P17	544 (3)
I/O	P116	P133	R20	P18	547 (3)
I/O	P117	P134	P18	P16	550 (3)
GND	P118	P135	GND(4)	GND(4)	-
I/O	-	P136	P20	P19	553 (3)
I/O	-	P137	N18	N17	556 (3)
I/O	P119	P138	N19	N18	559 (3)
I/O	P120	P139	N20	N19	562 (3)
VCC	P121	P140	VCC(4)	VCC(4)	-
I/O (D5(2))	P122	P141	M17	M19	565 (3)
I/O	P123	P142	M18	M17	568 (3)

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	-	-	-	M18	571 (3)
I/O	-	-	M19	M16	574 (3)
I/O	P124	P144	M20	L19	577 (3)
I/O	P125	P145	L19	L18	580 (3)
I/O	P126	P146	L18	L17	583 (3)
I/O	P127	P147	L20	L16	586 (3)
I/O (D4(2))	P128	P148	K20	K19	589 (3)
I/O	P129	P149	K19	K18	592 (3)
VCC	P130	P150	VCC(4)	VCC(4)	-
GND	P131	P151	GND(4)	GND(4)	-
I/O (D3(2))	P132	P152	K18	K16	595 (3)
I/O	P133	P153	K17	K15	598 (3)
I/O	P134	P154	J20	J19	601 (3)
I/O	P135	P155	J19	J18	604 (3)
I/O	P136	P156	J18	J17	607 (3)
I/O	P137	P157	J17	J16	610 (3)
I/O	-	-	H20	H19	613 (3)
I/O	-	-	-	H18	616 (3)
I/O (D2(2))	P138	P159	H19	H17	619 (3)
I/O	P139	P160	H18	H16	622 (3)
VCC	P140	P161	VCC(4)	VCC(4)	-
I/O	P141	P162	G19	G18	625 (3)
I/O	P142	P163	F20	G17	628 (3)
I/O	-	P164	G18	G16	631 (3)
I/O	-	P165	F19	F19	634 (3)
GND	P143	P166	GND(4)	GND(4)	-
I/O	-	P167	F18	F18	637 (3)
I/O	P144	P168	E19	F17	640 (3)
I/O	P145	P169	D20	F16	643 (3)
I/O	P146	P170	E18	F15	646 (3)
I/O	P147	P171	D19	E19	649 (3)
I/O	P148	P172	C20	E17	652 (3)
I/O (D1(2))	P149	P173	E17	E16	655 (3)
I/O	P150	P174	D18	D19	658 (3)
I/O	-	-	-	D18	661 (3)
I/O	-	-	-	D17	664 (3)
I/O	P151	P175	C19	C19	667 (3)
I/O	P152	P176	B20	B19	670 (3)
I/O (D0(2), DIN)	P153	P177	C18	C18	673 (3)
I/O, SGCK4(1), GCK6(2) (DOUT)	P154	P178	B19	B18	676 (3)
CCLK	P155	P179	A20	A19	-
VCC	P156	P180	VCC(4)	VCC(4)	-

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
O, TDO	P157	P181	A19	B17	0
GND	P158	P182	GND(4)	GND(4)	-
I/O	P159	P183	B18	A18	2
I/O, PGCK4(1), GCK7(2)	P160	P184	B17	A17	5
I/O	P161	P185	C17	D16	8
I/O	P162	P186	D16	C16	11
I/O (CS1(2))	P163	P187	A18	B16	14
I/O	P164	P188	A17	A16	17
I/O	-	-	-	E15	20
I/O	-	-	-	C15	23
I/O	P165	P189	C16	D15	26
I/O	-	P190	B16	A15	29
I/O	P166	P191	A16	E14	32
I/O	P167	P192	C15	C14	35
I/O	P168	P193	B15	B14	38
I/O	P169	P194	A15	D14	41
GND	P170	P196	GND(4)	GND(4)	-
I/O	P171	P197	B14	A14	44
I/O	P172	P198	A14	C13	47
I/O	-	P199	C13	B13	50
I/O	-	P200	B13	A13	53
VCC	P173	P201	VCC(4)	VCC(4)	-
I/O	-	-	A13	A12	56
I/O	-	-	D12	C12	59
I/O	P174	P202	C12	B12	62
I/O	P175	P203	B12	D12	65
I/O	P176	P205	A12	A11	68
I/O	P177	P206	B11	B11	71
I/O	P178	P207	C11	C11	74
I/O	P179	P208	A11	D11	77
I/O	P180	P209	A10	A10	80
I/O	P181	P210	B10	B10	83
GND	P182	P211	GND(4)	GND(4)	-

2/8/00

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS40XL is not part of the Boundary Scan chain. For the XCS40XL, subtract 1 from all Boundary Scan numbers from GCK3 on (343 and higher).
4. Pads labeled GND(4) or V_{CC}(4) are internally bonded to Ground or V_{CC} planes within the package.
5. CS280 package discontinued by PDN2004-01

Additional XCS40/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

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CS280

VCC Pins					
A1	A7	B5	B15	C10	C17
D13	E3	E18	G1	G19	K2
K17	M4	N16	R3	R18	T7
U3	U10	U17	V5	V15	W13
GND Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-

5/19/99