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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	576
Number of Logic Elements/Cells	1368
Total RAM Bits	18432
Number of I/O	77
Number of Gates	30000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs30xl-4vq100c

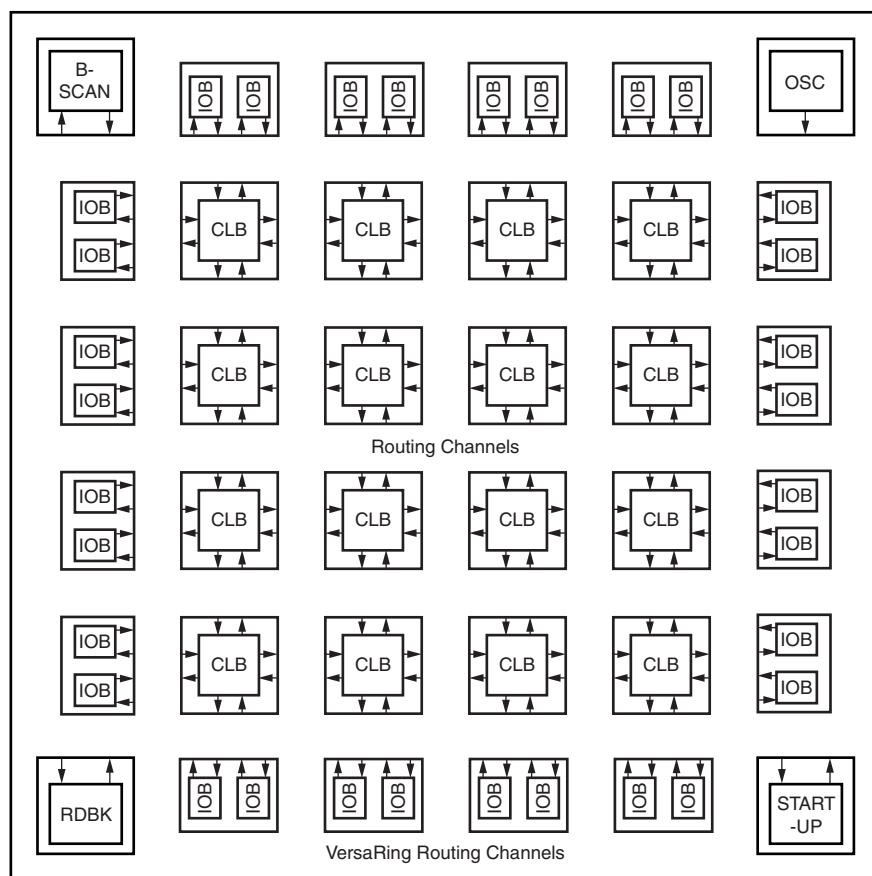
General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in **Figure 1**. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these

memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).


Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.




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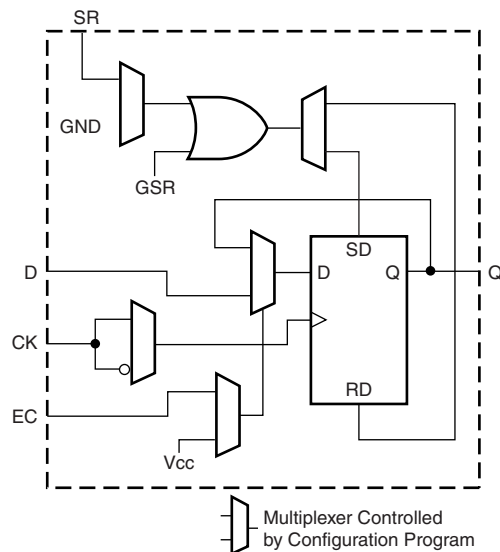
Figure 1: Basic FPGA Block Diagram

Table 2: CLB Storage Element Functionality

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
		1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (Spartan-XL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

- X Don't care
-  Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0* Input is Low or unconnected (default value)
- 1* Input is High or unconnected (default value)



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Figure 3: CLB Flip-Flop Functional Block Diagram

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

CLB Signal Flow Control

In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2, page 4) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinational CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinational output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1-C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

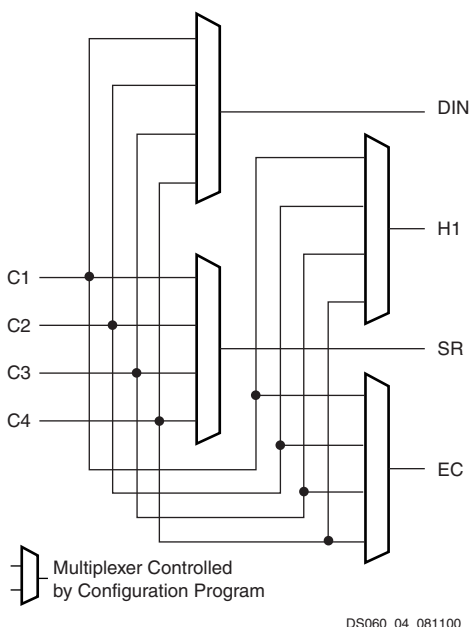


Figure 4: CLB Control Signal Interface

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

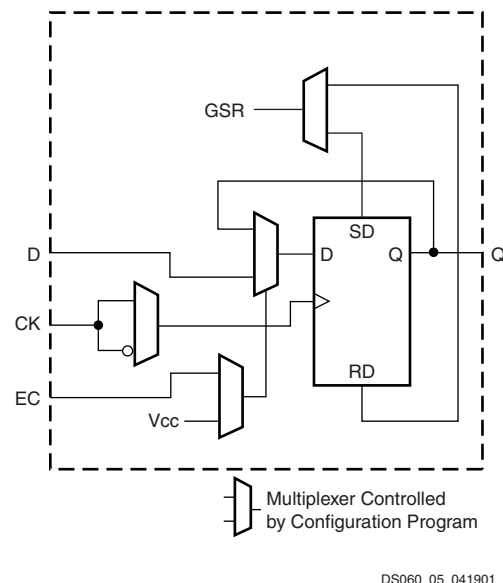


Figure 5: IOB Flip-Flop/Latch Functional Block Diagram

IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: Input Register Functionality

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop		1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

- X Don't care.
- Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0* Input is Low or unconnected (default value)
- 1* Input is High or unconnected (default value)

This high value makes them unsuitable as wired-AND pull-up resistors.

Table 7: Supported Destinations for Spartan/XL Outputs

Destination	Spartan-XL Outputs	Spartan Outputs	
	3.3V, CMOS	5V, TTL	5V, CMOS
Any device, $V_{CC} = 3.3V$, CMOS-threshold inputs	✓	✓	Some ⁽¹⁾
Any device, $V_{CC} = 5V$, TTL-threshold inputs	✓	✓	✓
Any device, $V_{CC} = 5V$, CMOS-threshold inputs	Unreliable Data		✓

Notes:

1. Only if destination device has 5V tolerant inputs.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULL-DOWN library component to the net attached to the pad.

Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops (Figure 5). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either

falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (see EC signal in Figure 5), which through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan/XL FPGA CLB. It cannot be inverted within the IOB.

Routing Channel Description

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

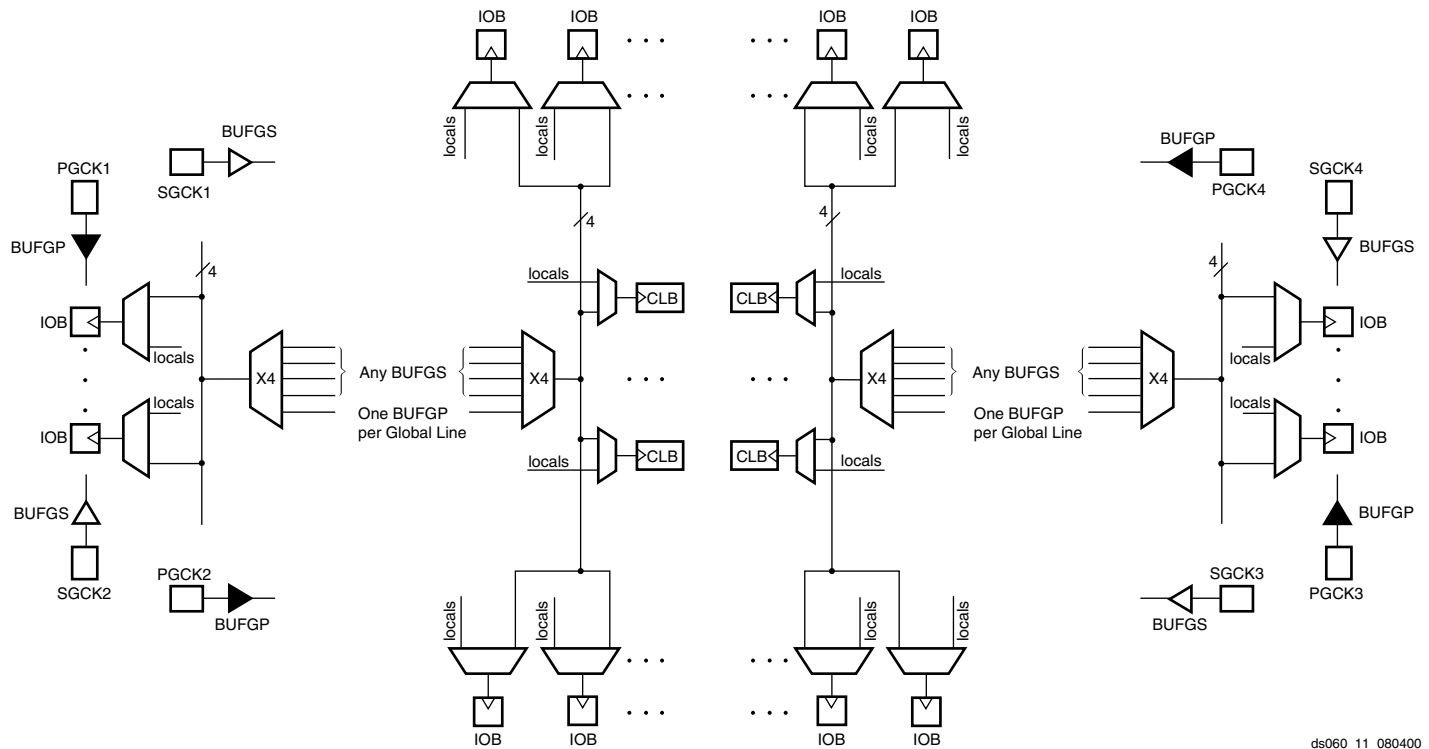
This section describes the routing channels available in Spartan/XL devices. Figure 8 shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the designer should open a design in the FPGA Editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

CLB Routing Channels

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). Figure 8 shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.



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Figure 11: 5V Spartan Family Global Net Distribution

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 8. Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 8: CLB Memory Configurations

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√	—	—

figuration are shown in Table 14 and Table 15.

Table 14: Pin Functions During Configuration (Spartan Family Only)

Configuration Mode (MODE Pin)		User Operation
Slave Serial (High)	Master Serial (Low)	
MODE (I)	MODE (I)	MODE
HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

Notes:

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Table 15: Pin Functions During Configuration (Spartan-XL Family Only)

CONFIGURATION MODE <M1:M0>			User Operation
Slave Serial [1:1]	Master Serial [1:0]	Express [0:X]	
M1 (High) (I)	M1 (High) (I)	M1(Low) (I)	M1
M0 (High) (I)	M0 (Low) (I)	M0 (I)	M0
HDC (High)	HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

Notes:

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to $+25\%$.

In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

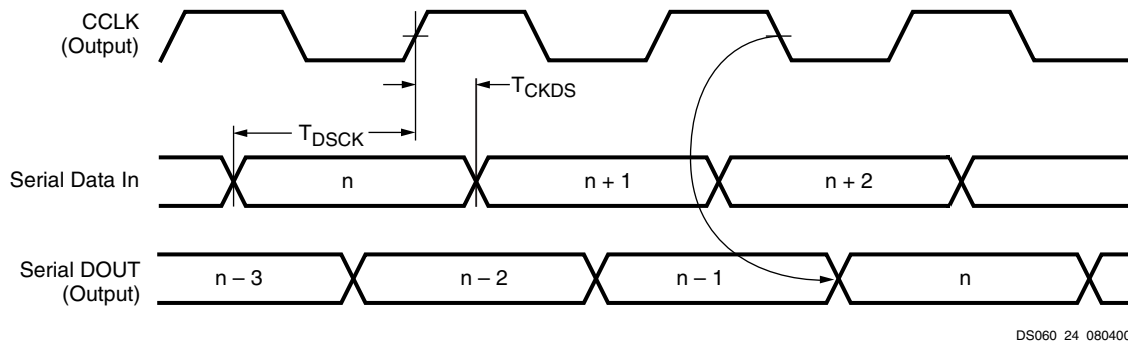
When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the

falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in Figure 24.

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Earlier families such as the XC3000 series do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

Figure 25 shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Symbol	Description	Min	Units
CCLK	T_{DSCK}	DIN setup	20	ns
	T_{CKDS}	DIN hold	0	ns

Notes:

1. At power-up, V_{CC} must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 24: Master Serial Mode Programming Switching Characteristics

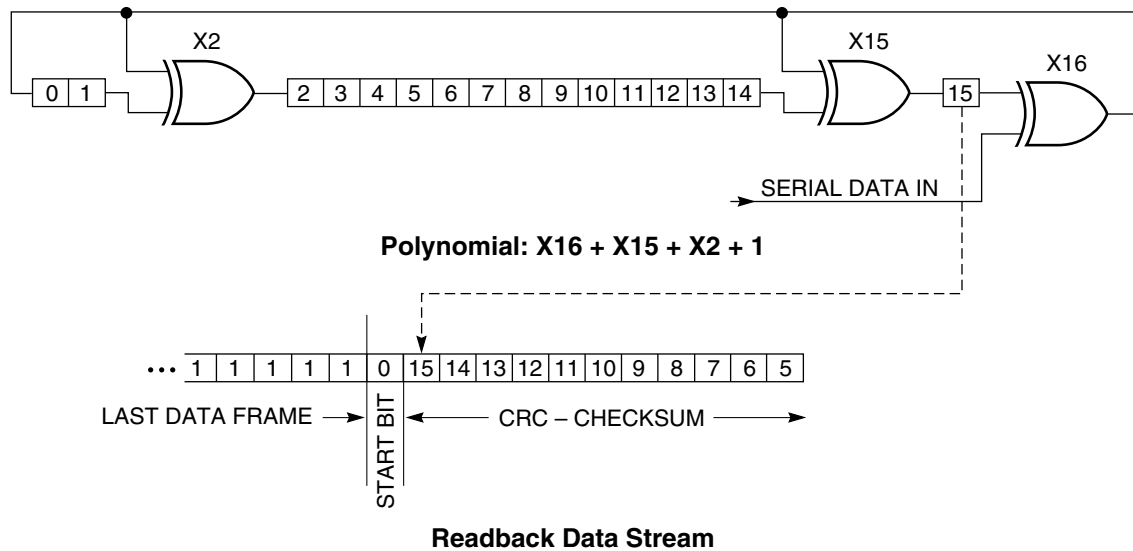
Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 25 shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.



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Figure 29: Circuit for Generating CRC-16

Configuration Sequence

There are four major steps in the Spartan/XL FPGA power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC} . When all \overline{INIT} pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin

Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

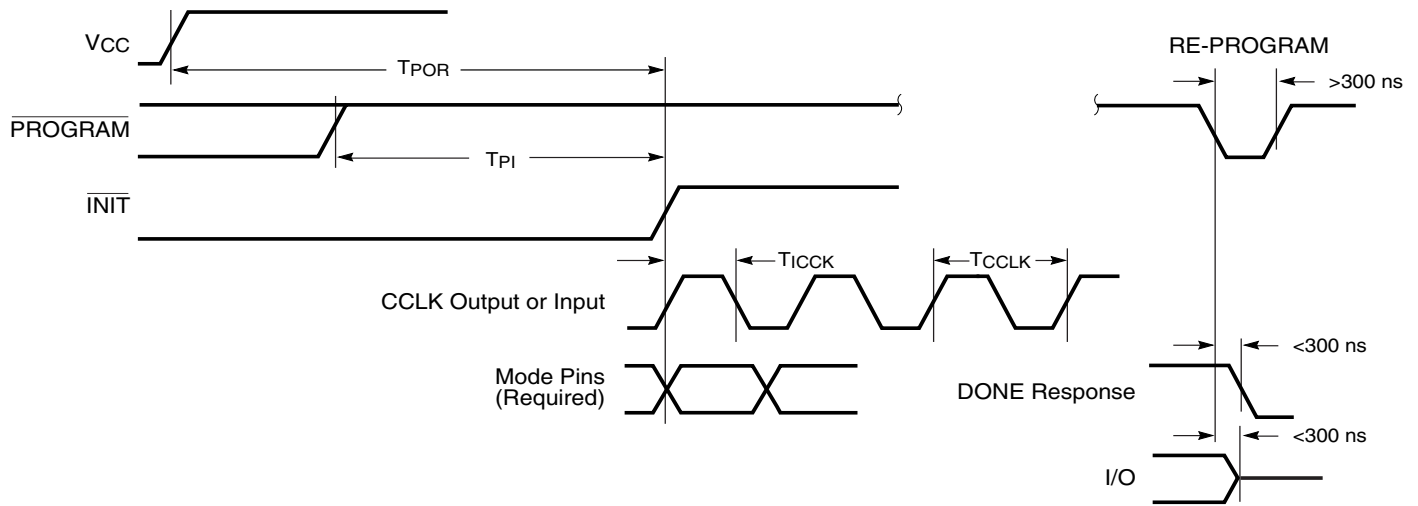
At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the \overline{INIT} input.

Initialization

During initialization and configuration, user pins \overline{HDC} , \overline{LDC} , \overline{INIT} and \overline{DONE} provide status outputs for the system interface. The outputs \overline{LDC} , \overline{INIT} and \overline{DONE} are held Low and \overline{HDC} is held High starting at the initial application of power.

The open drain \overline{INIT} pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive \overline{INIT} . Two internal clocks after the \overline{INIT} pin is recognized as High, the device samples the \overline{MODE} pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Configuration Switching Characteristics



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Master Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	40	130	ms
T_{PI}	Program Latency	30	200	μ s per CLB column
T_{ICCK}	CCLK (output) delay	40	250	μ s
T_{CCLK}	CCLK (output) period, slow	640	2000	ns
T_{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	10	33	ms
T_{PI}	Program latency	30	200	μ s per CLB column
T_{ICCK}	CCLK (input) delay (required)	4	-	μ s
T_{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-4		-3		
		Min	Max	Min	Max	
Clocks						
T _{CH}	Clock High time	3.0	-	4.0	-	ns
T _{CL}	Clock Low time	3.0	-	4.0	-	ns
Combinatorial Delays						
T _{ILO}	F/G inputs to X/Y outputs	-	1.2	-	1.6	ns
T _{IHO}	F/G inputs via H to X/Y outputs	-	2.0	-	2.7	ns
T _{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.7	-	2.2	ns
CLB Fast Carry Logic						
T _{OPCY}	Operand inputs (F1, F2, G1, G4) to C _{OUT}	-	1.7	-	2.1	ns
T _{ASCY}	Add/Subtract input (F3) to C _{OUT}	-	2.8	-	3.7	ns
T _{INCY}	Initialization inputs (F1, F3) to C _{OUT}	-	1.2	-	1.4	ns
T _{SUM}	C _{IN} through function generators to X/Y outputs	-	2.0	-	2.6	ns
T _{BYP}	C _{IN} to C _{OUT} , bypass function generators	-	0.5	-	0.6	ns
Sequential Delays						
T _{CKO}	Clock K to Flip-Flop outputs Q	-	2.1	-	2.8	ns
Setup Time before Clock K						
T _{ICK}	F/G inputs	1.8	-	2.4	-	ns
T _{IHCK}	F/G inputs via H	2.9	-	3.9	-	ns
T _{HH1CK}	C inputs via H1 through H	2.3	-	3.3	-	ns
T _{DICK}	C inputs via DIN	1.3	-	2.0	-	ns
T _{ECCK}	C inputs via EC	2.0	-	2.6	-	ns
T _{RCK}	C inputs via S/R, going Low (inactive)	2.5	-	4.0	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T _{RPW}	Width (High)	3.0	-	4.0	-	ns
T _{RIO}	Delay from C inputs via S/R, going High to Q	-	3.0	-	4.0	ns
Global Set/Reset						
T _{MRW}	Minimum GSR pulse width	11.5	-	13.5	-	ns
T _{MRQ}	Delay from GSR input to any Q	See page 50 for T _{RRI} values per device.				
F _{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	166	-	125	MHz

Spartan Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more pre-

cise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Spartan Family Output Flip-Flop, Clock-to-Out

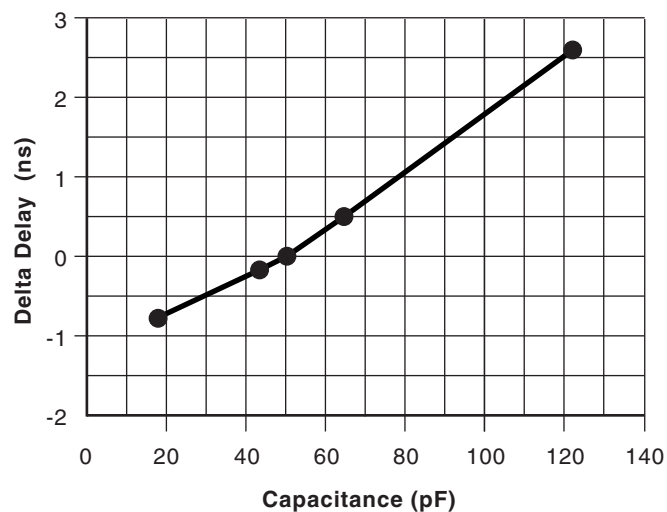
Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
Global Primary Clock to TTL Output using OFF					
T _{ICKOF}	Fast	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
T _{ICKO}	Slew-rate limited	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
T _{ICKSOF}	Fast	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
T _{ICKSO}	Slew-rate limited	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
T _{CMOSOF}	Fast	All devices	0.8	1.0	ns
T _{CMOSO}	Slew-rate limited	All devices	1.5	2.0	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see [Figure 34](#).
3. OFF = Output Flip-Flop

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



DS060_35_080400

Figure 34: Delay Factor at Various Capacitive Loads

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings⁽¹⁾

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked ^(2, 3)	–0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	–0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked ^(2, 3)	–0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	–0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0V or overshoot to $V_{CC} + 2.0V$, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ ⁽¹⁾	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage ⁽²⁾		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage ⁽²⁾		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:

- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement threshold is ~50% of V_{CC} .

Spartan-XL Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clocks						
T _{CH}	Clock High time	2.0	-	2.3	-	ns
T _{CL}	Clock Low time	2.0	-	2.3	-	ns
Combinatorial Delays						
T _{ILO}	F/G inputs to X/Y outputs	-	1.0	-	1.1	ns
T _{IHO}	F/G inputs via H to X/Y outputs	-	1.7	-	2.0	ns
T _{ITO}	F/G inputs via transparent latch to Q outputs	-	1.5	-	1.8	ns
T _{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.5	-	1.8	ns
Sequential Delays						
T _{CKO}	Clock K to Flip-Flop or latch outputs Q	-	1.2	-	1.4	ns
Setup Time before Clock K						
T _{ICK}	F/G inputs	0.6	-	0.7	-	ns
T _{IHCK}	F/G inputs via H	1.3	-	1.6	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T _{RPW}	Width (High)	2.5	-	2.8	-	ns
T _{RIO}	Delay from C inputs via S/R, going High to Q	-	2.3	-	2.7	ns
Global Set/Reset						
T _{MRW}	Minimum GSR Pulse Width	10.5	-	11.5	-	ns
T _{MRQ}	Delay from GSR input to any Q	See page 60 for T _{RRI} values per device.				
F _{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	250	-	217	MHz

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size ⁽¹⁾	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Write Operation							
T _{WCS}	Address write cycle time (clock K period)	16x2	7.7	-	8.4	-	ns
T _{WCTS}		32x1	7.7	-	8.4	-	ns
T _{WPS}	Clock K pulse width (active edge)	16x2	3.1	-	3.6	-	ns
T _{WPTS}		32x1	3.1	-	3.6	-	ns
T _{ASS}	Address setup time before clock K	16x2	1.3	-	1.5	-	ns
T _{ASTS}		32x1	1.5	-	1.7	-	ns
T _{DSS}	DIN setup time before clock K	16x2	1.5	-	1.7	-	ns
T _{DSTS}		32x1	1.8	-	2.1	-	ns
T _{WSS}	WE setup time before clock K	16x2	1.4	-	1.6	-	ns
T _{WSTS}		32x1	1.3	-	1.5	-	ns
	All hold times after clock K	16x2	0.0	-	0.0	-	ns
T _{WOS}	Data valid after clock K	32x1	-	4.5	-	5.3	ns
T _{WOTS}		16x2	-	5.4	-	6.3	ns
Read Operation							
T _{RC}	Address read cycle time	16x2	2.6	-	3.1	-	ns
T _{RCT}		32x1	3.8	-	5.5	-	ns
T _{ILO}	Data Valid after address change (no Write Enable)	16x2	-	1.0	-	1.1	ns
T _{IHO}		32x1	-	1.7	-	2.0	ns
T _{ICK}	Address setup time before clock K	16x2	0.6	-	0.7	-	ns
T _{IHCK}		32x1	1.3	-	1.6	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Setup and Hold

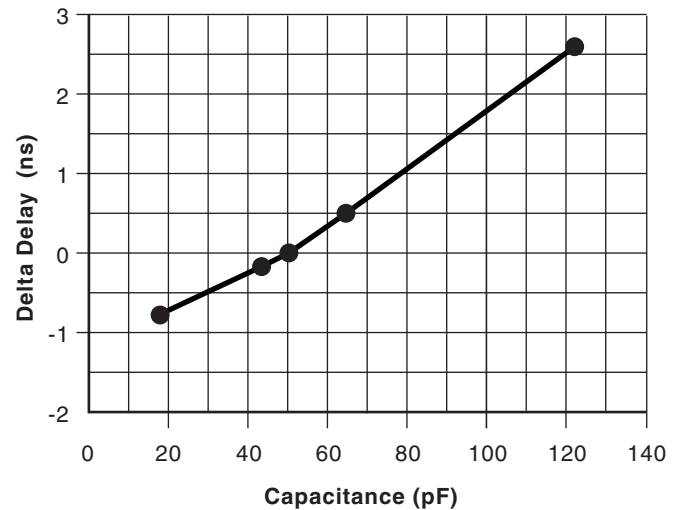
Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Input Setup/Hold Times Using Global Clock and IFF					
T_{SUF}/T_{HF}	No Delay	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
T_{SU}/T_H	Full Delay	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



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Figure 35: Delay Factor at Various Capacitive Loads

Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol		Device	Speed Grade				Units
			-5		-4		
	Description		Min	Max	Min	Max	
Setup Times							
T _{ECIK}	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T _{PICK}	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T _{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T _{PID}	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T _{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T _{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T _{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T _{Delay}	T _{PICKD} = T _{PICK} + T _{Delay} T _{PDLI} = T _{PLI} + T _{Delay}	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T _{RRI}	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

Notes:

- Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
- Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to

the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Propagation Delays							
T _{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.2	-	3.7	ns
T _{OPF}	Output (O) to Pad, fast	All devices	-	2.5	-	2.9	ns
T _{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	2.8	-	3.3	ns
T _{TSONF}	3-state to Pad active and valid, fast	All devices	-	2.6	-	3.0	ns
T _{OFFPF}	Output (O) to Pad via Output MUX, fast	All devices	-	3.7	-	4.4	ns
T _{OKFPF}	Select (OK) to Pad via Output MUX, fast	All devices	-	3.3	-	3.9	ns
T _{SLOW}	For Output SLOW option add	All devices	-	1.5	-	1.7	ns
Setup and Hold Times							
T _{OOK}	Output (O) to clock (OK) setup time	All devices	0.5	-	0.5	-	ns
T _{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T _{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	0.0	-	0.0	-	ns
T _{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.1	-	0.2	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T _{RPO}	Delay from GSR input to any Pad	XCS05XL	-	11.9	-	14.0	ns
		XCS10XL	-	12.4	-	14.5	ns
		XCS20XL	-	12.9	-	15.0	ns
		XCS30XL	-	13.9	-	16.0	ns
		XCS40XL	-	14.9	-	17.0	ns

Notes:

- Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
- Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	P124	P144	M20	L19	493 ⁽³⁾
I/O	-	-	P125	P145	L19	L18	496 ⁽³⁾
I/O	P59	P86	P126	P146	L18	L17	499 ⁽³⁾
I/O	P60	P87	P127	P147	L20	L16	502 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	P88	P128	P148	K20	K19	505 ⁽³⁾
I/O	P62	P89	P129	P149	K19	K18	508 ⁽³⁾
VCC	P63	P90	P130	P150	VCC ⁽⁴⁾	K17	-
GND	P64	P91	P131	P151	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O (D3 ⁽²⁾)	P65	P92	P132	P152	K18	K16	511 ⁽³⁾
I/O	P66	P93	P133	P153	K17	K15	514 ⁽³⁾
I/O	P67	P94	P134	P154	J20	J19	517 ⁽³⁾
I/O	-	P95	P135	P155	J19	J18	520 ⁽³⁾
I/O	-	-	P136	P156	J18	J17	523 ⁽³⁾
I/O	-	-	P137	P157	J17	J16	526 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	P96	P138	P159	H19	H17	529 ⁽³⁾
I/O	P69	P97	P139	P160	H18	H16	532 ⁽³⁾
VCC	-	-	P140	P161	VCC ⁽⁴⁾	G19	-
I/O	-	P98	P141	P162	G19	G18	535 ⁽³⁾
I/O	-	P99	P142	P163	F20	G17	538 ⁽³⁾
I/O	-	-	-	P164	G18	G16	541 ⁽³⁾
I/O	-	-	-	P165	F19	F19	544 ⁽³⁾
GND	-	P100	P143	P166	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P167	F18	F18	547 ⁽³⁾
I/O	-	-	P144	P168	E19	F17	550 ⁽³⁾
I/O	-	-	P145	P169	D20	F16	553 ⁽³⁾
I/O	-	-	P146	P170	E18	F15	556 ⁽³⁾
I/O	-	-	P147	P171	D19	E19	559 ⁽³⁾
I/O	-	-	P148	P172	C20	E17	562 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	P101	P149	P173	E17	E16	565 ⁽³⁾
I/O	P71	P102	P150	P174	D18	D19	568 ⁽³⁾
I/O	-	P103	P151	P175	C19	C19	571 ⁽³⁾
I/O	-	P104	P152	P176	B20	B19	574 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	P105	P153	P177	C18	C18	577 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	P106	P154	P178	B19	B18	580 ⁽³⁾
CCLK	P74	P107	P155	P179	A20	A19	-
VCC	P75	P108	P156	P180	VCC ⁽⁴⁾	C17	-
O, TDO	P76	P109	P157	P181	A19	B17	0
GND	P77	P110	P158	P182	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P78	P111	P159	P183	B18	A18	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	P112	P160	P184	B17	A17	5
I/O	-	P113	P161	P185	C17	D16	8
I/O	-	P114	P162	P186	D16	C16	11
I/O (CS1) ⁽²⁾	P80	P115	P163	P187	A18	B16	14
I/O	P81	P116	P164	P188	A17	A16	17
I/O	-	-	P165	P189	C16	D15	20

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
O, TDO	P157	P181	A19	B17	0
GND	P158	P182	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P159	P183	B18	A18	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P160	P184	B17	A17	5
I/O	P161	P185	C17	D16	8
I/O	P162	P186	D16	C16	11
I/O (CS1 ⁽²⁾)	P163	P187	A18	B16	14
I/O	P164	P188	A17	A16	17
I/O	-	-	-	E15	20
I/O	-	-	-	C15	23
I/O	P165	P189	C16	D15	26
I/O	-	P190	B16	A15	29
I/O	P166	P191	A16	E14	32
I/O	P167	P192	C15	C14	35
I/O	P168	P193	B15	B14	38
I/O	P169	P194	A15	D14	41
GND	P170	P196	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P171	P197	B14	A14	44
I/O	P172	P198	A14	C13	47
I/O	-	P199	C13	B13	50
I/O	-	P200	B13	A13	53
VCC	P173	P201	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	-	A13	A12	56
I/O	-	-	D12	C12	59
I/O	P174	P202	C12	B12	62
I/O	P175	P203	B12	D12	65
I/O	P176	P205	A12	A11	68
I/O	P177	P206	B11	B11	71
I/O	P178	P207	C11	C11	74
I/O	P179	P208	A11	D11	77
I/O	P180	P209	A10	A10	80
I/O	P181	P210	B10	B10	83
GND	P182	P211	GND ⁽⁴⁾	GND ⁽⁴⁾	-

2/8/00

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS40XL is not part of the Boundary Scan chain. For the XCS40XL, subtract 1 from all Boundary Scan numbers from GCK3 on (343 and higher).
4. Pads labeled GND⁽⁴⁾ or VCC⁽⁴⁾ are internally bonded to Ground or VCC planes within the package.
5. CS280 package discontinued by [PDN2004-01](#)

Additional XCS40/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

6/17/97

CS280

VCC Pins					
A1	A7	B5	B15	C10	C17
D13	E3	E18	G1	G19	K2
K17	M4	N16	R3	R18	T7
U3	U10	U17	V5	V15	W13
GND Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-

5/19/99