



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.


Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.


Details

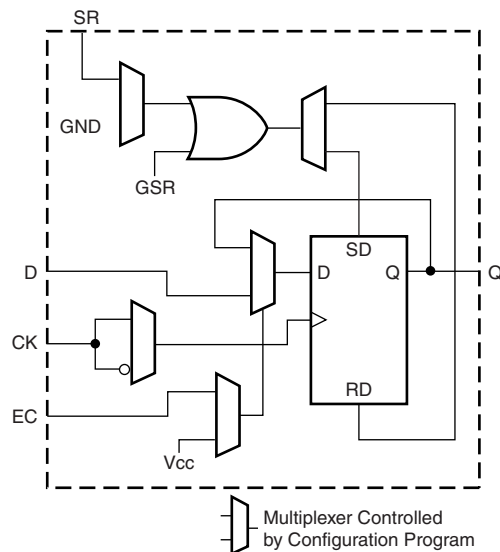
Product Status	Obsolete
Number of LABs/CLBs	576
Number of Logic Elements/Cells	1368
Total RAM Bits	18432
Number of I/O	77
Number of Gates	30000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs30xl-4vq100i

Table 2: CLB Storage Element Functionality

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
		1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (Spartan-XL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

- X Don't care
-  Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0* Input is Low or unconnected (default value)
- 1* Input is High or unconnected (default value)



DS060_03_041901

Figure 3: CLB Flip-Flop Functional Block Diagram

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

CLB Signal Flow Control

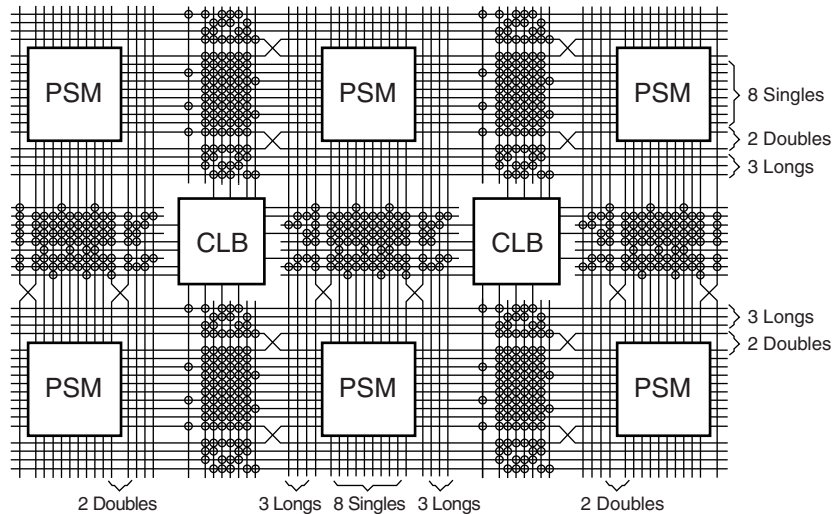
In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2, page 4) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinational CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinational output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1-C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

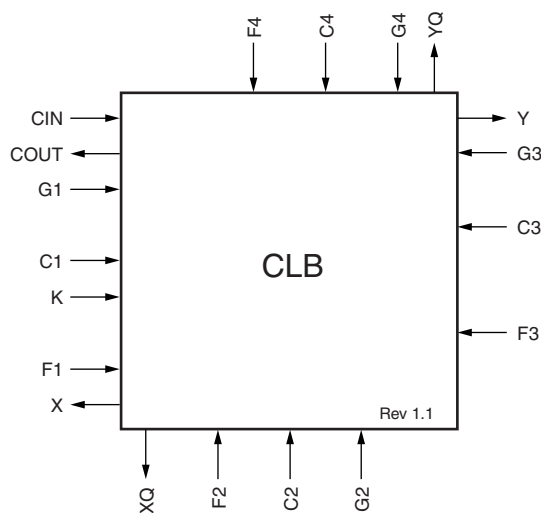


DS060_09_041901

Figure 8: Spartan/XL CLB Routing Channels and Interface Block Diagram

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.



DS060_08_081100

Figure 9: CLB Interconnect Signals

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs. Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

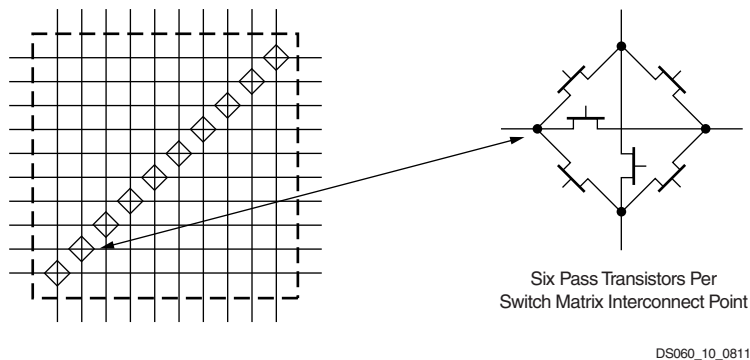


Figure 10: Programmable Switch Matrix

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see [Figure 8](#)).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in [Figure 8](#). The longlines also interface to some 3-state buffers which is described later in [3-State Long Line Drivers](#), page 19.

I/O Routing

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in [Figure 11](#). In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.

- The 16 x 1 single-port configuration contains a RAM array with 16 locations, each one-bit wide. One 4-bit address decoder determines the RAM location for write and read operations. There is one input for writing data and one output for reading data, all at the selected address.
- The (16 x 1) x 2 single-port configuration combines two 16 x 1 single-port configurations (each according to the preceding description). There is one data input, one data output and one address decoder for each array. These arrays can be addressed independently.
- The 32 x 1 single-port configuration contains a RAM array with 32 locations, each one-bit wide. There is one data input, one data output, and one 5-bit address decoder.
- The dual-port mode 16 x 1 configuration contains a RAM array with 16 locations, each one-bit wide. There are two 4-bit address decoders, one for each port. One port consists of an input for writing and an output for reading, all at a selected address. The other port consists of one output for reading from an independently selected address.

The appropriate choice of RAM configuration mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Selection criteria include the following: Whereas the 32 x 1 single-port, the (16 x 1) x 2 single-port, and the 16 x 1 dual-port configurations each use one entire CLB, the 16 x 1 single-port configuration uses only one half of a CLB. Due to its simultaneous read/write capability, the dual-port RAM can transfer twice as much data as the single-port RAM, which permits only one data operation at any given time.

CLB memory configuration options are selected by using the appropriate library symbol in the design entry.

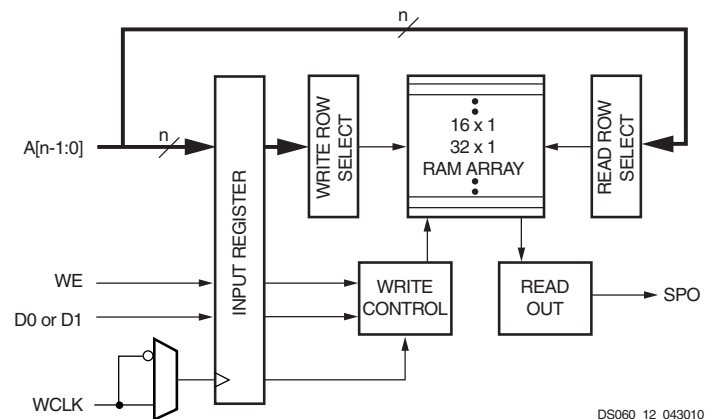
Single-Port Mode

There are three CLB memory configurations for the single-port RAM: 16 x 1, (16 x 1) x 2, and 32 x 1, the functional organization of which is shown in Figure 12.

The single-port RAM signals and the CLB signals (Figure 2, page 4) from which they are originally derived are shown in Table 9.

Table 9: Single-Port RAM Signals

RAM Signal	Function	CLB Signal
D0 or D1	Data In	DIN or H1
A[3:0]	Address	F[4:1] or G[4:1]
A4 (32 x 1 only)	Address	H1
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (Data Out)	F _{OUT} or G _{OUT}



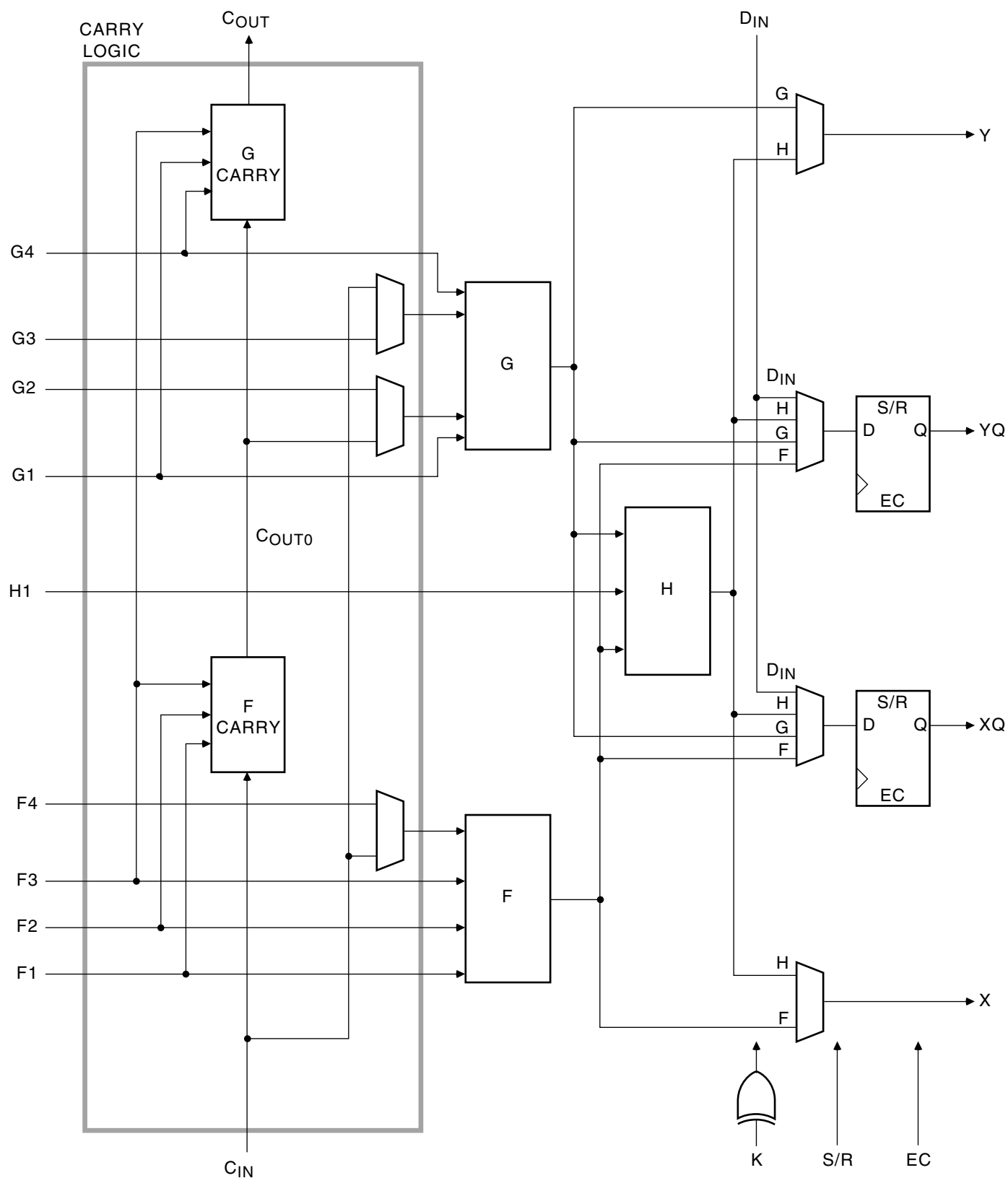
Notes:

1. The (16 x 1) x 2 configuration combines two 16 x 1 single-port RAMs, each with its own independent address bus and data input. The same WE and WCLK signals are connected to both RAMs.
2. n = 4 for the 16 x 1 and (16 x 1) x 2 configurations. n = 5 for the 32 x 1 configuration.

Figure 12: Logic Diagram for the Single-Port RAM

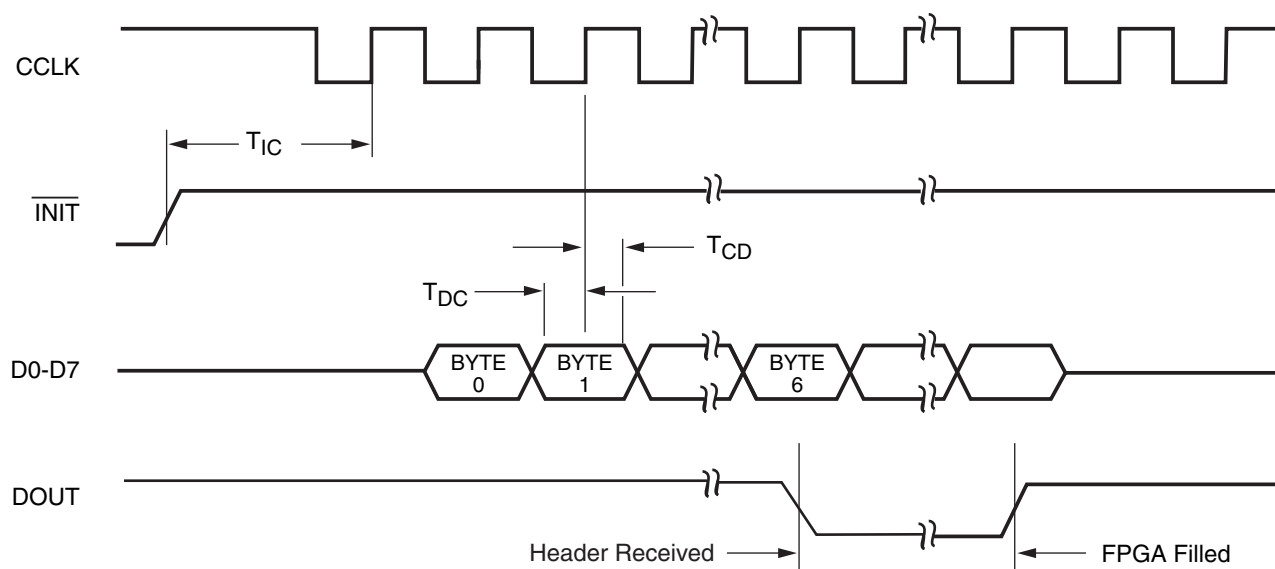
Writing data to the single-port RAM is essentially the same as writing to a data register. It is an edge-triggered (synchronous) operation performed by applying an address to the A inputs and data to the D input during the active edge of WCLK while WE is High.

The timing relationships are shown in Figure 13. The High logic level on WE enables the input data register for writing. The active edge of WCLK latches the address, input data, and WE signals. Then, an internal write pulse is generated that loads the data into the memory cell.



DS060_16_080400

Figure 16: Fast Carry Logic in Spartan/XL CLB



DS060_28_080400

Symbol		Description	Min	Max	Units
T_{IC}	CCLK	\overline{INIT} (High) setup time	5	-	μs
T_{DC}		D0-D7 setup time	20	-	ns
T_{CD}		D0-D7 hold time	0	-	ns
T_{CCH}		CCLK High time	45	-	ns
T_{CCL}		CCLK Low time	45	-	ns
F_{CC}		CCLK Frequency	-	10	MHz

Notes:

1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: Express Mode Programming Switching Characteristics

Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right.

Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

Table 16: Spartan/XL Data Stream Formats

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0] ⁽¹⁾
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	11111110b ⁽²⁾
Data Frame	DATA[n-1:0]	DATA[n-1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes ⁽³⁾	FFh	FFFFFFFFFFFFFFh

Legend:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Notes:

1. Not used by configuration logic.
2. 11111111b for XCS40XL only.
3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the $\overline{\text{INIT}}$ pin. In Master serial mode, CCLK continues to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the PROGRAM pin Low or cycling VCC.

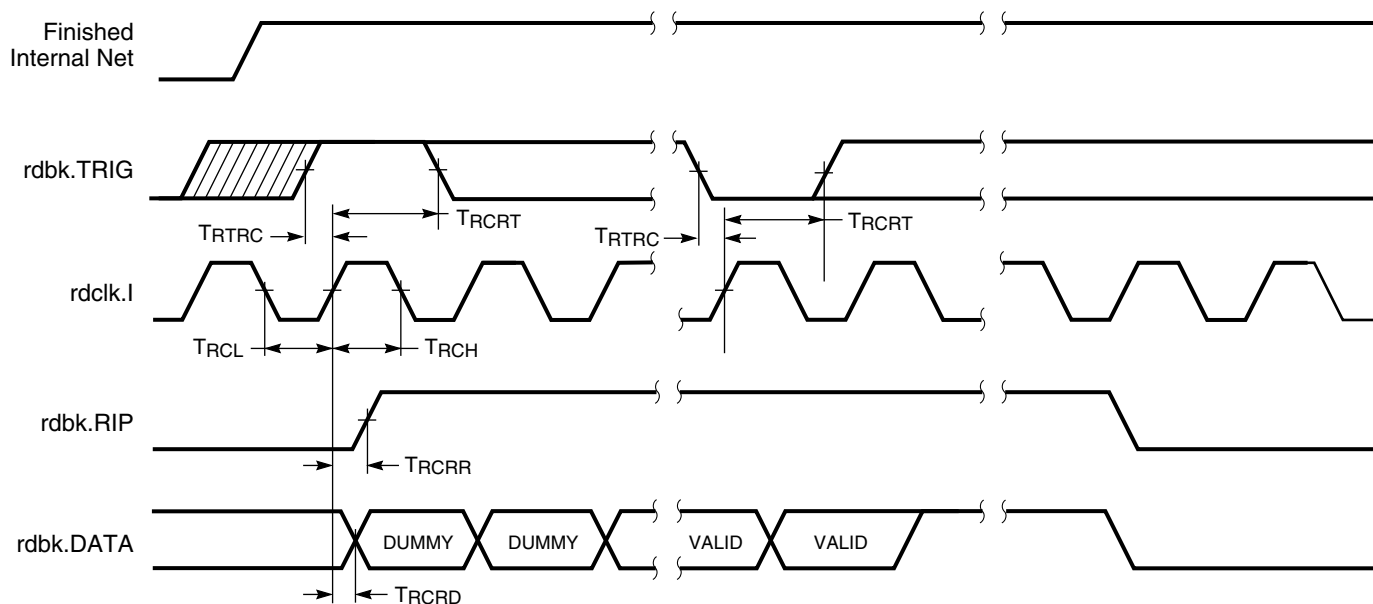
Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.



DS060_32_080400

Figure 33: Spartan and Spartan-XL Readback Timing Diagram

Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:

1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size ⁽¹⁾	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Write Operation							
T _{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T _{WCTS}		32x1	8.0	-	11.6	-	ns
T _{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T _{WPTS}		32x1	4.0	-	5.8	-	ns
T _{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T _{ASTS}		32x1	1.5	-	2.0	-	ns
T _{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{AHTS}		32x1	0.0	-	0.0	-	ns
T _{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T _{DSTS}		32x1	1.5	-	1.7	-	ns
T _{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{DHTS}		32x1	0.0	-	0.0	-	ns
T _{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T _{WSTS}		32x1	1.5	-	1.6	-	ns
T _{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{WHTS}		32x1	0.0	-	0.0	-	ns
T _{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T _{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T _{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T _{RCT}		32x1	3.8	-	3.8	-	ns
T _{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T _{IHO}		32x1	-	2.0	-	2.7	ns
T _{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T _{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Min	Min	
Input Setup/Hold Times Using Primary Clock and IFF					
T _{PSUF} /T _{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T _{PSU} /T _{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T _{SSUF} /T _{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T _{SSU} /T _{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:

1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Setup Times - TTL Inputs ⁽¹⁾							
T _{ECIK}	Clock Enable (EC) to Clock (IK), no delay	All devices	1.6	-	2.1	-	ns
T _{PICK}	Pad to Clock (IK), no delay	All devices	1.5	-	2.0	-	ns
Hold Times							
T _{IKEC}	Clock Enable (EC) to Clock (IK), no delay	All devices	0.0	-	0.9	-	ns
	All Other Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays - TTL Inputs ⁽¹⁾							
T _{PID}	Pad to I1, I2	All devices	-	1.5	-	2.0	ns
T _{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.8	-	3.6	ns
T _{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	2.7	-	2.8	ns
T _{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	3.2	-	3.9	ns
Delay Adder for Input with Delay Option							
T _{Delay}	T _{ECIKD} = T _{ECIK} + T _{Delay} T _{PICKD} = T _{PICK} + T _{Delay} T _{PDLI} = T _{PLI} + T _{Delay}	XCS05	3.6	-	4.0	-	ns
		XCS10	3.7	-	4.1	-	ns
		XCS20	3.8	-	4.2	-	ns
		XCS30	4.5	-	5.0	-	ns
		XCS40	5.5	-	5.5	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	11.5	-	13.5	-	ns
T _{RRI}	Delay from GSR input to any Q	XCS05	-	9.0	-	11.3	ns
		XCS10	-	9.5	-	11.9	ns
		XCS20	-	10.0	-	12.5	ns
		XCS30	-	10.5	-	13.1	ns
		XCS40	-	11.0	-	13.8	ns

Notes:

1. Delay adder for CMOS Inputs option: for -3 speed grade, add 0.4 ns; for -4 speed grade, add 0.2 ns.
2. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
3. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Typ.	Max	Units
V _{OH}	High-level output voltage @ I _{OH} = −4.0 mA, V _{CC} min (LVTTL)		2.4	-	-	V
	High-level output voltage @ I _{OH} = −500 μA, (LVCMOS)		90% V _{CC}	-	-	V
V _{OL}	Low-level output voltage @ I _{OL} = 12.0 mA, V _{CC} min (LVTTL) ⁽¹⁾		-	-	0.4	V
	Low-level output voltage @ I _{OL} = 24.0 mA, V _{CC} min (LVTTL) ⁽²⁾		-	-	0.4	V
	Low-level output voltage @ I _{OL} = 1500 μA, (LVCMOS)		-	-	10% V _{CC}	V
V _{DR}	Data retention supply voltage (below which configuration data may be lost)		2.5	-	-	V
I _{CCO}	Quiescent FPGA supply current ^(3,4)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I _{CCPD}	Power Down FPGA supply current ^(3,5)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I _L	Input or output leakage current		−10	-	10	μA
C _{IN}	Input capacitance (sample tested)		-	-	10	pF
I _{RPU}	Pad pull-up (when selected) @ V _{IN} = 0V (sample tested)		0.02	-	0.25	mA
I _{RPD}	Pad pull-down (when selected) @ V _{IN} = 3.3V (sample tested)		0.02	-	-	mA

Notes:

1. With up to 64 pins simultaneously sinking 12 mA (default mode).
2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
4. With no output current loads, no active input resistors, and all package pins at V_{CC} or GND.
5. With \overline{PWRDWN} active.

Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CC} lines for a successful power on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Max	Units
I_{CCPO}	Total V_{CC} supply current required during power-on	100	-	mA
T_{CCPO}	V_{CC} ramp time ^(2,3)	-	50	ms

Notes:

1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CC} ramps from 0 to 3.3V.
2. The ramp time is measured from GND to V_{CC} max on a fully loaded board.
3. V_{CC} must not dip in the negative direction during power on.

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

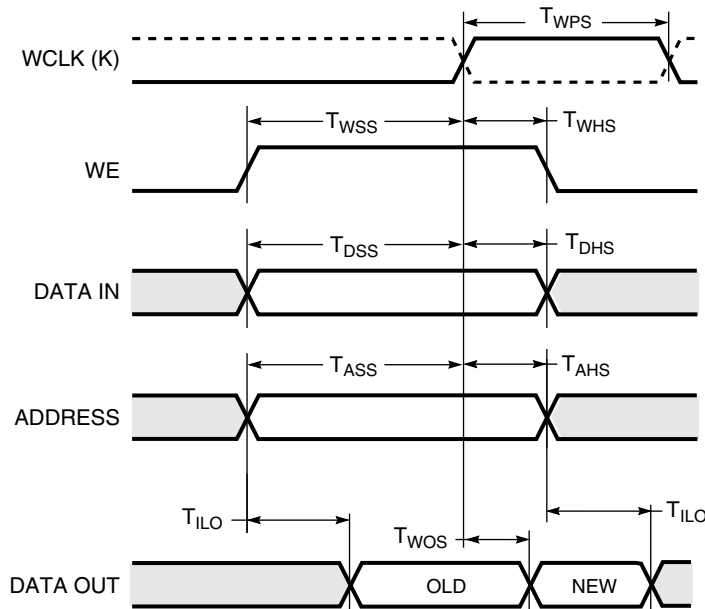
Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation ⁽¹⁾							
T _{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T _{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T _{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T _{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T _{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T _{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

Notes:

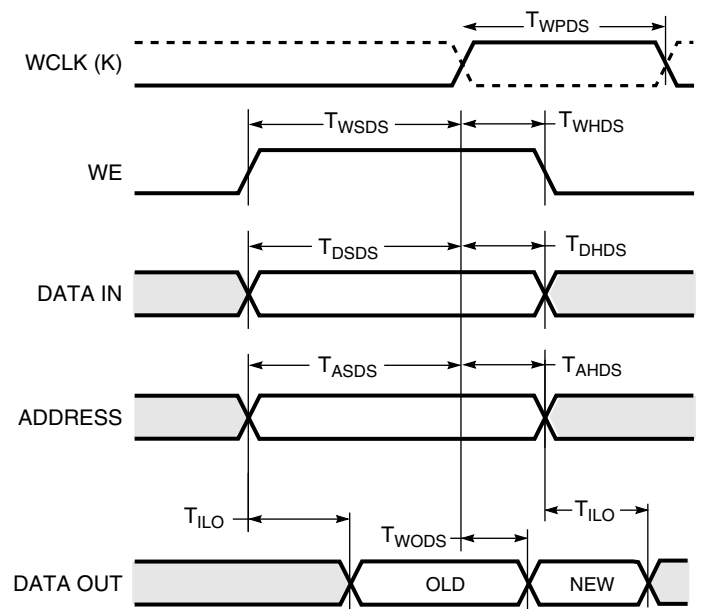
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



DS060_34_011300

Spartan-XL Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case oper-

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Global Clock to Output using OFF					
T _{ICKOF}	Fast	XCS05XL	4.6	5.2	ns
		XCS10XL	4.9	5.5	ns
		XCS20XL	5.2	5.8	ns
		XCS30XL	5.5	6.2	ns
		XCS40XL	5.8	6.5	ns
Slew Rate Adjustment					
T _{SLOW}	For Output SLOW option add	All Devices	1.5	1.7	ns

Notes:

1. Output delays are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.
3. OFF = Output Flip Flop

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84(4)	VQ100	CS144(2,4)	TQ144	Bndry Scan
I/O	P80	P81	A10	P116	17
GND	-	-	C9	P118	-
I/O	-	-	B9	P119	20
I/O	-	-	A9	P120	23
I/O	P81	P82	D8	P121	26
I/O	P82	P83	C8	P122	29
I/O	-	P84	B8	P123	32
I/O	-	P85	A8	P124	35
I/O	P83	P86	B7	P125	38
I/O	P84	P87	A7	P126	41
GND	P1	P88	C7	P127	-

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS10XL is not part of the Boundary Scan chain. For the XCS10XL, subtract 1 from all Boundary Scan numbers from GCK3 on (175 and higher).
4. PC84 and CS144 packages discontinued by [PDN2004-01](#)

Additional XCS10/XL Package Pins

TQ144					
Not Connected Pins					
P117	-	-	-	-	-
5/5/97					

CS144					
Not Connected Pins					
D9	-	-	-	-	-
4/28/99					

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144(2,4)	TQ144	PQ208	Bndry Scan
VCC	P89	D7	P128	P183	-
I/O	P90	A6	P129	P184	62
I/O	P91	B6	P130	P185	65
I/O	P92	C6	P131	P186	68
I/O	P93	D6	P132	P187	71
I/O	-	-	-	P188	74
I/O	-	-	-	P189	77
I/O	P94	A5	P133	P190	80
I/O	P95	B5	P134	P191	83
VCC ⁽²⁾	-	-	-	P192	-
I/O	-	C5	P135	P193	86
I/O	-	D5	P136	P194	89
GND	-	A4	P137	P195	-
I/O	-	-	-	P196	92
I/O	-	-	-	P197	95
I/O	-	-	-	P198	98
I/O	-	-	-	P199	101
I/O	P96	B4	P138	P200	104
I/O	P97	C4	P139	P201	107
I/O	-	A3	P140	P204	110
I/O	-	B3	P141	P205	113
I/O	P98	C3	P142	P206	116

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144(2,4)	TQ144	PQ208	Bndry Scan
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P99	A2	P143	P207	119
VCC	P100	B2	P144	P208	-
GND	P1	A1	P1	P1	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	B1	P2	P2	122
I/O	P3	C2	P3	P3	125
I/O	-	C1	P4	P4	128
I/O	-	D4	P5	P5	131
I/O, TDI	P4	D3	P6	P6	134
I/O, TCK	P5	D2	P7	P7	137
I/O	-	-	-	P8	140
I/O	-	-	-	P9	143
I/O	-	-	-	P10	146
I/O	-	-	-	P11	149
GND	-	D1	P8	P13	-
I/O	-	E4	P9	P14	152
I/O	-	E3	P10	P15	155
I/O, TMS	P6	E2	P11	P16	158
I/O	P7	E1	P12	P17	161
VCC ⁽²⁾	-	-	-	P18	-
I/O	-	-	-	P19	164
I/O	-	-	-	P20	167

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC ⁽²⁾	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P21	L2	P33	P49	239
Not Connected ⁽¹⁾ M1 ⁽²⁾	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected ⁽¹⁾ PWRDWN ⁽²⁾	P26	N2	P38	P54	246 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P27	M3	P39	P55	247 ⁽³⁾
I/O (HDC)	P28	N3	P40	P56	250 ⁽³⁾
I/O	-	K4	P41	P57	253 ⁽³⁾
I/O	-	L4	P42	P58	256 ⁽³⁾
I/O	P29	M4	P43	P59	259 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O (LDC)	P30	N4	P44	P60	262 ⁽³⁾
I/O	-	-	-	P61	265 ⁽³⁾
I/O	-	-	-	P62	268 ⁽³⁾
I/O	-	-	-	P63	271 ⁽³⁾
I/O	-	-	-	P64	274 ⁽³⁾
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 ⁽³⁾
I/O	-	M5	P47	P68	280 ⁽³⁾
I/O	P31	N5	P48	P69	283 ⁽³⁾
I/O	P32	K6	P49	P70	286 ⁽³⁾
VCC ⁽²⁾	-	-	-	P71	-
I/O	-	-	-	P72	289 ⁽³⁾
I/O	-	-	-	P73	292 ⁽³⁾
I/O	P33	L6	P50	P74	295 ⁽³⁾
I/O	P34	M6	P51	P75	298 ⁽³⁾
I/O	P35	N6	P52	P76	301 ⁽³⁾
I/O (INIT)	P36	M7	P53	P77	304 ⁽³⁾
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 ⁽³⁾
I/O	P40	N8	P57	P81	310 ⁽³⁾
I/O	P41	M8	P58	P82	313 ⁽³⁾
I/O	P42	L8	P59	P83	316 ⁽³⁾
I/O	-	-	-	P84	319 ⁽³⁾
I/O	-	-	-	P85	322 ⁽³⁾
VCC ⁽²⁾	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 ⁽³⁾
I/O	P44	N9	P61	P88	328 ⁽³⁾
I/O	-	M9	P62	P89	331 ⁽³⁾
I/O	-	L9	P63	P90	334 ⁽³⁾
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 ⁽³⁾
I/O	-	-	-	P94	340 ⁽³⁾
I/O	-	-	-	P95	343 ⁽³⁾
I/O	-	-	-	P96	346 ⁽³⁾
I/O	P45	N10	P65	P97	349 ⁽³⁾
I/O	P46	M10	P66	P98	352 ⁽³⁾
I/O	-	L10	P67	P99	355 ⁽³⁾
I/O	-	N11	P68	P100	358 ⁽³⁾
I/O	P47	M11	P69	P101	361 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P48	L11	P70	P102	364 ⁽³⁾
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 ⁽¹⁾	P33 ⁽¹⁾	P39	P65	P71 ⁽¹⁾
P86 ⁽¹⁾	P92	P111	P121 ⁽¹⁾	P140 ⁽¹⁾	P144
P165	P173 ⁽¹⁾	P192 ⁽¹⁾	P202	P203	-
9/16/98					

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by [PDN2004-01](#)

XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
VCC	P89	P128	P183	P212	VCC ⁽⁴⁾	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC ⁽⁴⁾	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC ⁽⁴⁾	A1	-
GND	P1	P1	P1	P1	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
GND	P25	P29	GND ⁽⁴⁾	GND ⁽⁴⁾	-
VCC	P26	P30	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P27	P31	L2	K3	254
I/O	P28	P32	L3	K4	257
I/O	P29	P33	L4	K5	260
I/O	P30	P34	M1	L1	263
I/O	P31	P35	M2	L2	266
I/O	P32	P36	M3	L3	269
I/O	-	-	M4	L4	272
I/O	-	-	-	M1	275
I/O	-	P38	N1	M2	278
I/O	-	P39	N2	M3	281
VCC	P33	P40	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P34	P41	P1	N1	284
I/O	P35	P42	P2	N2	287
I/O	P36	P43	R1	N3	290
I/O	P37	P44	P3	N4	293
GND	P38	P45	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P46	T1	P1	296
I/O	P39	P47	R3	P2	299
I/O	P40	P48	T2	P3	302
I/O	P41	P49	U1	P4	305
I/O	P42	P50	T3	P5	308
I/O	P43	P51	U2	R1	311
I/O	-	-	-	R2	314
I/O	-	-	-	R4	317
I/O	P44	P52	V1	T1	320
I/O	P45	P53	T4	T2	323
I/O	P46	P54	U3	T3	326
I/O	P47	P55	V2	U1	329
I/O	P48	P56	W1	V1	332
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P49	P57	V3	U2	335
Not Connected ⁽¹⁾ M1 ⁽²⁾	P50	P58	W2	V2	338
GND	P51	P59	GND ⁽⁴⁾	GND ⁽⁴⁾	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P52	P60	Y1	W1	341
VCC	P53	P61	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
Not Connected ⁽¹⁾ PWRDWN ⁽²⁾	P54	P62	W3	V3	342 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P55	P63	Y2	W2	343 ⁽³⁾

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
I/O (HDC)	P56	P64	W4	W3	346 ⁽³⁾
I/O	P57	P65	V4	T4	349 ⁽³⁾
I/O	P58	P66	U5	U4	352 ⁽³⁾
I/O	P59	P67	Y3	V4	355 ⁽³⁾
I/O (LDC)	P60	P68	Y4	W4	358 ⁽³⁾
I/O	-	-	-	R5	361 ⁽³⁾
I/O	-	-	-	U5	364 ⁽³⁾
I/O	P61	P69	V5	T5	367 ⁽³⁾
I/O	P62	P70	W5	W5	370 ⁽³⁾
I/O	P63	P71	Y5	R6	373 ⁽³⁾
I/O	P64	P72	V6	U6	376 ⁽³⁾
I/O	P65	P73	W6	V6	379 ⁽³⁾
I/O	-	P74	Y6	T6	382 ⁽³⁾
GND	P66	P75	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P67	P76	W7	W6	385 ⁽³⁾
I/O	P68	P77	Y7	U7	388 ⁽³⁾
I/O	P69	P78	V8	V7	391 ⁽³⁾
I/O	P70	P79	W8	W7	394 ⁽³⁾
VCC	P71	P80	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P72	P81	Y8	W8	397 ⁽³⁾
I/O	P73	P82	U9	U8	400 ⁽³⁾
I/O	-	-	V9	V8	403 ⁽³⁾
I/O	-	-	W9	T8	406 ⁽³⁾
I/O	-	P84	Y9	W9	409 ⁽³⁾
I/O	-	P85	W10	V9	412 ⁽³⁾
I/O	P74	P86	V10	U9	415 ⁽³⁾
I/O	P75	P87	Y10	T9	418 ⁽³⁾
I/O	P76	P88	Y11	W10	421 ⁽³⁾
I/O (INIT)	P77	P89	W11	V10	424 ⁽³⁾
VCC	P78	P90	VCC ⁽⁴⁾	VCC ⁽⁴⁾	VCC ⁽⁴⁾
GND	P79	P91	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P80	P92	V11	T10	427 ⁽³⁾
I/O	P81	P93	U11	R10	430 ⁽³⁾
I/O	P82	P94	Y12	W11	433 ⁽³⁾
I/O	P83	P95	W12	V11	436 ⁽³⁾
I/O	P84	P96	V12	U11	439 ⁽³⁾
I/O	P85	P97	U12	T11	442 ⁽³⁾
I/O	-	-	Y13	W12	445 ⁽³⁾
I/O	-	-	W13	V12	448 ⁽³⁾
I/O	-	P99	V13	U12	451 ⁽³⁾
I/O	-	P100	Y14	T12	454 ⁽³⁾
VCC	P86	P101	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P87	P102	Y15	V13	457 ⁽³⁾
I/O	P88	P103	V14	U13	460 ⁽³⁾
I/O	P89	P104	W15	T13	463 ⁽³⁾

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
O, TDO	P157	P181	A19	B17	0
GND	P158	P182	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P159	P183	B18	A18	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P160	P184	B17	A17	5
I/O	P161	P185	C17	D16	8
I/O	P162	P186	D16	C16	11
I/O (CS1 ⁽²⁾)	P163	P187	A18	B16	14
I/O	P164	P188	A17	A16	17
I/O	-	-	-	E15	20
I/O	-	-	-	C15	23
I/O	P165	P189	C16	D15	26
I/O	-	P190	B16	A15	29
I/O	P166	P191	A16	E14	32
I/O	P167	P192	C15	C14	35
I/O	P168	P193	B15	B14	38
I/O	P169	P194	A15	D14	41
GND	P170	P196	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P171	P197	B14	A14	44
I/O	P172	P198	A14	C13	47
I/O	-	P199	C13	B13	50
I/O	-	P200	B13	A13	53
VCC	P173	P201	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	-	A13	A12	56
I/O	-	-	D12	C12	59
I/O	P174	P202	C12	B12	62
I/O	P175	P203	B12	D12	65
I/O	P176	P205	A12	A11	68
I/O	P177	P206	B11	B11	71
I/O	P178	P207	C11	C11	74
I/O	P179	P208	A11	D11	77
I/O	P180	P209	A10	A10	80
I/O	P181	P210	B10	B10	83
GND	P182	P211	GND ⁽⁴⁾	GND ⁽⁴⁾	-

2/8/00

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS40XL is not part of the Boundary Scan chain. For the XCS40XL, subtract 1 from all Boundary Scan numbers from GCK3 on (343 and higher).
4. Pads labeled GND⁽⁴⁾ or VCC⁽⁴⁾ are internally bonded to Ground or VCC planes within the package.
5. CS280 package discontinued by [PDN2004-01](#)

Additional XCS40/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

2/12/98

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

6/17/97

CS280

VCC Pins					
A1	A7	B5	B15	C10	C17
D13	E3	E18	G1	G19	K2
K17	M4	N16	R3	R18	T7
U3	U10	U17	V5	V15	W13
GND Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-

5/19/99

Revision History

The following table shows the revision history for this document.

Date	Version	Description
11/20/98	1.3	Added Spartan-XL specs and Power Down.
01/06/99	1.4	All Spartan-XL -4 specs designated Preliminary with no changes.
03/02/00	1.5	Added CS package, updated Spartan-XL specs to Final.
09/19/01	1.6	Reformatted, updated power specs, clarified configuration information. Removed T_{SOL} soldering information from Absolute Maximum Ratings table. Changed Figure 26 : Slave Serial Mode Characteristics: T_{CCH} , T_{CCL} from 45 to 40 ns. Changed Master Mode Configuration Switching Characteristics: T_{CCLK} min. from 80 to 100 ns. Added Total Dist. RAM Bits to Table 1 ; added Start-Up, page 36 characteristics.
06/27/02	1.7	Clarified Express Mode pseudo daisy chain. Added new Industrial options. Clarified XCS30XL CS280 V_{CC} pinout.
06/26/08	1.8	Noted that PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, are discontinued by PDN2004-01 . Extended description of recommended maximum delay of reconfiguration in Delaying Configuration After Power-Up, page 35 . Added reference to Pb-free package options and provided link to Package Specifications, page 81 . Updated links.
03/01/13	2.0	The products listed in this data sheet are obsolete. See XCN10016 and XCN11010 for further information.