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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

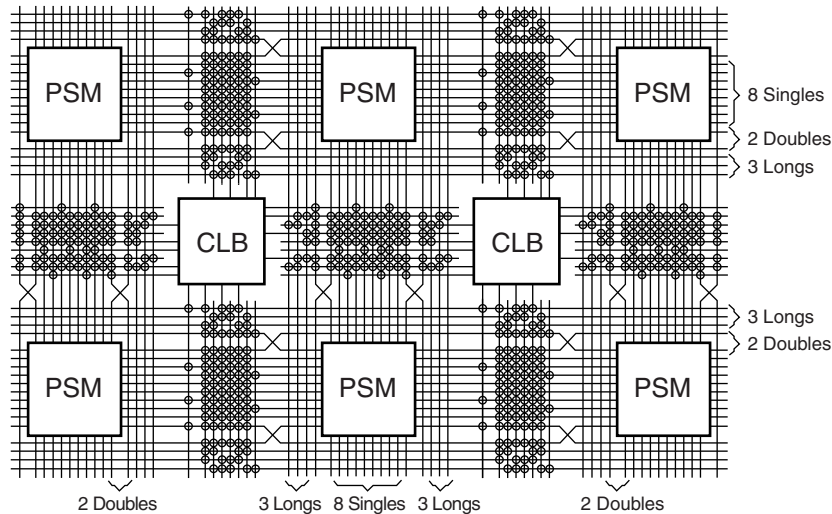
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	205
Number of Gates	40000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40-3bg256c

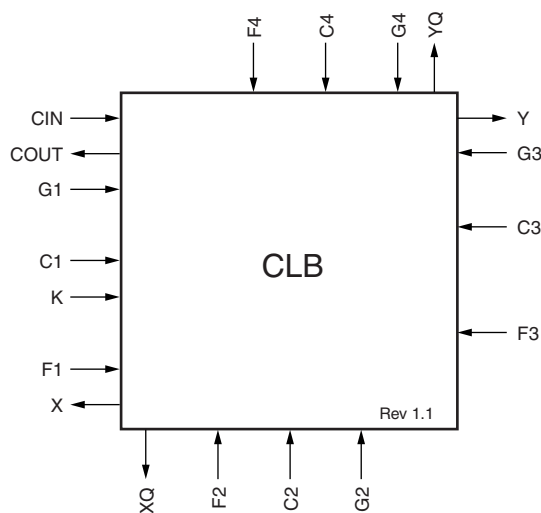


DS060_09_041901

Figure 8: Spartan/XL CLB Routing Channels and Interface Block Diagram

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.



DS060_08_081100

Figure 9: CLB Interconnect Signals

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs. Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

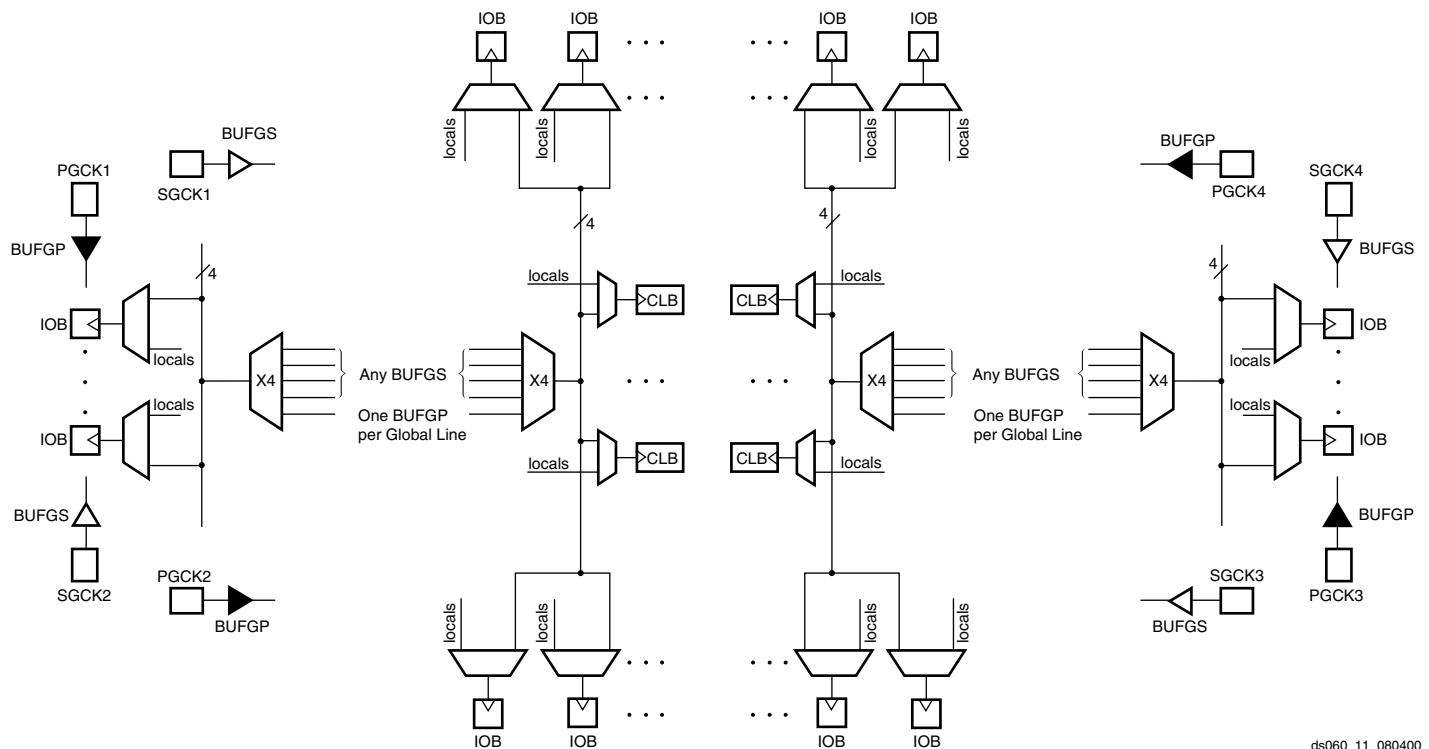


Figure 11: 5V Spartan Family Global Net Distribution

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16×1 , $(16 \times 1) \times 2$, or 32×1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16×1 RAM array. The different CLB memory configurations are summarized in [Table 8](#). Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 8: CLB Memory Configurations

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√	—	—

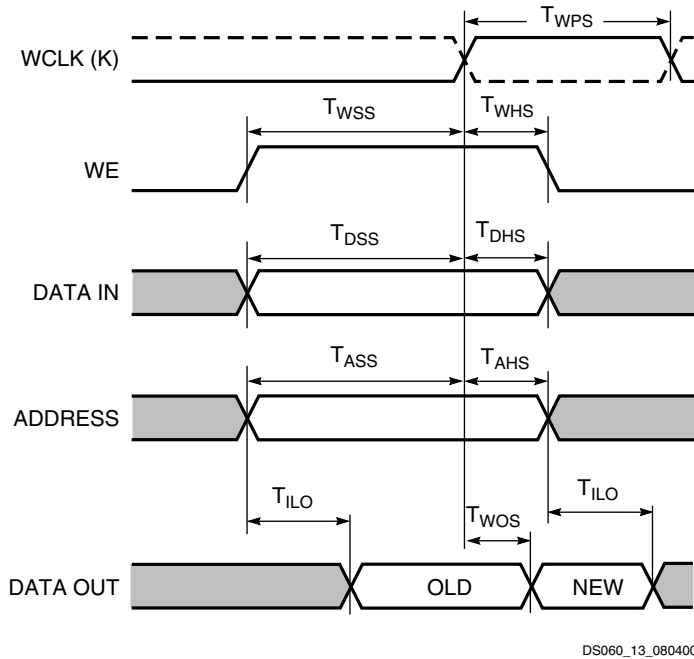


Figure 13: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be

inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO} , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS} , the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by $A[3:0]$ while the second provides only for read operations at the address specified independently by $DPRA[3:0]$. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the

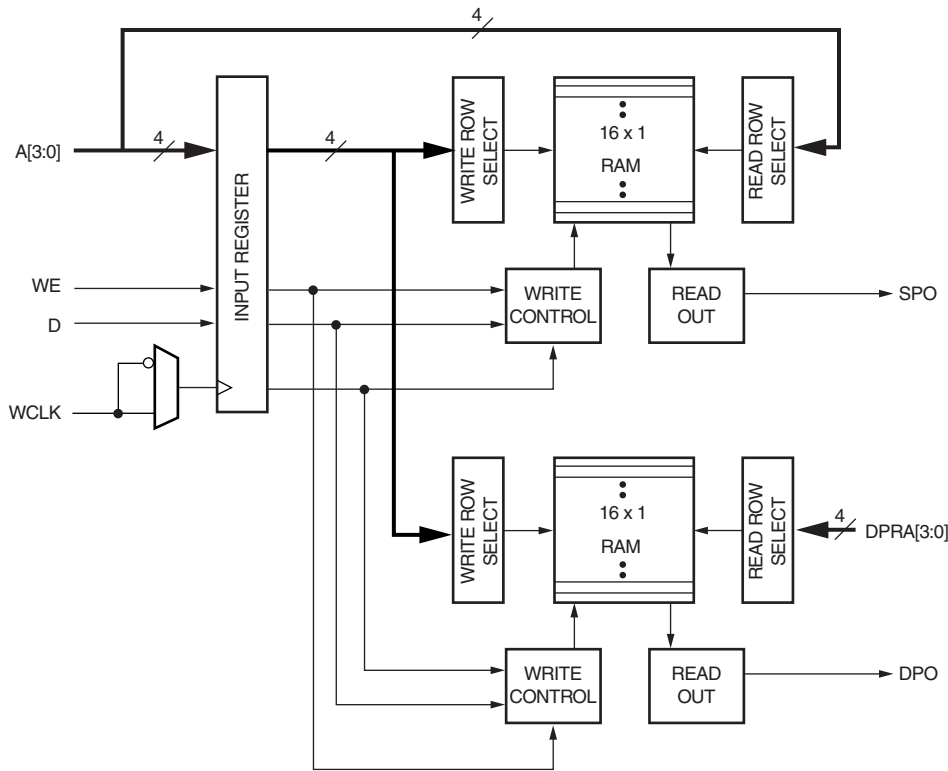


Figure 14: Logic Diagram for the Dual-Port RAM

and Spartan-XL families, speeding up arithmetic and counting functions.

The carry chain in 5V Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in Spartan-XL devices can only run up the column, providing even higher speed.

Figure 16, page 18 shows a Spartan/XL FPGA CLB with dedicated fast carry logic. The carry logic shares operand

and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 17, page 19 shows the details of the Spartan/XL FPGA carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 16.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.

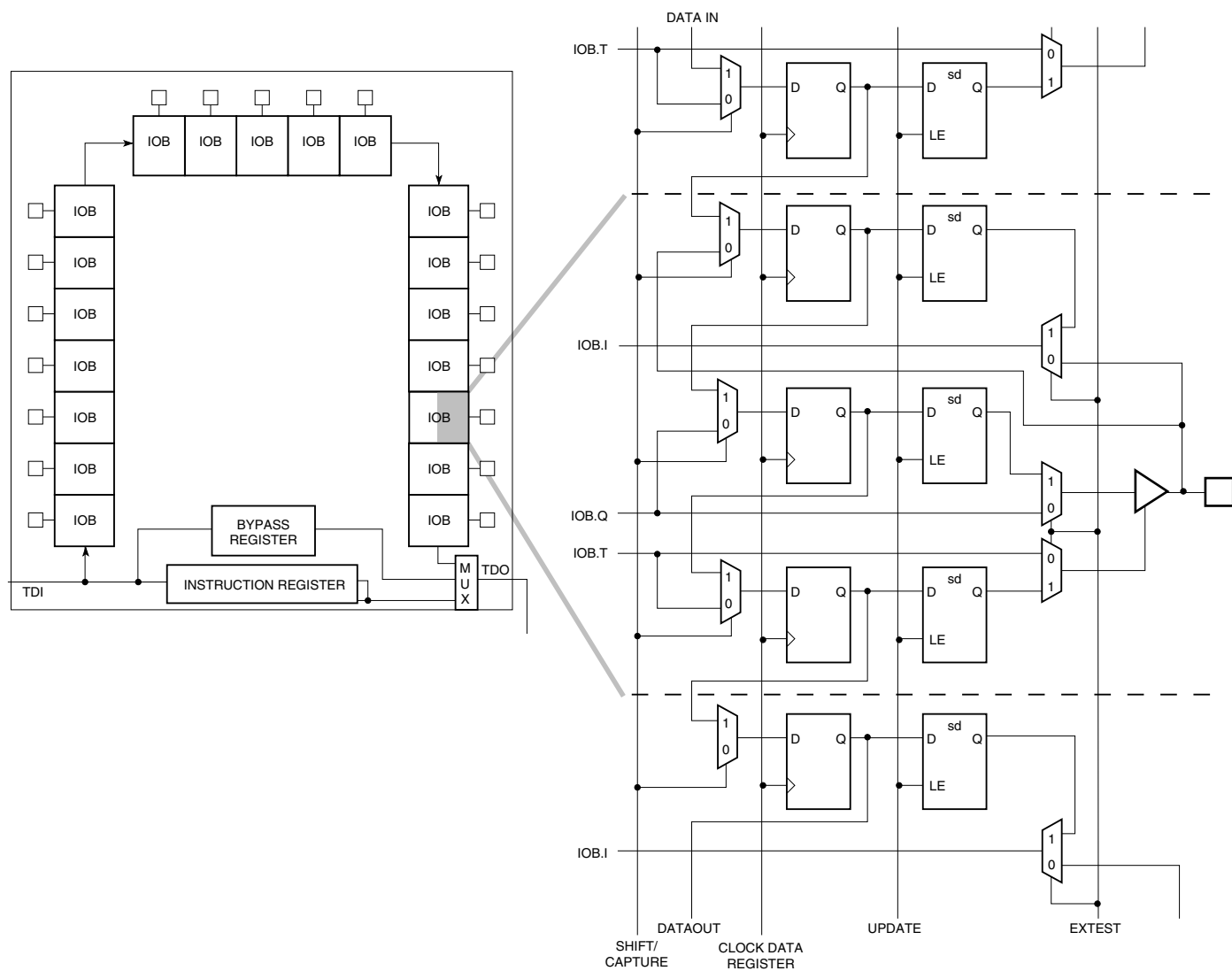


Figure 20: Spartan/XL Boundary Scan Logic

figuration are shown in Table 14 and Table 15.

Table 14: Pin Functions During Configuration (Spartan Family Only)

Configuration Mode (MODE Pin)		User Operation
Slave Serial (High)	Master Serial (Low)	
MODE (I)	MODE (I)	MODE
HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

Notes:

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Table 15: Pin Functions During Configuration (Spartan-XL Family Only)

CONFIGURATION MODE <M1:M0>			User Operation
Slave Serial [1:1]	Master Serial [1:0]	Express [0:X]	
M1 (High) (I)	M1 (High) (I)	M1(Low) (I)	M1
M0 (High) (I)	M0 (Low) (I)	M0 (I)	M0
HDC (High)	HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

Notes:

1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Table 17: Spartan/XL Program Data

Device	XCS05		XCS10		XCS20		XCS30		XCS40	
Max System Gates	5,000		10,000		20,000		30,000		40,000	
CLBs (Row x Col.)	100 (10 x 10)		196 (14 x 14)		400 (20 x 20)		576 (24 x 24)		784 (28 x 28)	
I/Os	80		112		160		192		205 ⁽⁴⁾	
Part Number	XCS05	XCS05XL	XCS10	XCS10XL	XCS20	XCS20XL	XCS30	XCS30XL	XCS40	XCS40XL
Supply Voltage	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V
Bits per Frame	126	127	166	167	226	227	266	267	306	307
Frames	428	429	572	573	788	789	932	933	1,076	1,077
Program Data	53,936	54,491	94,960	95,699	178,096	179,111	247,920	249,119	329,264	330,647
PROM Size (bits)	53,984	54,544	95,008	95,752	178,144	179,160	247,968	249,168	329,312	330,696
Express Mode PROM Size (bits)	-	79,072	-	128,488	-	221,056	-	298,696	-	387,856

Notes:

- Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits (+1 for Spartan-XL device)
 Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1 (+ 1 for Spartan-XL device)
 Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
 PROM Size = Program Data + 40 (header) + 8, rounded up to the nearest byte
- The user can add more "1" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.
- Express mode adds 57 (XCS05XL, XCS10XL), or 53 (XCS20XL, XCS30XL, XCS40XL) bits per frame, + additional start-up bits.
- XCS40XL provided 224 max I/O in CS280 package discontinued by [PDN2004-01](#).

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in [Figure 29](#). The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback

data is independent of the current device state. CLB outputs should not be included (Readback Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

to wait after completing the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing the state of the Mode pins, and is ready to start the configuration process. A master device waits up to an additional 300 μs to make sure that any slaves in the optional daisy chain have seen that $\overline{\text{INIT}}$ is High.

For more details on Configuration, refer to the Xilinx Application Note "FPGA Configuration Guidelines" (XAPP090).

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user system. Start-up must make sure that the user logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the Global Set/Reset (GSR) at the right time.

Start-Up Initiation

Two conditions have to be met in order for the start-up sequence to begin:

- The chip's internal memory must be full, and
- The configuration length count must be met, exactly.

In all configuration modes except Express mode, Spartan/XL devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

In Express mode, there is no length count. The start-up sequence for each device begins when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

Start-Up Events

The device can be programmed to control three start-up events.

- The release of the open-drain DONE output
- The termination of the Global Three-State and the change of configuration-related pins to the user function, activating all IOBs.
- The termination of the Global Set/Reset initialization of all CLB and IOB storage elements.

Figure 31 describes start-up timing in detail. The three events — DONE going High, the internal GSR being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. This relative timing is selected by options in the bitstream generation software. Heavy lines in Figure 31 show the default timing. The thin lines indicate all other possible timing options. The start-up logic must be clocked until the "F" (Finished) state is reached.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. GSR is then released another clock period later to make sure that user operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 31, but the designer can modify it to meet particular requirements.

Start-Up Clock

Normally, the start-up sequence is controlled by the internal device oscillator (CCLK), which is asynchronous to the system clock. As a configuration option, they can be triggered by an on-chip user net called UCLK. This user net can be accessed by placing the STARTUP library symbol, and the start-up modes are known as UCLK_NOSYNC or UCLK_SYNC. This allows the device to wake up in synchronism with the user system.

DONE Pin

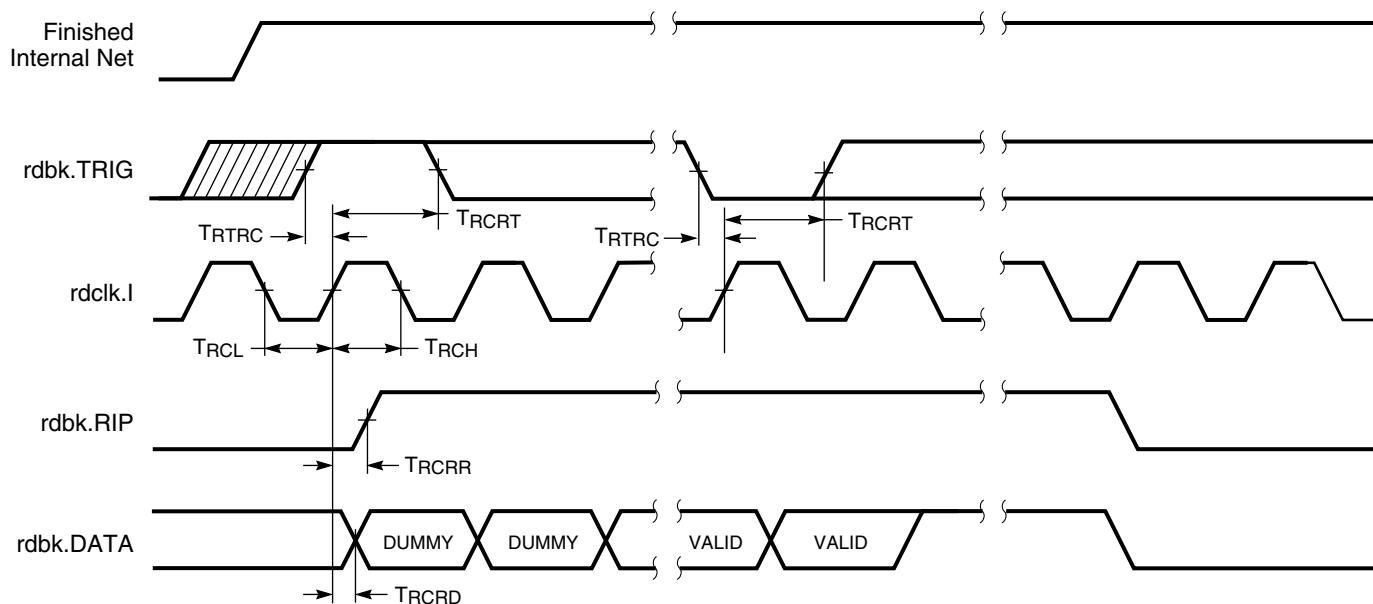
Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to the start-up control logic. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK_SYNC or UCLK_SYNC. When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK_NOSYNC or UCLK_NOSYNC. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, while the other configuration modes can use any of the four timing sequences.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.



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Figure 33: Spartan and Spartan-XL Readback Timing Diagram

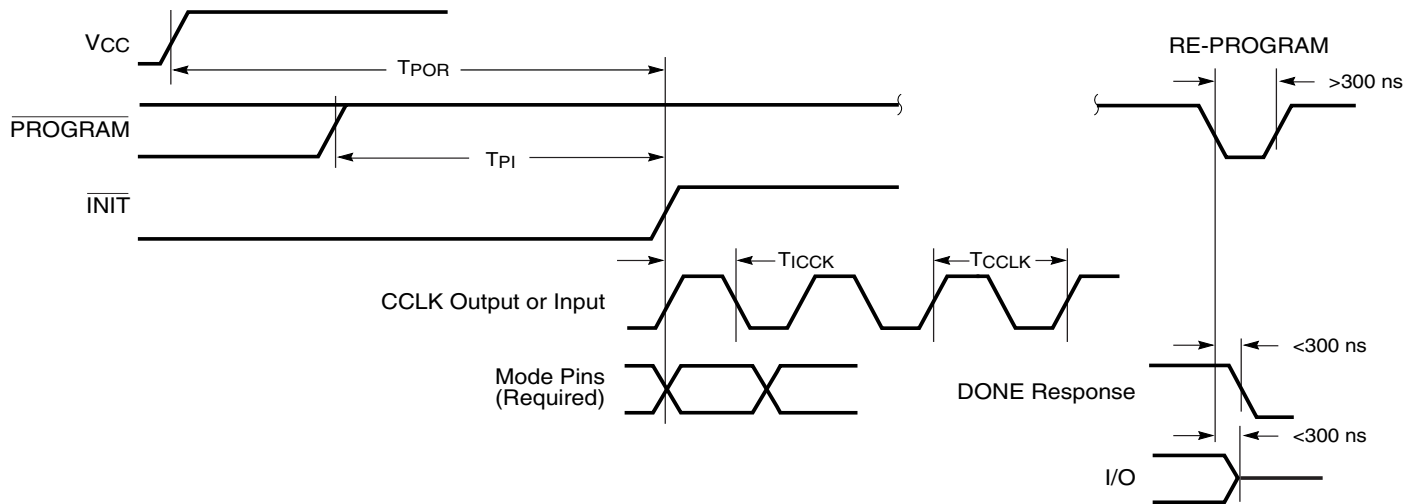
Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:

1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Configuration Switching Characteristics



DS060_33_080400

Master Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	40	130	ms
T_{PI}	Program Latency	30	200	μ s per CLB column
T_{ICCK}	CCLK (output) delay	40	250	μ s
T_{CCLK}	CCLK (output) period, slow	640	2000	ns
T_{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Max	Units
T_{POR}	Power-on reset	10	33	ms
T_{PI}	Program latency	30	200	μ s per CLB column
T_{ICCK}	CCLK (input) delay (required)	4	-	μ s
T_{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

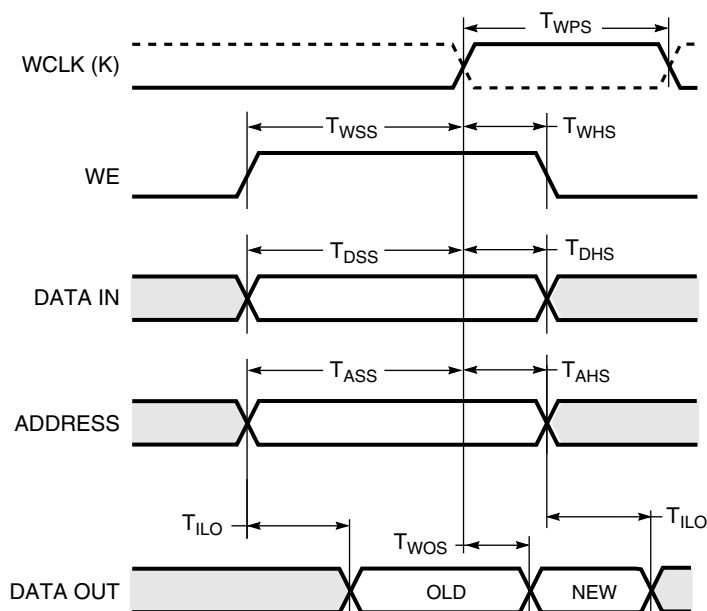
Symbol	Dual Port RAM	Size ⁽¹⁾	-4		-3		Units
			Min	Max	Min	Max	
Write Operation							
T _{WCDS}	Address write cycle time (clock K period)	16x1	8.0	-	11.6	-	ns
T _{WPDS}	Clock K pulse width (active edge)	16x1	4.0	-	5.8	-	ns
T _{ASDS}	Address setup time before clock K	16x1	1.5	-	2.1	-	ns
T _{AHDS}	Address hold time after clock K	16x1	0	-	0	-	ns
T _{DSDS}	DIN setup time before clock K	16x1	1.5	-	1.6	-	ns
T _{DHDS}	DIN hold time after clock K	16x1	0	-	0	-	ns
T _{WSDS}	WE setup time before clock K	16x1	1.5	-	1.6	-	ns
T _{WHDS}	WE hold time after clock K	16x1	0	-	0	-	ns
T _{WODS}	Data valid after clock K	16x1	-	6.5	-	7.0	ns

Notes:

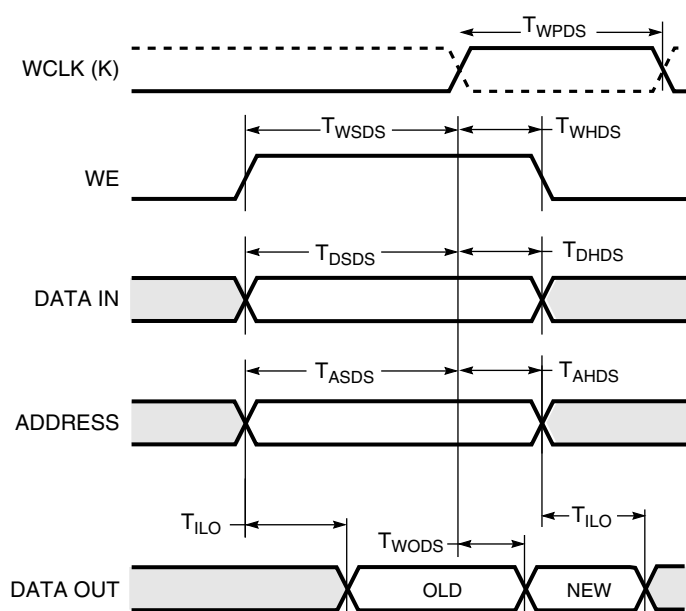
- Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



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Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Min	Min	
Input Setup/Hold Times Using Primary Clock and IFF					
T _{PSUF} /T _{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T _{PSU} /T _{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T _{SSUF} /T _{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T _{SSU} /T _{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:

1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings⁽¹⁾

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked ^(2, 3)	–0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	–0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked ^(2, 3)	–0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	–0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0V or overshoot to $V_{CC} + 2.0V$, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ ⁽¹⁾	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage ⁽²⁾		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage ⁽²⁾		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:

- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement threshold is ~50% of V_{CC} .

Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See **Global Signals: GSR and GTS**, page 20 for more information.

Device pins for Spartan/XL devices are described in **Table 18**.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pin-outs as the standard package options.

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
V _{CC}	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 – 0.1 μ F capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See Violating the Maximum High and Low Time Specification for the Readback Clock , page 39 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an open-drain output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.

Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and Spartan-XL device. They follow the pad locations around the die, and include boundary scan register locations.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 ⁽⁴⁾	VQ100	Bndry Scan
VCC	P2	P89	-
I/O	P3	P90	32
I/O	P4	P91	35
I/O	-	P92	38
I/O	-	P93	41
I/O	P5	P94	44
I/O	P6	P95	47
I/O	P7	P96	50
I/O	P8	P97	53
I/O	P9	P98	56
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P10	P99	59
VCC	P11	P100	-
GND	P12	P1	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P13	P2	62
I/O	P14	P3	65
I/O, TDI	P15	P4	68
I/O, TCK	P16	P5	71
I/O, TMS	P17	P6	74
I/O	P18	P7	77
I/O	-	P8	83
I/O	P19	P9	86
I/O	P20	P10	89
GND	P21	P11	-
VCC	P22	P12	-
I/O	P23	P13	92
I/O	P24	P14	95
I/O	-	P15	98
I/O	P25	P16	104
I/O	P26	P17	107
I/O	P27	P18	110
I/O	-	P19	113
I/O	P28	P20	116
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P29	P21	119
Not Connected ⁽¹⁾ , M1 ⁽²⁾	P30	P22	122
GND	P31	P23	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P32	P24	125
VCC	P33	P25	-

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 ⁽⁴⁾	VQ100	Bndry Scan
Not Connected ⁽¹⁾ , PWRDWN ⁽²⁾	P34	P26	126 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P35	P27	127 ⁽³⁾
I/O (HDC)	P36	P28	130 ⁽³⁾
I/O	-	P29	133 ⁽³⁾
I/O (LDC)	P37	P30	136 ⁽³⁾
I/O	P38	P31	139 ⁽³⁾
I/O	P39	P32	142 ⁽³⁾
I/O	-	P33	145 ⁽³⁾
I/O	-	P34	148 ⁽³⁾
I/O	P40	P35	151 ⁽³⁾
I/O (INIT)	P41	P36	154 ⁽³⁾
VCC	P42	P37	-
GND	P43	P38	-
I/O	P44	P39	157 ⁽³⁾
I/O	P45	P40	160 ⁽³⁾
I/O	-	P41	163 ⁽³⁾
I/O	-	P42	166 ⁽³⁾
I/O	P46	P43	169 ⁽³⁾
I/O	P47	P44	172 ⁽³⁾
I/O	P48	P45	175 ⁽³⁾
I/O	P49	P46	178 ⁽³⁾
I/O	P50	P47	181 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P51	P48	184 ⁽³⁾
GND	P52	P49	-
DONE	P53	P50	-
VCC	P54	P51	-
PROGRAM	P55	P52	-
I/O (D7 ⁽²⁾)	P56	P53	187 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P57	P54	190 ⁽³⁾
I/O (D6 ⁽²⁾)	P58	P55	193 ⁽³⁾
I/O	-	P56	196 ⁽³⁾
I/O (D5 ⁽²⁾)	P59	P57	199 ⁽³⁾
I/O	P60	P58	202 ⁽³⁾
I/O	-	P59	205 ⁽³⁾
I/O	-	P60	208 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	P61	211 ⁽³⁾
I/O	P62	P62	214 ⁽³⁾
VCC	P63	P63	-
GND	P64	P64	-
I/O (D3 ⁽²⁾)	P65	P65	217 ⁽³⁾
I/O	P66	P66	220 ⁽³⁾
I/O	-	P67	223 ⁽³⁾
I/O (D2 ⁽²⁾)	P67	P68	229 ⁽³⁾
I/O	P68	P69	232 ⁽³⁾
I/O (D1 ⁽²⁾)	P69	P70	235 ⁽³⁾

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	P5	P5	P5	D3	C1	155
I/O, TDI	P4	P6	P6	P6	E4	D4	158
I/O, TCK	P5	P7	P7	P7	C1	D3	161
I/O	-	-	P8	P8	D1	E2	164
I/O	-	-	P9	P9	E3	E4	167
I/O	-	-	P10	P10	E2	E1	170
I/O	-	-	P11	P11	E1	F5	173
I/O	-	-	P12	P12	F3	F3	176
I/O	-	-	-	P13	F2	F2	179
GND	-	P8	P13	P14	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P9	P14	P15	G3	F4	182
I/O	-	P10	P15	P16	G2	F1	185
I/O, TMS	P6	P11	P16	P17	G1	G3	188
I/O	P7	P12	P17	P18	H3	G2	191
VCC	-	-	P18	P19	VCC ⁽⁴⁾	G1	-
I/O	-	-	-	P20	H2	G4	194
I/O	-	-	-	P21	H1	H1	197
I/O	-	-	P19	P23	J2	H4	200
I/O	-	-	P20	P24	J1	J1	203
I/O	-	P13	P21	P25	K2	J2	206
I/O	P8	P14	P22	P26	K3	J3	209
I/O	P9	P15	P23	P27	K1	J4	212
I/O	P10	P16	P24	P28	L1	K1	215
GND	P11	P17	P25	P29	GND ⁽⁴⁾	GND ⁽⁴⁾	-
VCC	P12	P18	P26	P30	VCC ⁽⁴⁾	K2	-
I/O	P13	P19	P27	P31	L2	K3	218
I/O	P14	P20	P28	P32	L3	K4	221
I/O	P15	P21	P29	P33	L4	K5	224
I/O	-	P22	P30	P34	M1	L1	227
I/O	-	-	P31	P35	M2	L2	230
I/O	-	-	P32	P36	M3	L3	233
I/O	-	-	-	P38	N1	M2	236
I/O	-	-	-	P39	N2	M3	239
VCC	-	-	P33	P40	VCC ⁽⁴⁾	M4	-
I/O	P16	P23	P34	P41	P1	N1	242
I/O	P17	P24	P35	P42	P2	N2	245
I/O	-	P25	P36	P43	R1	N3	248
I/O	-	P26	P37	P44	P3	N4	251
GND	-	P27	P38	P45	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P46	T1	P1	254
I/O	-	-	P39	P47	R3	P2	257
I/O	-	-	P40	P48	T2	P3	260
I/O	-	-	P41	P49	U1	P4	263
I/O	-	-	P42	P50	T3	P5	266
I/O	-	-	P43	P51	U2	R1	269

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	P18	P28	P44	P52	V1	T1	272
I/O	P19	P29	P45	P53	T4	T2	275
I/O	-	P30	P46	P54	U3	T3	278
I/O	-	P31	P47	P55	V2	U1	281
I/O	P20	P32	P48	P56	W1	V1	284
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P21	P33	P49	P57	V3	U2	287
Not Connected ⁽¹⁾ , M1 ⁽²⁾	P22	P34	P50	P58	W2	V2	290
GND	P23	P35	P51	P59	GND ⁽⁴⁾	GND ⁽⁴⁾	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P24	P36	P52	P60	Y1	W1	293
VCC	P25	P37	P53	P61	VCC ⁽⁴⁾	U3	-
Not Connected ⁽¹⁾ , PWRDWN ⁽²⁾	P26	P38	P54	P62	W3	V3	294 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P27	P39	P55	P63	Y2	W2	295 ⁽³⁾
I/O (HDC)	P28	P40	P56	P64	W4	W3	298 ⁽³⁾
I/O	-	P41	P57	P65	V4	T4	301 ⁽³⁾
I/O	-	P42	P58	P66	U5	U4	304 ⁽³⁾
I/O	P29	P43	P59	P67	Y3	V4	307 ⁽³⁾
I/O (LDC)	P30	P44	P60	P68	Y4	W4	310 ⁽³⁾
I/O	-	-	P61	P69	V5	T5	313 ⁽³⁾
I/O	-	-	P62	P70	W5	W5	316 ⁽³⁾
I/O	-	-	P63	P71	Y5	R6	319 ⁽³⁾
I/O	-	-	P64	P72	V6	U6	322 ⁽³⁾
I/O	-	-	P65	P73	W6	V6	325 ⁽³⁾
I/O	-	-	-	P74	Y6	T6	328 ⁽³⁾
GND	-	P45	P66	P75	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P46	P67	P76	W7	W6	331 ⁽³⁾
I/O	-	P47	P68	P77	Y7	U7	334 ⁽³⁾
I/O	P31	P48	P69	P78	V8	V7	337 ⁽³⁾
I/O	P32	P49	P70	P79	W8	W7	340 ⁽³⁾
VCC	-	-	P71	P80	VCC ⁽⁴⁾	T7	-
I/O	-	-	P72	P81	Y8	W8	343 ⁽³⁾
I/O	-	-	P73	P82	U9	U8	346 ⁽³⁾
I/O	-	-	-	P84	Y9	W9	349 ⁽³⁾
I/O	-	-	-	P85	W10	V9	352 ⁽³⁾
I/O	P33	P50	P74	P86	V10	U9	355 ⁽³⁾
I/O	P34	P51	P75	P87	Y10	T9	358 ⁽³⁾
I/O	P35	P52	P76	P88	Y11	W10	361 ⁽³⁾
I/O (INIT)	P36	P53	P77	P89	W11	V10	364 ⁽³⁾
VCC	P37	P54	P78	P90	VCC ⁽⁴⁾	U10	-
GND	P38	P55	P79	P91	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P39	P56	P80	P92	V11	T10	367 ⁽³⁾
I/O	P40	P57	P81	P93	U11	R10	370 ⁽³⁾
I/O	P41	P58	P82	P94	Y12	W11	373 ⁽³⁾
I/O	P42	P59	P83	P95	W12	V11	376 ⁽³⁾
I/O	-	-	P84	P96	V12	U11	379 ⁽³⁾

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	P124	P144	M20	L19	493 ⁽³⁾
I/O	-	-	P125	P145	L19	L18	496 ⁽³⁾
I/O	P59	P86	P126	P146	L18	L17	499 ⁽³⁾
I/O	P60	P87	P127	P147	L20	L16	502 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	P88	P128	P148	K20	K19	505 ⁽³⁾
I/O	P62	P89	P129	P149	K19	K18	508 ⁽³⁾
VCC	P63	P90	P130	P150	VCC ⁽⁴⁾	K17	-
GND	P64	P91	P131	P151	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O (D3 ⁽²⁾)	P65	P92	P132	P152	K18	K16	511 ⁽³⁾
I/O	P66	P93	P133	P153	K17	K15	514 ⁽³⁾
I/O	P67	P94	P134	P154	J20	J19	517 ⁽³⁾
I/O	-	P95	P135	P155	J19	J18	520 ⁽³⁾
I/O	-	-	P136	P156	J18	J17	523 ⁽³⁾
I/O	-	-	P137	P157	J17	J16	526 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	P96	P138	P159	H19	H17	529 ⁽³⁾
I/O	P69	P97	P139	P160	H18	H16	532 ⁽³⁾
VCC	-	-	P140	P161	VCC ⁽⁴⁾	G19	-
I/O	-	P98	P141	P162	G19	G18	535 ⁽³⁾
I/O	-	P99	P142	P163	F20	G17	538 ⁽³⁾
I/O	-	-	-	P164	G18	G16	541 ⁽³⁾
I/O	-	-	-	P165	F19	F19	544 ⁽³⁾
GND	-	P100	P143	P166	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P167	F18	F18	547 ⁽³⁾
I/O	-	-	P144	P168	E19	F17	550 ⁽³⁾
I/O	-	-	P145	P169	D20	F16	553 ⁽³⁾
I/O	-	-	P146	P170	E18	F15	556 ⁽³⁾
I/O	-	-	P147	P171	D19	E19	559 ⁽³⁾
I/O	-	-	P148	P172	C20	E17	562 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	P101	P149	P173	E17	E16	565 ⁽³⁾
I/O	P71	P102	P150	P174	D18	D19	568 ⁽³⁾
I/O	-	P103	P151	P175	C19	C19	571 ⁽³⁾
I/O	-	P104	P152	P176	B20	B19	574 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	P105	P153	P177	C18	C18	577 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	P106	P154	P178	B19	B18	580 ⁽³⁾
CCLK	P74	P107	P155	P179	A20	A19	-
VCC	P75	P108	P156	P180	VCC ⁽⁴⁾	C17	-
O, TDO	P76	P109	P157	P181	A19	B17	0
GND	P77	P110	P158	P182	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P78	P111	P159	P183	B18	A18	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	P112	P160	P184	B17	A17	5
I/O	-	P113	P161	P185	C17	D16	8
I/O	-	P114	P162	P186	D16	C16	11
I/O (CS1 ⁽²⁾)	P80	P115	P163	P187	A18	B16	14
I/O	P81	P116	P164	P188	A17	A16	17
I/O	-	-	P165	P189	C16	D15	20

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	-	P190	B16	A15	23
I/O	-	P117	P166	P191	A16	E14	26
I/O	-	-	P167	P192	C15	C14	29
I/O	-	-	P168	P193	B15	B14	32
I/O	-	-	P169	P194	A15	D14	35
GND	-	P118	P170	P196	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P119	P171	P197	B14	A14	38
I/O	-	P120	P172	P198	A14	C13	41
I/O	-	-	-	P199	C13	B13	44
I/O	-	-	-	P200	B13	A13	47
VCC	-	-	P173	P201	VCC ⁽⁴⁾	D13	-
I/O	P82	P121	P174	P202	C12	B12	50
I/O	P83	P122	P175	P203	B12	D12	53
I/O	-	-	P176	P205	A12	A11	56
I/O	-	-	P177	P206	B11	B11	59
I/O	P84	P123	P178	P207	C11	C11	62
I/O	P85	P124	P179	P208	A11	D11	65
I/O	P86	P125	P180	P209	A10	A10	68
I/O	P87	P126	P181	P210	B10	B10	71
GND	P88	P127	P182	P211	GND ⁽⁴⁾	GND ⁽⁴⁾	-

2/8/00

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND⁽⁴⁾ or VCC⁽⁴⁾ are internally bonded to Ground or VCC planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)

Additional XCS30/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

2/12/98

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

GND Pins

A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

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CS280

VCC Pins					
A1	A7	C10	C17	D13	G1
G1	G19	K2	K17	M4	N16
T7	U3	U10	U17	W13	-
GND Pins					