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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	169
Number of Gates	40000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40-3pq208c

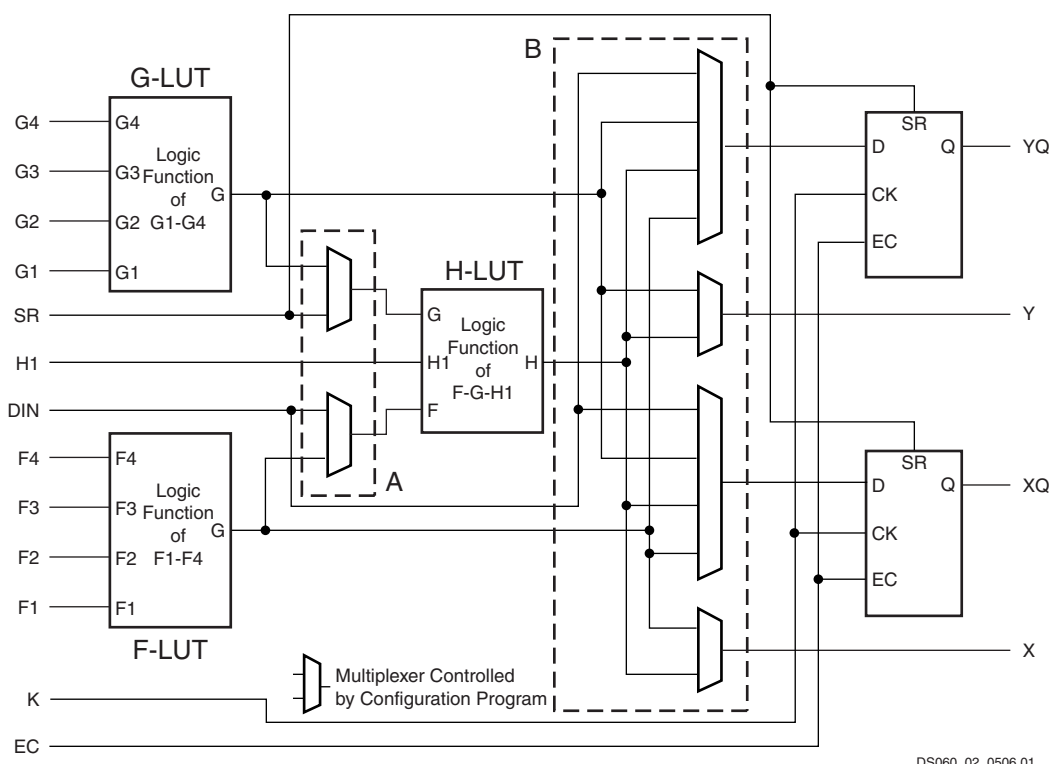


Figure 2: Spartan/XL Simplified CLB Logic Diagram (some features not shown)

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

Note: When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops


Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.


Latches (Spartan-XL Family Only)

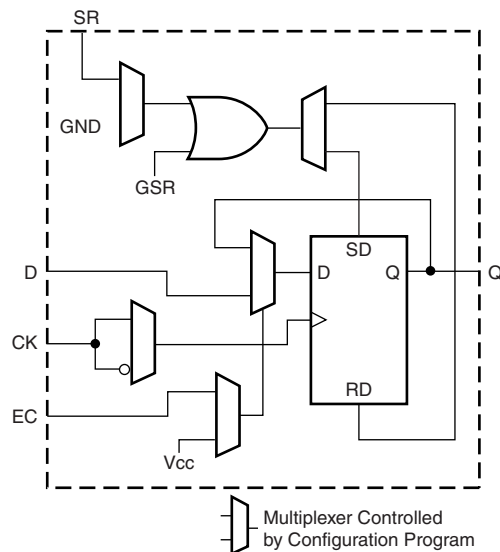
The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.

Table 2: CLB Storage Element Functionality

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
		1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (Spartan-XL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

- X Don't care
-  Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0* Input is Low or unconnected (default value)
- 1* Input is High or unconnected (default value)



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Figure 3: CLB Flip-Flop Functional Block Diagram

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

CLB Signal Flow Control

In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2, page 4) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinational CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinational output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1-C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

Table 4: Supported Sources for Spartan/XL Inputs

Source	Spartan Inputs		Spartan-XL Inputs
	5V, TTL	5V, CMOS	3.3V CMOS
Any device, $V_{CC} = 3.3V$, CMOS outputs	✓	Unreliable Data	✓
Spartan family, $V_{CC} = 5V$, TTL outputs	✓		✓
Any device, $V_{CC} = 5V$, TTL outputs ($V_{OH} \leq 3.7V$)	✓		✓
Any device, $V_{CC} = 5V$, CMOS outputs	✓	✓	✓ (default mode)

Table 5: I/O Standards Supported by Spartan-XL FPGAs

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}
LVC MOS 3V	OK	12/24 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}

Additional Fast Capture Input Latch (Spartan-XL Family Only)

The Spartan-XL family OB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active High input flip-flop. ILFLX is a transparent Low Fast Capture latch followed by a transparent High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 6.


Spartan-XL Family V_{CC} Clamping

Spartan-XL FPGAs have an optional clamping diode connected from each I/O to V_{CC} . When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. V_{CC} clamping is a global option affecting all I/O pins.


Spartan-XL devices are fully 5V TTL I/O compatible if V_{CC} clamping is not enabled. With V_{CC} clamping enabled, the Spartan-XL devices will begin to clamp input voltages to one diode voltage drop above V_{CC} . If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

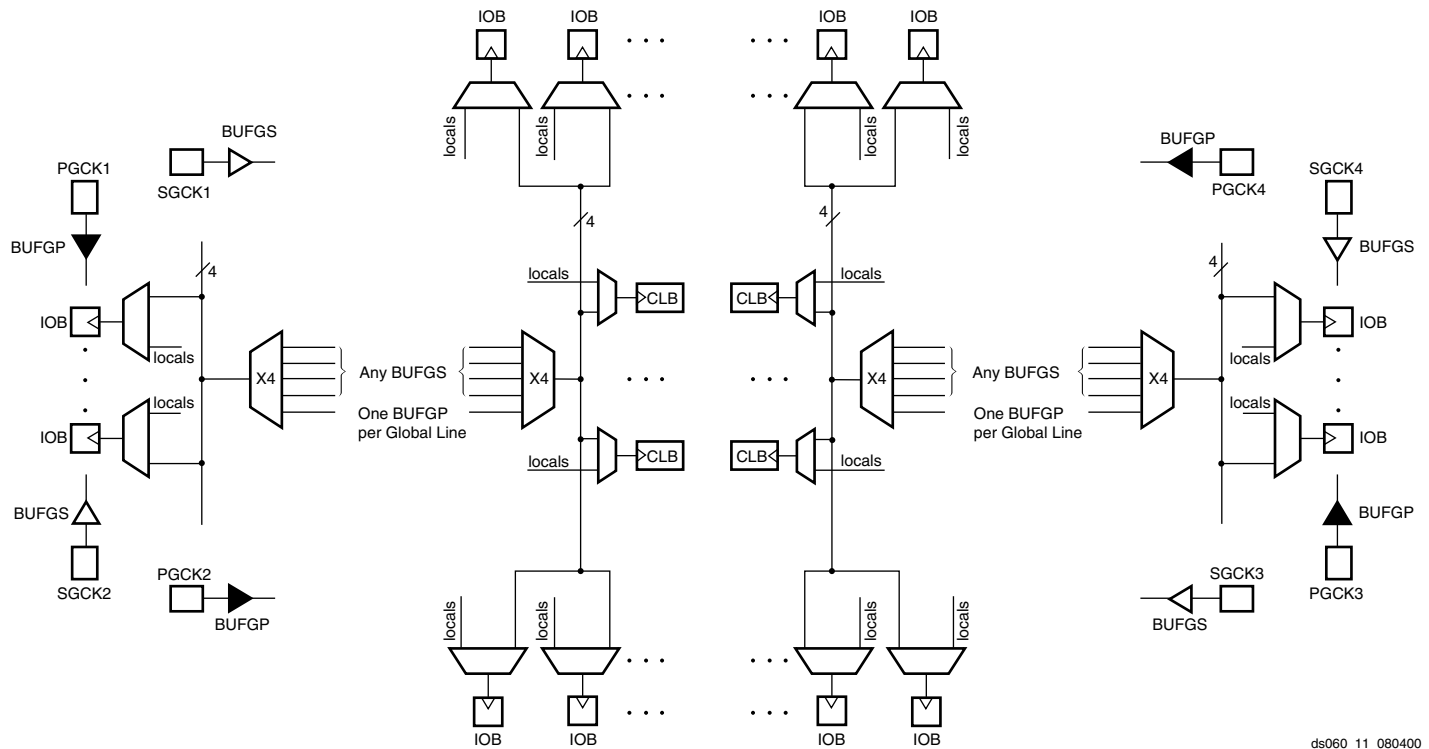
Spartan-XL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 5.

Table 6: Output Flip-Flop Functionality

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
		1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state



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Figure 11: 5V Spartan Family Global Net Distribution

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFPG (primary buffer), BUFSG (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 8. Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 8: CLB Memory Configurations

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√	—	—

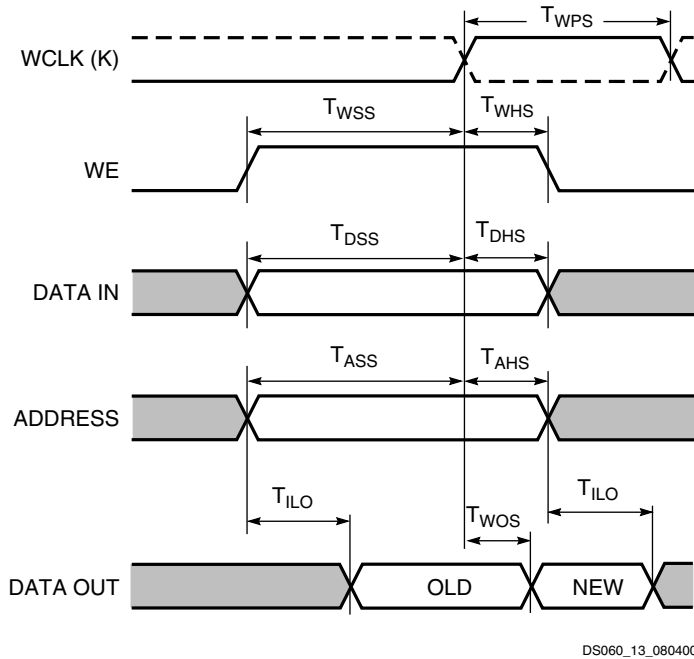


Figure 13: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be

inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO} , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS} , the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by $A[3:0]$ while the second provides only for read operations at the address specified independently by $DPRA[3:0]$. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the

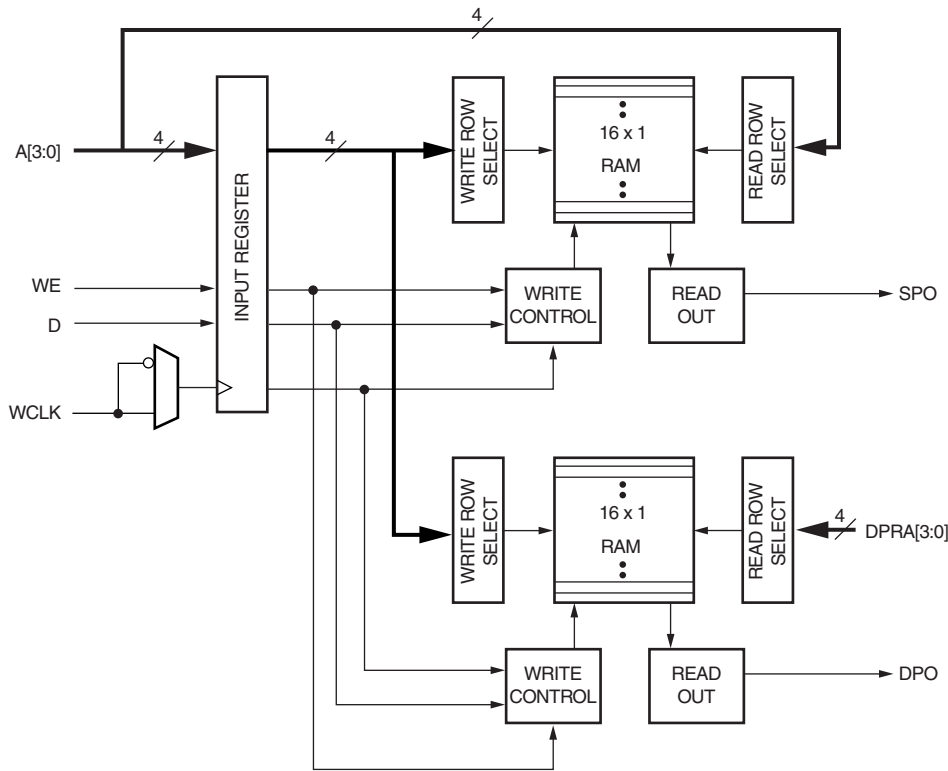


Figure 14: Logic Diagram for the Dual-Port RAM

CLB signals from which they are originally derived are shown in Table 10.

Table 10: Dual-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F _{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G _{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

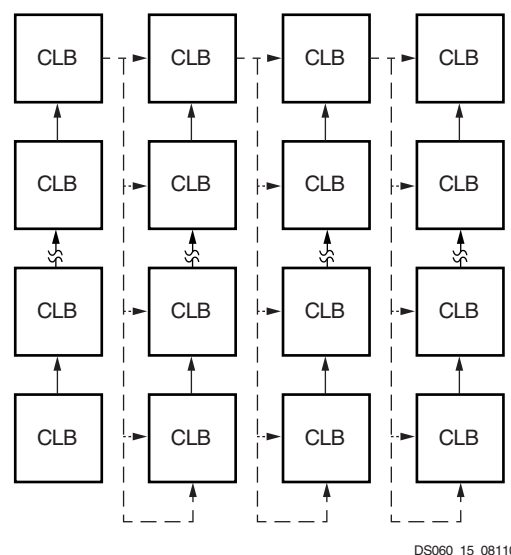
Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

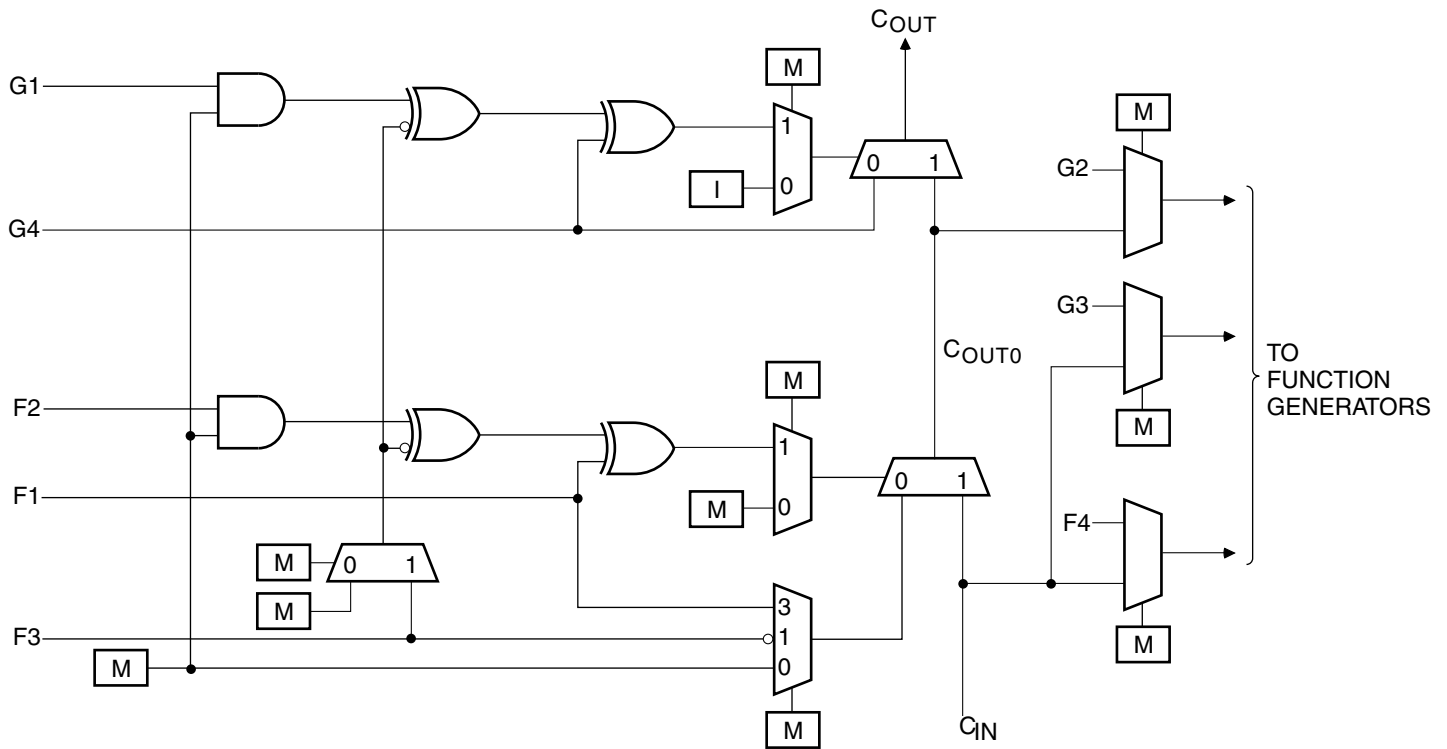
Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in micro-processor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan



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Figure 15: Available Spartan/XL Carry Propagation Paths



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Figure 17: Detail of Spartan/XL Dedicated Carry Logic

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

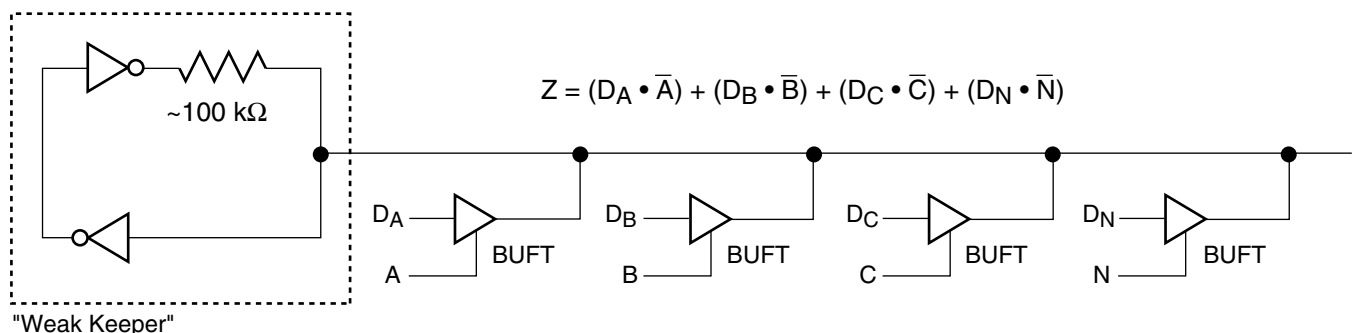
Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

Table 11: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN



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Figure 18: 3-state Buffers Implement a Multiplexer

Table 12: Boundary Scan Instructions

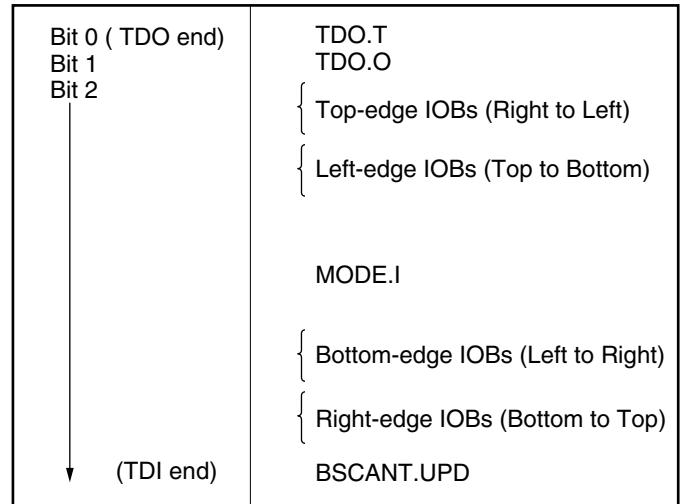
Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	IDCODE (Spartan-XL only)	IDCODE Register	-
1	1	1	BYPASS	Bypass Register	-

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-state. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contribute all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 21. The device-specific pinout tables for the Spartan/XL devices include the boundary scan locations for each IOB pin.



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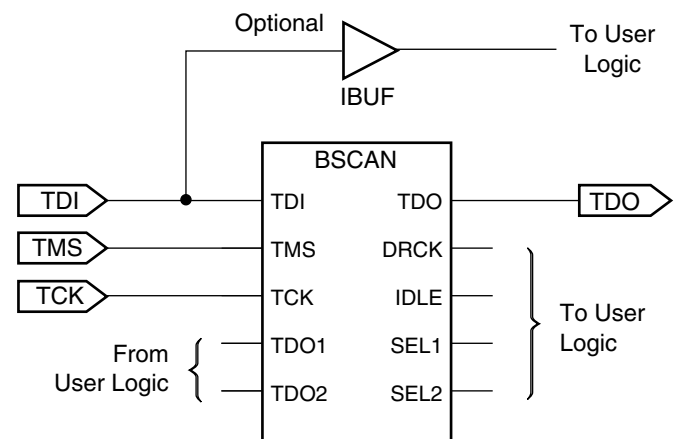
Figure 21: Boundary Scan Bit Sequence

BSDL (Boundary Scan Description Language) files for Spartan/XL devices are available on the Xilinx website in the File Download area. Note that the 5V Spartan devices and 3V Spartan-XL devices have different BSDL files.

Including Boundary Scan in a Design

If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 22.



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Figure 22: Boundary Scan Example

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

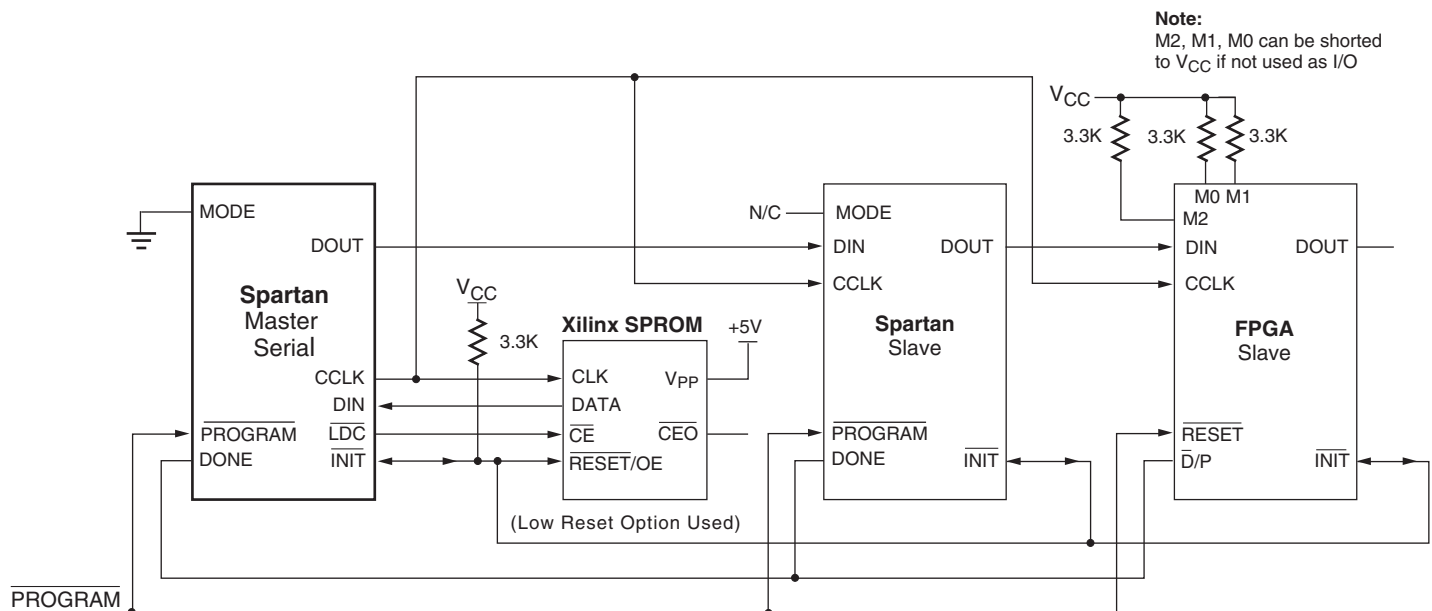
Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through

and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.



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Figure 25: Master/Slave Serial Mode Circuit Diagram

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be

met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in [Table 16](#) and [Table 17](#).

Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-4		-3		
		Min	Max	Min	Max	
Clocks						
T _{CH}	Clock High time	3.0	-	4.0	-	ns
T _{CL}	Clock Low time	3.0	-	4.0	-	ns
Combinatorial Delays						
T _{ILO}	F/G inputs to X/Y outputs	-	1.2	-	1.6	ns
T _{IHO}	F/G inputs via H to X/Y outputs	-	2.0	-	2.7	ns
T _{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.7	-	2.2	ns
CLB Fast Carry Logic						
T _{OPCY}	Operand inputs (F1, F2, G1, G4) to C _{OUT}	-	1.7	-	2.1	ns
T _{ASCY}	Add/Subtract input (F3) to C _{OUT}	-	2.8	-	3.7	ns
T _{INCY}	Initialization inputs (F1, F3) to C _{OUT}	-	1.2	-	1.4	ns
T _{SUM}	C _{IN} through function generators to X/Y outputs	-	2.0	-	2.6	ns
T _{BYP}	C _{IN} to C _{OUT} , bypass function generators	-	0.5	-	0.6	ns
Sequential Delays						
T _{CKO}	Clock K to Flip-Flop outputs Q	-	2.1	-	2.8	ns
Setup Time before Clock K						
T _{ICK}	F/G inputs	1.8	-	2.4	-	ns
T _{IHCK}	F/G inputs via H	2.9	-	3.9	-	ns
T _{HH1CK}	C inputs via H1 through H	2.3	-	3.3	-	ns
T _{DICK}	C inputs via DIN	1.3	-	2.0	-	ns
T _{ECKK}	C inputs via EC	2.0	-	2.6	-	ns
T _{RCK}	C inputs via S/R, going Low (inactive)	2.5	-	4.0	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T _{RPW}	Width (High)	3.0	-	4.0	-	ns
T _{RIO}	Delay from C inputs via S/R, going High to Q	-	3.0	-	4.0	ns
Global Set/Reset						
T _{MRW}	Minimum GSR pulse width	11.5	-	13.5	-	ns
T _{MRQ}	Delay from GSR input to any Q	See page 50 for T _{RRI} values per device.				
F _{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	166	-	125	MHz

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size ⁽¹⁾	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Write Operation							
T _{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T _{WCTS}		32x1	8.0	-	11.6	-	ns
T _{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T _{WPTS}		32x1	4.0	-	5.8	-	ns
T _{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T _{ASTS}		32x1	1.5	-	2.0	-	ns
T _{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{AHTS}		32x1	0.0	-	0.0	-	ns
T _{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T _{DSTS}		32x1	1.5	-	1.7	-	ns
T _{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{DHTS}		32x1	0.0	-	0.0	-	ns
T _{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T _{WSTS}		32x1	1.5	-	1.6	-	ns
T _{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{WHTS}		32x1	0.0	-	0.0	-	ns
T _{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T _{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T _{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T _{RCT}		32x1	3.8	-	3.8	-	ns
T _{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T _{IHO}		32x1	-	2.0	-	2.7	ns
T _{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T _{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Min	Min	
Input Setup/Hold Times Using Primary Clock and IFF					
T _{PSUF} /T _{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T _{PSU} /T _{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T _{SSUF} /T _{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T _{SSU} /T _{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:

1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Setup Times - TTL Inputs ⁽¹⁾							
T _{ECIK}	Clock Enable (EC) to Clock (IK), no delay	All devices	1.6	-	2.1	-	ns
T _{PICK}	Pad to Clock (IK), no delay	All devices	1.5	-	2.0	-	ns
Hold Times							
T _{IKEC}	Clock Enable (EC) to Clock (IK), no delay	All devices	0.0	-	0.9	-	ns
	All Other Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays - TTL Inputs ⁽¹⁾							
T _{PID}	Pad to I1, I2	All devices	-	1.5	-	2.0	ns
T _{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.8	-	3.6	ns
T _{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	2.7	-	2.8	ns
T _{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	3.2	-	3.9	ns
Delay Adder for Input with Delay Option							
T _{Delay}	T _{ECIKD} = T _{ECIK} + T _{Delay} T _{PICKD} = T _{PICK} + T _{Delay} T _{PDLI} = T _{PLI} + T _{Delay}	XCS05	3.6	-	4.0	-	ns
		XCS10	3.7	-	4.1	-	ns
		XCS20	3.8	-	4.2	-	ns
		XCS30	4.5	-	5.0	-	ns
		XCS40	5.5	-	5.5	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	11.5	-	13.5	-	ns
T _{RRI}	Delay from GSR input to any Q	XCS05	-	9.0	-	11.3	ns
		XCS10	-	9.5	-	11.9	ns
		XCS20	-	10.0	-	12.5	ns
		XCS30	-	10.5	-	13.1	ns
		XCS40	-	11.0	-	13.8	ns

Notes:

1. Delay adder for CMOS Inputs option: for -3 speed grade, add 0.4 ns; for -4 speed grade, add 0.2 ns.
2. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
3. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For

more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
T_{GLS}	From pad through buffer, to any clock K	XCS05XL	1.4	1.5	ns
		XCS10XL	1.7	1.8	ns
		XCS20XL	2.0	2.1	ns
		XCS30XL	2.3	2.5	ns
		XCS40XL	2.6	2.8	ns

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84 ⁽⁴⁾	VQ100	CS144 ^(2,4)	TQ144	Bndry Scan
I/O	P80	P81	A10	P116	17
GND	-	-	C9	P118	-
I/O	-	-	B9	P119	20
I/O	-	-	A9	P120	23
I/O	P81	P82	D8	P121	26
I/O	P82	P83	C8	P122	29
I/O	-	P84	B8	P123	32
I/O	-	P85	A8	P124	35
I/O	P83	P86	B7	P125	38
I/O	P84	P87	A7	P126	41
GND	P1	P88	C7	P127	-

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS10XL is not part of the Boundary Scan chain. For the XCS10XL, subtract 1 from all Boundary Scan numbers from GCK3 on (175 and higher).
4. PC84 and CS144 packages discontinued by [PDN2004-01](#)

Additional XCS10/XL Package Pins

TQ144					
Not Connected Pins					
P117	-	-	-	-	-
5/5/97					

CS144					
Not Connected Pins					
D9	-	-	-	-	-
4/28/99					

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
VCC	P89	D7	P128	P183	-
I/O	P90	A6	P129	P184	62
I/O	P91	B6	P130	P185	65
I/O	P92	C6	P131	P186	68
I/O	P93	D6	P132	P187	71
I/O	-	-	-	P188	74
I/O	-	-	-	P189	77
I/O	P94	A5	P133	P190	80
I/O	P95	B5	P134	P191	83
VCC ⁽²⁾	-	-	-	P192	-
I/O	-	C5	P135	P193	86
I/O	-	D5	P136	P194	89
GND	-	A4	P137	P195	-
I/O	-	-	-	P196	92
I/O	-	-	-	P197	95
I/O	-	-	-	P198	98
I/O	-	-	-	P199	101
I/O	P96	B4	P138	P200	104
I/O	P97	C4	P139	P201	107
I/O	-	A3	P140	P204	110
I/O	-	B3	P141	P205	113
I/O	P98	C3	P142	P206	116

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P99	A2	P143	P207	119
VCC	P100	B2	P144	P208	-
GND	P1	A1	P1	P1	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	B1	P2	P2	122
I/O	P3	C2	P3	P3	125
I/O	-	C1	P4	P4	128
I/O	-	D4	P5	P5	131
I/O, TDI	P4	D3	P6	P6	134
I/O, TCK	P5	D2	P7	P7	137
I/O	-	-	-	P8	140
I/O	-	-	-	P9	143
I/O	-	-	-	P10	146
I/O	-	-	-	P11	149
GND	-	D1	P8	P13	-
I/O	-	E4	P9	P14	152
I/O	-	E3	P10	P15	155
I/O, TMS	P6	E2	P11	P16	158
I/O	P7	E1	P12	P17	161
VCC ⁽²⁾	-	-	-	P18	-
I/O	-	-	-	P19	164
I/O	-	-	-	P20	167

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC ⁽²⁾	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P21	L2	P33	P49	239
Not Connected ⁽¹⁾ M1 ⁽²⁾	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected ⁽¹⁾ PWRDWN ⁽²⁾	P26	N2	P38	P54	246 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P27	M3	P39	P55	247 ⁽³⁾
I/O (HDC)	P28	N3	P40	P56	250 ⁽³⁾
I/O	-	K4	P41	P57	253 ⁽³⁾
I/O	-	L4	P42	P58	256 ⁽³⁾
I/O	P29	M4	P43	P59	259 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O (LDC)	P30	N4	P44	P60	262 ⁽³⁾
I/O	-	-	-	P61	265 ⁽³⁾
I/O	-	-	-	P62	268 ⁽³⁾
I/O	-	-	-	P63	271 ⁽³⁾
I/O	-	-	-	P64	274 ⁽³⁾
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 ⁽³⁾
I/O	-	M5	P47	P68	280 ⁽³⁾
I/O	P31	N5	P48	P69	283 ⁽³⁾
I/O	P32	K6	P49	P70	286 ⁽³⁾
VCC ⁽²⁾	-	-	-	P71	-
I/O	-	-	-	P72	289 ⁽³⁾
I/O	-	-	-	P73	292 ⁽³⁾
I/O	P33	L6	P50	P74	295 ⁽³⁾
I/O	P34	M6	P51	P75	298 ⁽³⁾
I/O	P35	N6	P52	P76	301 ⁽³⁾
I/O (INIT)	P36	M7	P53	P77	304 ⁽³⁾
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 ⁽³⁾
I/O	P40	N8	P57	P81	310 ⁽³⁾
I/O	P41	M8	P58	P82	313 ⁽³⁾
I/O	P42	L8	P59	P83	316 ⁽³⁾
I/O	-	-	-	P84	319 ⁽³⁾
I/O	-	-	-	P85	322 ⁽³⁾
VCC ⁽²⁾	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 ⁽³⁾
I/O	P44	N9	P61	P88	328 ⁽³⁾
I/O	-	M9	P62	P89	331 ⁽³⁾
I/O	-	L9	P63	P90	334 ⁽³⁾
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 ⁽³⁾
I/O	-	-	-	P94	340 ⁽³⁾
I/O	-	-	-	P95	343 ⁽³⁾
I/O	-	-	-	P96	346 ⁽³⁾
I/O	P45	N10	P65	P97	349 ⁽³⁾
I/O	P46	M10	P66	P98	352 ⁽³⁾
I/O	-	L10	P67	P99	355 ⁽³⁾
I/O	-	N11	P68	P100	358 ⁽³⁾
I/O	P47	M11	P69	P101	361 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P48	L11	P70	P102	364 ⁽³⁾
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7 ⁽²⁾)	P53	L12	P75	P107	367 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P54	L13	P76	P108	370 ⁽³⁾
I/O	-	K10	P77	P109	373 ⁽³⁾
I/O	-	K11	P78	P110	376 ⁽³⁾
I/O (D6 ⁽²⁾)	P55	K12	P79	P112	379 ⁽³⁾
I/O	P56	K13	P80	P113	382 ⁽³⁾
I/O	-	-	-	P114	385 ⁽³⁾
I/O	-	-	-	P115	388 ⁽³⁾
I/O	-	-	-	P116	391 ⁽³⁾
I/O	-	-	-	P117	394 ⁽³⁾
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 ⁽³⁾
I/O	-	J12	P83	P120	400 ⁽³⁾
VCC ⁽²⁾	-	-	-	P121	-
I/O (D5 ⁽²⁾)	P57	J13	P84	P122	403 ⁽³⁾
I/O	P58	H10	P85	P123	406 ⁽³⁾
I/O	-	-	-	P124	409 ⁽³⁾
I/O	-	-	-	P125	412 ⁽³⁾
I/O	P59	H11	P86	P126	415 ⁽³⁾
I/O	P60	H12	P87	P127	418 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	H13	P88	P128	421 ⁽³⁾
I/O	P62	G12	P89	P129	424 ⁽³⁾
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3 ⁽²⁾)	P65	G10	P92	P132	427 ⁽³⁾
I/O	P66	F13	P93	P133	430 ⁽³⁾
I/O	P67	F12	P94	P134	433 ⁽³⁾
I/O	-	F11	P95	P135	436 ⁽³⁾
I/O	-	-	-	P136	439 ⁽³⁾
I/O	-	-	-	P137	442 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	F10	P96	P138	445 ⁽³⁾
I/O	P69	E13	P97	P139	448 ⁽³⁾
VCC ⁽²⁾	-	-	-	P140	-
I/O	-	E12	P98	P141	451 ⁽³⁾
I/O	-	E11	P99	P142	454 ⁽³⁾
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 ⁽³⁾
I/O	-	-	-	P146	460 ⁽³⁾
I/O	-	-	-	P147	463 ⁽³⁾
I/O	-	-	-	P148	466 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	D13	P101	P149	469 ⁽³⁾
I/O	P71	D12	P102	P150	472 ⁽³⁾
I/O	-	D11	P103	P151	475 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	C12	P105	P153	481 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	C11	P106	P154	484 ⁽³⁾
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1 ⁽²⁾)	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC ⁽²⁾	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

2/8/00

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	P5	P5	P5	D3	C1	155
I/O, TDI	P4	P6	P6	P6	E4	D4	158
I/O, TCK	P5	P7	P7	P7	C1	D3	161
I/O	-	-	P8	P8	D1	E2	164
I/O	-	-	P9	P9	E3	E4	167
I/O	-	-	P10	P10	E2	E1	170
I/O	-	-	P11	P11	E1	F5	173
I/O	-	-	P12	P12	F3	F3	176
I/O	-	-	-	P13	F2	F2	179
GND	-	P8	P13	P14	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P9	P14	P15	G3	F4	182
I/O	-	P10	P15	P16	G2	F1	185
I/O, TMS	P6	P11	P16	P17	G1	G3	188
I/O	P7	P12	P17	P18	H3	G2	191
VCC	-	-	P18	P19	VCC ⁽⁴⁾	G1	-
I/O	-	-	-	P20	H2	G4	194
I/O	-	-	-	P21	H1	H1	197
I/O	-	-	P19	P23	J2	H4	200
I/O	-	-	P20	P24	J1	J1	203
I/O	-	P13	P21	P25	K2	J2	206
I/O	P8	P14	P22	P26	K3	J3	209
I/O	P9	P15	P23	P27	K1	J4	212
I/O	P10	P16	P24	P28	L1	K1	215
GND	P11	P17	P25	P29	GND ⁽⁴⁾	GND ⁽⁴⁾	-
VCC	P12	P18	P26	P30	VCC ⁽⁴⁾	K2	-
I/O	P13	P19	P27	P31	L2	K3	218
I/O	P14	P20	P28	P32	L3	K4	221
I/O	P15	P21	P29	P33	L4	K5	224
I/O	-	P22	P30	P34	M1	L1	227
I/O	-	-	P31	P35	M2	L2	230
I/O	-	-	P32	P36	M3	L3	233
I/O	-	-	-	P38	N1	M2	236
I/O	-	-	-	P39	N2	M3	239
VCC	-	-	P33	P40	VCC ⁽⁴⁾	M4	-
I/O	P16	P23	P34	P41	P1	N1	242
I/O	P17	P24	P35	P42	P2	N2	245
I/O	-	P25	P36	P43	R1	N3	248
I/O	-	P26	P37	P44	P3	N4	251
GND	-	P27	P38	P45	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P46	T1	P1	254
I/O	-	-	P39	P47	R3	P2	257
I/O	-	-	P40	P48	T2	P3	260
I/O	-	-	P41	P49	U1	P4	263
I/O	-	-	P42	P50	T3	P5	266
I/O	-	-	P43	P51	U2	R1	269

CS280

VCC Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-
Not Connected Pins					
A4	A12	C8	C12	C15	D1
D2	D5	D8	D17	D18	E15
H2	H3	H18	H19	L4	M1
M16	M18	R2	R4	R5	R15
R17	T8	T15	U5	V8	V12
W12	W16	-	-	-	-
Not Connected Pins (VCC in XCS40XL)					
B5	B15	E3	E18	R3	R18
V5	V15	-	-	-	-

5/21/02

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
VCC	P183	P212	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P184	P213	C10	D10	86
I/O	P185	P214	D10	E10	89
I/O	P186	P215	A9	A9	92
I/O	P187	P216	B9	B9	95
I/O	P188	P217	C9	C9	98
I/O	P189	P218	D9	D9	101
I/O	P190	P220	A8	A8	104
I/O	P191	P221	B8	B8	107
I/O	-	-	C8	C8	110
I/O	-	-	A7	D8	113
VCC	P192	P222	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	P223	A6	B7	116
I/O	-	P224	C7	C7	119
I/O	P193	P225	B6	D7	122
I/O	P194	P226	A5	A6	125
GND	P195	P227	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P196	P228	C6	B6	128
I/O	P197	P229	B5	C6	131
I/O	P198	P230	A4	D6	134
I/O	P199	P231	C5	E6	137

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
I/O	P200	P232	B4	A5	140
I/O	P201	P233	A3	C5	143
I/O	-	-	-	D5	146
I/O	-	-	-	A4	149
I/O	P202	P234	D5	B4	152
I/O	P203	P235	C4	C4	155
I/O	P204	P236	B3	A3	158
I/O	P205	P237	B2	A2	161
I/O	P206	P238	A2	B3	164
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P207	P239	C3	B2	167
VCC	P208	P240	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
GND	P1	P1	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	P2	B1	C3	170
I/O	P3	P3	C2	C2	173
I/O	P4	P4	D2	B1	176
I/O	P5	P5	D3	C1	179
I/O, TDI	P6	P6	E4	D4	182
I/O, TCK	P7	P7	C1	D3	185
I/O	-	-	-	D2	188
I/O	-	-	-	D1	191
I/O	P8	P8	D1	E2	194
I/O	P9	P9	E3	E4	197
I/O	P10	P10	E2	E1	200
I/O	P11	P11	E1	F5	203
I/O	P12	P12	F3	F3	206
I/O	-	P13	F2	F2	209
GND	P13	P14	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P14	P15	G3	F4	212
I/O	P15	P16	G2	F1	215
I/O, TMS	P16	P17	G1	G3	218
I/O	P17	P18	H3	G2	221
VCC	P18	P19	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	P20	H2	G4	224
I/O	-	P21	H1	H1	227
I/O	-	-	J4	H3	230
I/O	-	-	J3	H2	233
I/O	P19	P23	J2	H4	236
I/O	P20	P24	J1	J1	239
I/O	P21	P25	K2	J2	242
I/O	P22	P26	K3	J3	245
I/O	P23	P27	K1	J4	248
I/O	P24	P28	L1	K1	251