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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	192
Number of Gates	40000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40-3pq240c

Table 4: **Supported Sources for Spartan/XL Inputs**

Source	Spartan Inputs		Spartan-XL Inputs
	5V, TTL	5V, CMOS	3.3V CMOS
Any device, V_{CC} = 3.3V, CMOS outputs	√	Unreliable Data	√
Spartan family, V_{CC} = 5V, TTL outputs	√		√
Any device, V_{CC} = 5V, TTL outputs ($V_{OH} \leq 3.7V$)	√		√
Any device, V_{CC} = 5V, CMOS outputs	√	√	√ (default mode)

Spartan-XL Family V_{CC} Clamping

Spartan-XL FPGAs have an optional clamping diode connected from each I/O to V_{CC}. When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. V_{CC} clamping is a global option affecting all I/O pins.

Spartan-XL devices are fully 5V TTL I/O compatible if V_{CC} clamping is not enabled. With V_{CC} clamping enabled, the Spartan-XL devices will begin to clamp input voltages to one diode voltage drop above V_{CC}. If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

Spartan-XL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 5.

Table 5: **I/O Standards Supported by Spartan-XL FPGAs**

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}
LVCMOS 3V	OK	12/24 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}

Additional Fast Capture Input Latch (Spartan-XL Family Only)

The Spartan-XL family OB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active High input flip-flop. ILFLX is a transparent Low Fast Capture latch followed by a transparent High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 6.

Table 6: **Output Flip-Flop Functionality**

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	⌐	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
⌐	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

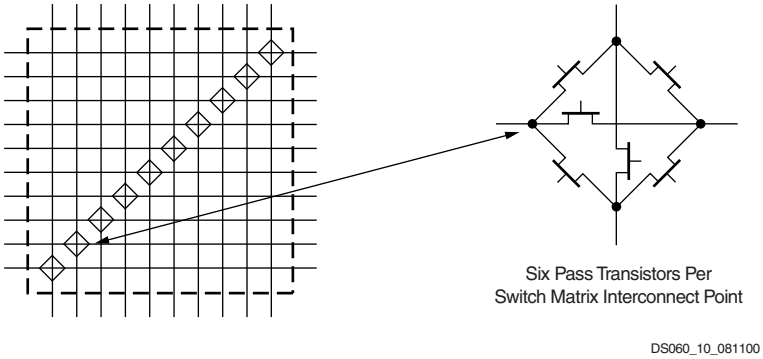


Figure 10: **Programmable Switch Matrix**

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 8).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 8. The longlines also interface to some 3-state buffers which is described later in **3-State Long Line Drivers**, page 19.

I/O Routing

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 11. In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.

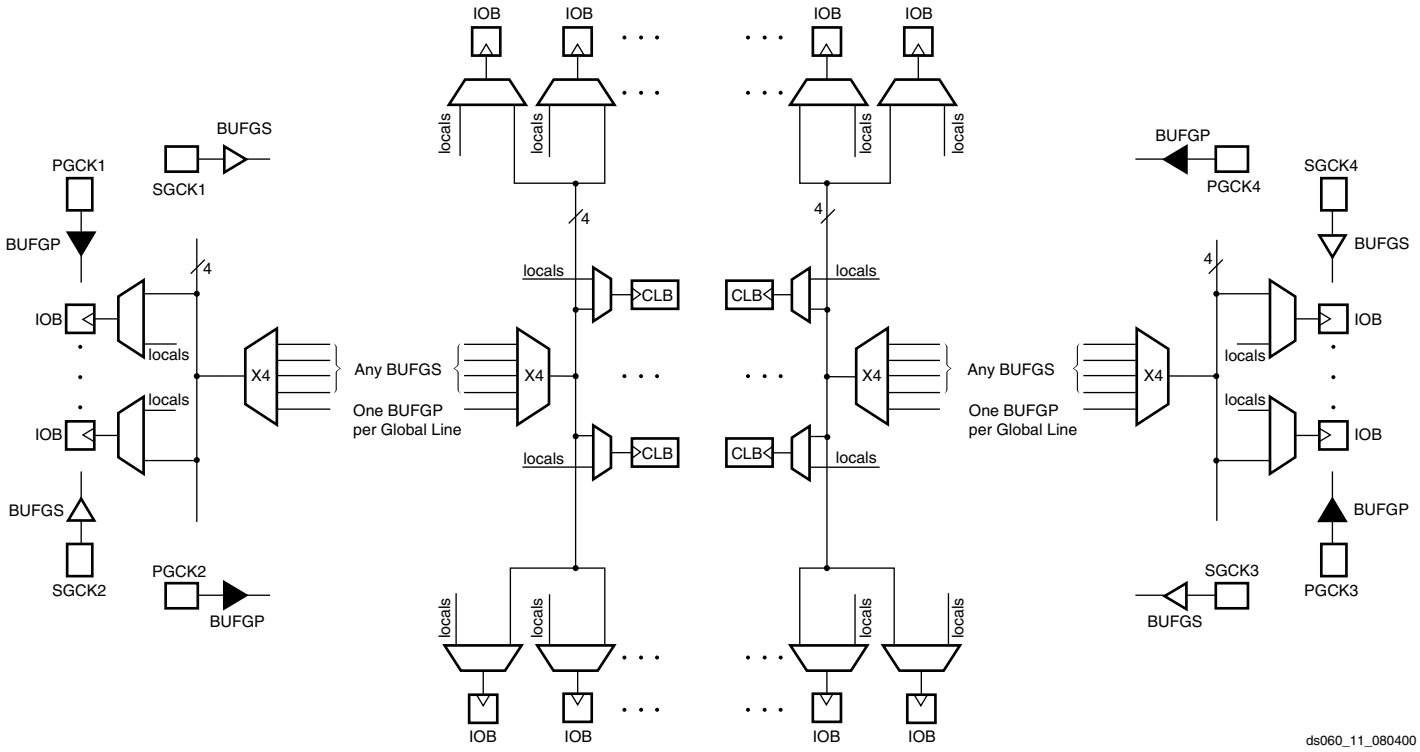


Figure 11: **5V Spartan Family Global Net Distribution**

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL family global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 8. Any of these possibilities can be individually programmed into a Spartan/XL FPGA CLB.

Table 8: **CLB Memory Configurations**

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√	–	–

CLB signals from which they are originally derived are shown in Table 10.

Table 10: **Dual-Port RAM Signals**

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F_{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G_{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: *"Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM,"* and *"Synchronous and Asynchronous FIFO Designs."* All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan

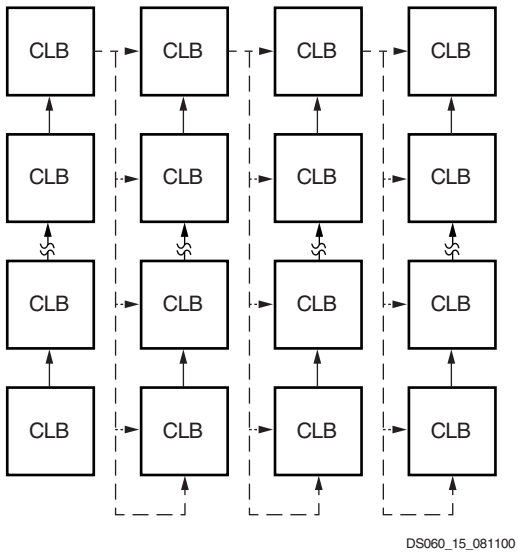


Figure 15: **Available Spartan/XL Carry Propagation Paths**

and Spartan-XL families, speeding up arithmetic and counting functions.

The carry chain in 5V Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in Spartan-XL devices can only run up the column, providing even higher speed.

Figure 16, page 18 shows a Spartan/XL FPGA CLB with dedicated fast carry logic. The carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 17, page 19 shows the details of the Spartan/XL FPGA carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 16.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

On-Chip Oscillator

Spartan/XL devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, V_{CC}, and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8-MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in Figure 3, page 5 for the CLB and Figure 5, page 6 for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 19.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

Global 3-State

A separate Global 3-state line (GTS) as shown in Figure 6, page 7 forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in Figure 19 for GSR except the IBUF would be connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-state signal. Alternatively, GTS can be driven from any internal node.

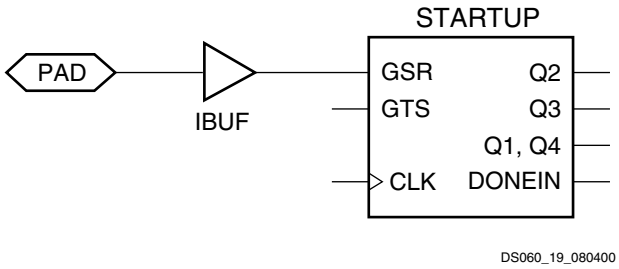


Figure 19: **Symbols for Global Set/Reset**

Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan compatible device. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan and Spartan-XL families implement IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Spartan/XL devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "*Boundary Scan in FPGA Devices*."

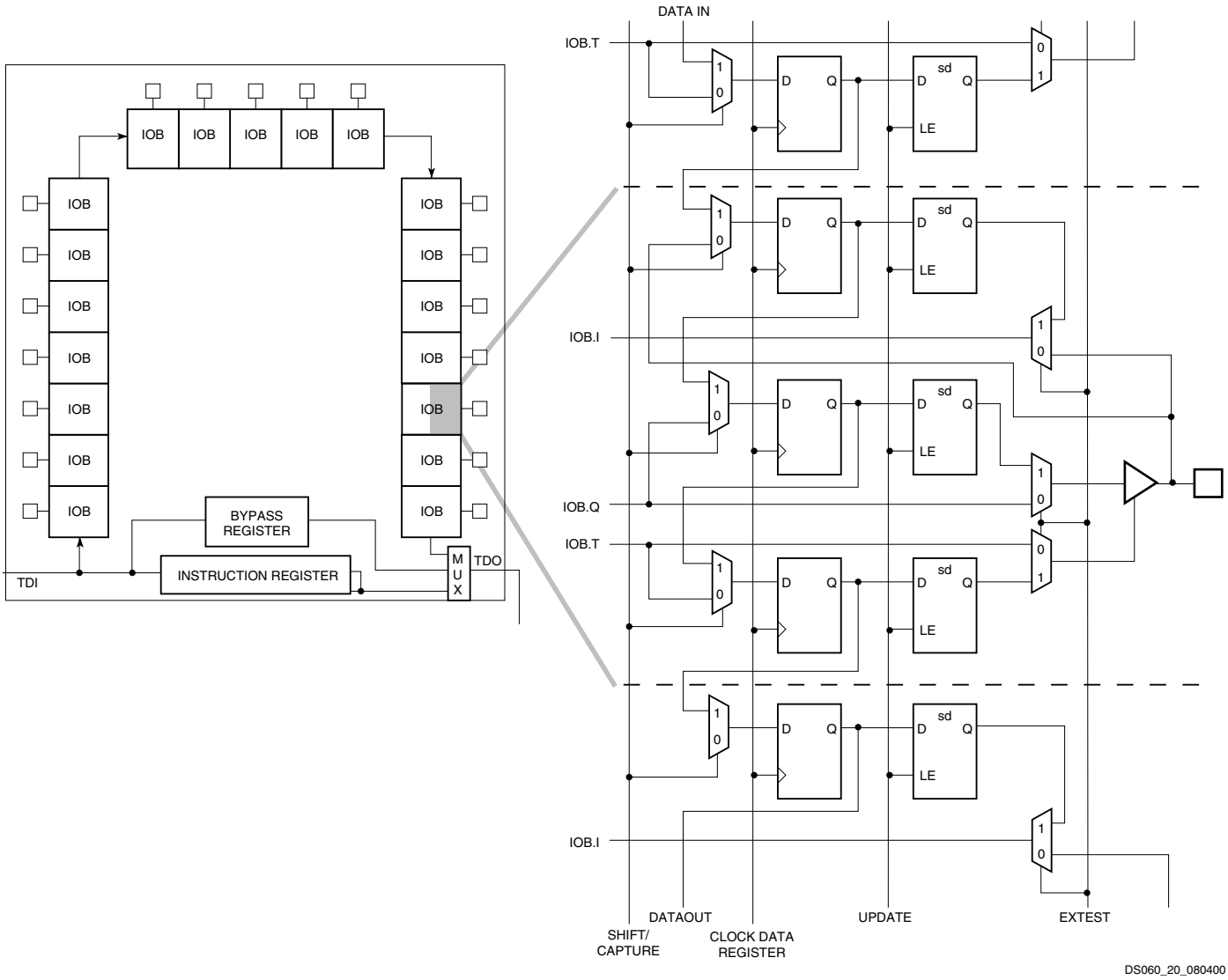


Figure 20: **Spartan/XL Boundary Scan Logic**

Even if the boundary scan symbol is used in a design, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state.
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "*Boundary Scan in FPGA Devices*. "

Boundary Scan Enhancements (Spartan-XL Family Only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

IDCODE: The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

c = the company code (49h for Xilinx)

a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)

f = the family code (02h for Spartan-XL family)

v = the die version number

Table 13: **IDCODEs Assigned to Spartan-XL FPGAs**

FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

Configuration State: The configuration state is available to JTAG controllers.

Configuration Disable: The JTAG port can be prevented from configuring the FPGA.

TCK Startup: TCK can now be used to clock the start-up block in addition to other user clocks.

CCLK Holdoff: Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

Reissue Configure: The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

Bypass FF: Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

Power-Down (Spartan-XL Family Only)

All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low power-down pin ($\overline{\text{PWRDWN}}$) to reduce supply current to 100 µA typical. The $\overline{\text{PWRDWN}}$ pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The $\overline{\text{PWRDWN}}$ pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

V_{CC} must continue to be supplied during Power-down, and configuration data is maintained. When the $\overline{\text{PWRDWN}}$ pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The $\overline{\text{PROGRAM}}$ pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

$\overline{\text{PWRDWN}}$ has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before $\overline{\text{PWRDWN}}$ to affect the order of events. When the $\overline{\text{PWRDWN}}$ signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of $\overline{\text{PWRDWN}}$ before using the device.

figuration are shown in Table 14 and Table 15.

Table 14: **Pin Functions During Configuration (Spartan Family Only)**

Configuration Mode (MODE Pin)		User Operation
Slave Serial (High)	**Master Serial (Low)**	
MODE (I)	MODE (I)	MODE
HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

Notes:
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Table 15: **Pin Functions During Configuration (Spartan-XL Family Only)**

CONFIGURATION MODE <M1:M0>			User Operation
Slave Serial [1:1]	**Master Serial [1:0]**	**Express [0:X]**	
M1 (High) (I)	M1 (High) (I)	M1(Low) (I)	M1
M0 (High) (I)	M0 (Low) (I)	M0 (I)	M0
HDC (High)	HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

Notes:
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is –50% to +25%.

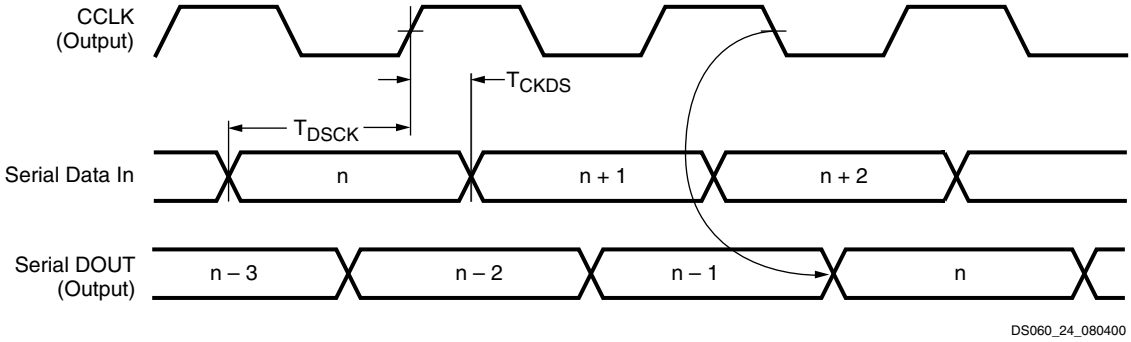
In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in Figure 24.

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Earlier families such as the XC3000 series do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

Figure 25 shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Symbol	Description	Min	Units
CCLK	T_{DSCK}	DIN setup	20	ns
	T_{CKDS}	DIN hold	0	ns

Notes:
1. At power-up, V_{CC} must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling $\overline{PROGRAM}$ Low until V_{CC} is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 24: **Master Serial Mode Programming Switching Characteristics**

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 25 shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.

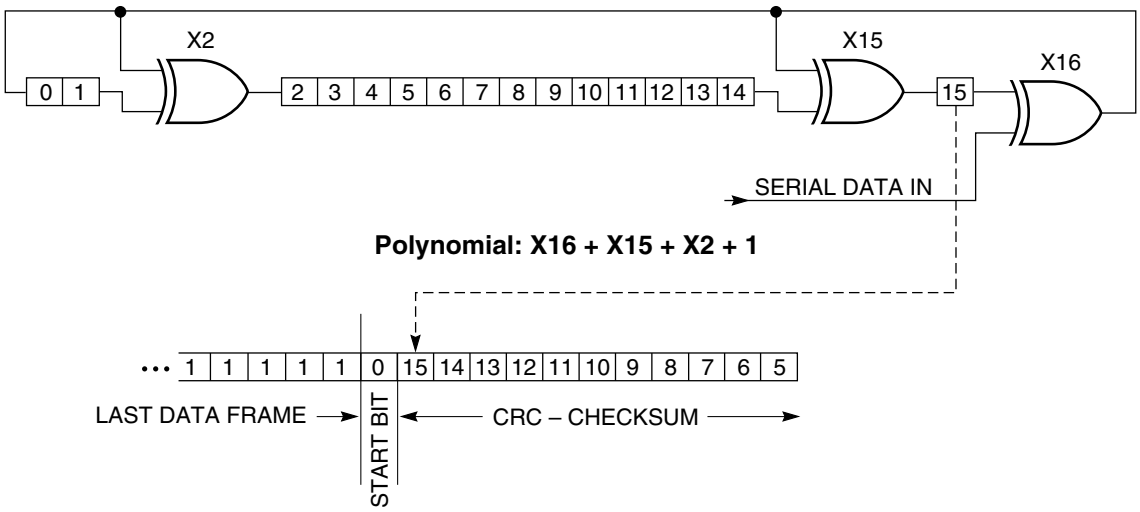


Figure 29: **Circuit for Generating CRC-16**

Configuration Sequence

There are four major steps in the Spartan/XL FPGA power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC}. When all $\overline{INIT}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{INIT}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{LDC}$, $\overline{INIT}$ and DONE provide status outputs for the system interface. The outputs $\overline{LDC}$, $\overline{INIT}$ and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain $\overline{INIT}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive $\overline{INIT}$. Two internal clocks after the $\overline{INIT}$ pin is recognized as High, the device samples the MODE pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 16 and Table 17.

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.

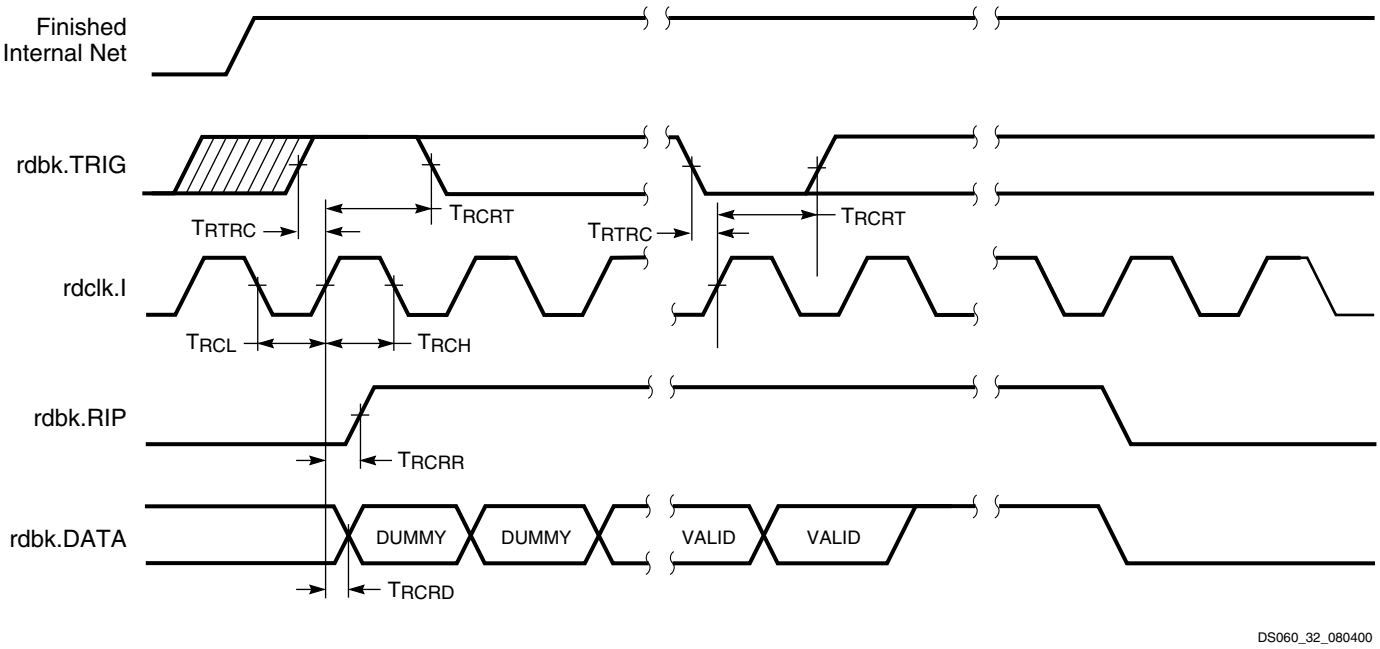


Figure 33: **Spartan and Spartan-XL Readback Timing Diagram**

Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:
1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

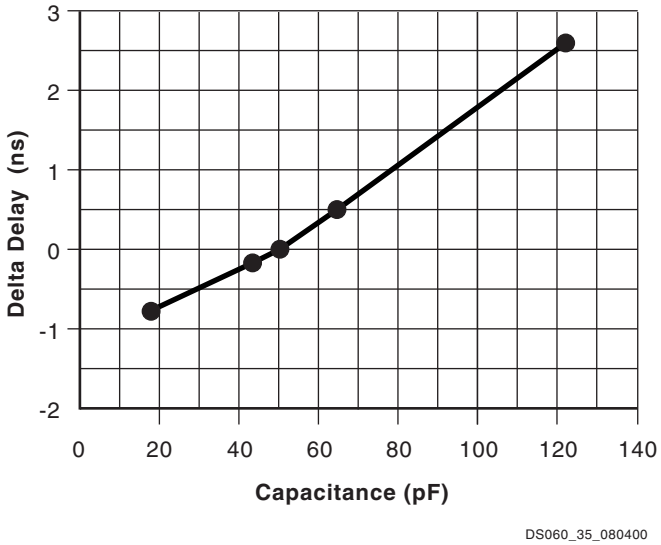


Figure 34: **Delay Factor at Various Capacitive Loads**

Spartan Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Clocks							
T_{CH}	Clock High	All devices	3.0	-	4.0	-	ns
T_{CL}	Clock Low	All devices	3.0	-	4.0	-	ns
Propagation Delays - TTL Outputs(1,2)							
T_{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.3	-	4.5	ns
T_{OKPOS}	Clock (OK to Pad, slew-rate limited	All devices	-	6.9	-	7.0	ns
T_{OPF}	Output (O) to Pad, fast	All devices	-	3.6	-	4.8	ns
T_{OPS}	Output (O) to Pad, slew-rate limited	All devices	-	7.2	-	7.3	ns
T_{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	3.0	-	3.8	ns
T_{TSONF}	3-state to Pad active and valid, fast	All devices	-	6.0	-	7.3	ns
T_{TSONS}	3-state to Pad active and valid, slew-rate limited	All devices	-	9.6	-	9.8	ns
Setup and Hold Times							
T_{OOK}	Output (O) to clock (OK) setup time	All devices	2.5	-	3.8	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T_{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	2.0	-	2.7	-	ns
T_{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.0	-	0.5	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	11.5		13.5		ns
T_{RPO}	Delay from GSR input to any Pad	XCS05	-	12.0	-	15.0	ns
		XCS10	-	12.5	-	15.7	ns
		XCS20	-	13.0	-	16.2	ns
		XCS30	-	13.5	-	16.9	ns
		XCS40	-	14.0	-	17.5	ns

Notes:

1. Delay adder for CMOS Outputs option (with fast slew rate option): for -3 speed grade, add 1.0 ns; for -4 speed grade, add 0.8 ns.
2. Delay adder for CMOS Outputs option (with slow slew rate option): for -3 speed grade, add 2.0 ns; for -4 speed grade, add 1.5 ns.
3. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
4. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings(1)

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked(2, 3)	–0.5 to 5.5	V
		Not 5V Tolerant I/Os(4, 5)	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked(2, 3)	–0.5 to 5.5	V
		Not 5V Tolerant I/Os(4, 5)	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
5. Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0V or overshoot to V_{CC} + 2.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C(1)	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage(2)		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage(2)		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold is ~50% of V_{CC}.

Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Propagation Delays							
T_{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.2	-	3.7	ns
T_{OPF}	Output (O) to Pad, fast	All devices	-	2.5	-	2.9	ns
T_{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	2.8	-	3.3	ns
T_{TSONF}	3-state to Pad active and valid, fast	All devices	-	2.6	-	3.0	ns
T_{OFPF}	Output (O) to Pad via Output MUX, fast	All devices	-	3.7	-	4.4	ns
T_{OKFPF}	Select (OK) to Pad via Output MUX, fast	All devices	-	3.3	-	3.9	ns
T_{SLOW}	For Output SLOW option add	All devices	-	1.5	-	1.7	ns
Setup and Hold Times							
T_{OOK}	Output (O) to clock (OK) setup time	All devices	0.5	-	0.5	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T_{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	0.0	-	0.0	-	ns
T_{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.1	-	0.2	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T_{RPO}	Delay from GSR input to any Pad	XCS05XL	-	11.9	-	14.0	ns
		XCS10XL	-	12.4	-	14.5	ns
		XCS20XL	-	12.9	-	15.0	ns
		XCS30XL	-	13.9	-	16.0	ns
		XCS40XL	-	14.9	-	17.0	ns

Notes:

1. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	-	P85	P97	U12	T11	382 [3]
I/O	-	-	-	P99	V13	U12	385 [3]
I/O	-	-	-	P100	Y14	T12	388 [3]
VCC	-	-	P86	P101	VCC[4]	W13	-
I/O	P43	P60	P87	P102	Y15	V13	391 [3]
I/O	P44	P61	P88	P103	V14	U13	394 [3]
I/O	-	P62	P89	P104	W15	T13	397 [3]
I/O	-	P63	P90	P105	Y16	W14	400 [3]
GND	-	P64	P91	P106	GND[4]	GND[4]	-
I/O	-	-	-	P107	V15	V14	403 [3]
I/O	-	-	P92	P108	W16	U14	406 [3]
I/O	-	-	P93	P109	Y17	T14	409 [3]
I/O	-	-	P94	P110	V16	R14	412 [3]
I/O	-	-	P95	P111	W17	W15	415 [3]
I/O	-	-	P96	P112	Y18	U15	418 [3]
I/O	P45	P65	P97	P113	U16	V16	421 [3]
I/O	P46	P66	P98	P114	V17	U16	424 [3]
I/O	-	P67	P99	P115	W18	W17	427 [3]
I/O	-	P68	P100	P116	Y19	W18	430 [3]
I/O	P47	P69	P101	P117	V18	V17	433 [3]
I/O, SGCK3[1], GCK4[2]	P48	P70	P102	P118	W19	V18	436 [3]
GND	P49	P71	P103	P119	GND[4]	GND[4]	-
DONE	P50	P72	P104	P120	Y20	W19	-
VCC	P51	P73	P105	P121	VCC[4]	U17	-
$\overline{\text{PROGRAM}}$	P52	P74	P106	P122	V19	U18	-
I/O (D7[2])	P53	P75	P107	P123	U19	V19	439 [3]
I/O, PGCK3[1], GCK5[2]	P54	P76	P108	P124	U18	U19	442 [3]
I/O	-	P77	P109	P125	T17	T16	445 [3]
I/O	-	P78	P110	P126	V20	T17	448 [3]
I/O	-	-	-	P127	U20	T18	451 [3]
I/O	-	-	P111	P128	T18	T19	454 [3]
I/O (D6[2])	P55	P79	P112	P129	T19	R16	457 [3]
I/O	P56	P80	P113	P130	T20	R19	460 [3]
I/O	-	-	P114	P131	R18	P15	463 [3]
I/O	-	-	P115	P132	R19	P17	466 [3]
I/O	-	-	P116	P133	R20	P18	469 [3]
I/O	-	-	P117	P134	P18	P16	472 [3]
GND	-	P81	P118	P135	GND[4]	GND[4]	-
I/O	-	-	-	P136	P20	P19	475 [3]
I/O	-	-	-	P137	N18	N17	478 [3]
I/O	-	P82	P119	P138	N19	N18	481 [3]
I/O	-	P83	P120	P139	N20	N19	484 [3]
VCC	-	-	P121	P140	VCC[4]	N16	-
I/O (D5[2])	P57	P84	P122	P141	M17	M19	487 [3]
I/O	P58	P85	P123	P142	M18	M17	490 [3]

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	-	-	P190	B16	A15	23
I/O	-	P117	P166	P191	A16	E14	26
I/O	-	-	P167	P192	C15	C14	29
I/O	-	-	P168	P193	B15	B14	32
I/O	-	-	P169	P194	A15	D14	35
GND	-	P118	P170	P196	GND[4]	GND[4]	-
I/O	-	P119	P171	P197	B14	A14	38
I/O	-	P120	P172	P198	A14	C13	41
I/O	-	-	-	P199	C13	B13	44
I/O	-	-	-	P200	B13	A13	47
VCC	-	-	P173	P201	VCC[4]	D13	-
I/O	P82	P121	P174	P202	C12	B12	50
I/O	P83	P122	P175	P203	B12	D12	53
I/O	-	-	P176	P205	A12	A11	56
I/O	-	-	P177	P206	B11	B11	59
I/O	P84	P123	P178	P207	C11	C11	62
I/O	P85	P124	P179	P208	A11	D11	65
I/O	P86	P125	P180	P209	A10	A10	68
I/O	P87	P126	P181	P210	B10	B10	71
GND	P88	P127	P182	P211	GND[4]	GND[4]	-

2/8/00

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND[4] or V_{CC}[4] are internally bonded to Ground or V_{CC} planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01

Additional XCS30/XL Package Pins

PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

2/12/98

GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

6/4/97

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

CS280

VCC Pins					
A1	A7	C10	C17	D13	G1
G1	G19	K2	K17	M4	N16
T7	U3	U10	U17	W13	-
GND Pins					

Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: **Component Availability Chart for Spartan/XL FPGAs**

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84(3)	VQ100(3)	CS144(3)	TQ144	PQ208	PQ240	BG256(3)	CS280(3)
XCS05	-3	C(3)	C, I	-	-	-	-	-	-
	-4	C(3)	C	-	-	-	-	-	-
XCS10	-3	C(3)	C, I	-	C	-	-	-	-
	-4	C(3)	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C(3)	-	C, I	C, I	C	C(3)	-
	-4	-	C(3)	-	C	C	C	C(3)	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C(3)	C, I	-	-	-	-	-	-
	-5	C(3)	C	-	-	-	-	-	-
XCS10XL	-4	C(3)	C, I	C(3)	C	-	-	-	-
	-5	C(3)	C	C(3)	C	-	-	-	-
XCS20XL	-4	-	C, I	C(3)	C, I	C, I	-	-	-
	-5	-	C	C(3)	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C(3)
	-5	-	C	-	C	C	C	C	C(3)
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C(3)
	-5	-	-	-	-	C	C	C	C(3)

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Notes:

1. C = Commercial T_J = 0° to +85°C
2. I = Industrial T_J = –40°C to +100°C
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

www.xilinx.com/support/documentation/spartan-xl.htm#19687

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

www.xilinx.com/cgi-bin/thermal/thermal.pl