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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	205
Number of Gates	40000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40-4bg256c

This high value makes them unsuitable as wired-AND pull-up resistors.

Table 7: Supported Destinations for Spartan/XL Outputs

Destination	Spartan-XL Outputs	Spartan Outputs	
	3.3V, CMOS	5V, TTL	5V, CMOS
Any device, $V_{CC} = 3.3V$, CMOS-threshold inputs	✓	✓	Some ⁽¹⁾
Any device, $V_{CC} = 5V$, TTL-threshold inputs	✓	✓	✓
Any device, $V_{CC} = 5V$, CMOS-threshold inputs	Unreliable Data		✓

Notes:

1. Only if destination device has 5V tolerant inputs.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULL-DOWN library component to the net attached to the pad.

Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops (Figure 5). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either

falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (see EC signal in Figure 5), which through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan/XL FPGA CLB. It cannot be inverted within the IOB.

Routing Channel Description

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

This section describes the routing channels available in Spartan/XL devices. Figure 8 shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the designer should open a design in the FPGA Editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

CLB Routing Channels

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). Figure 8 shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.

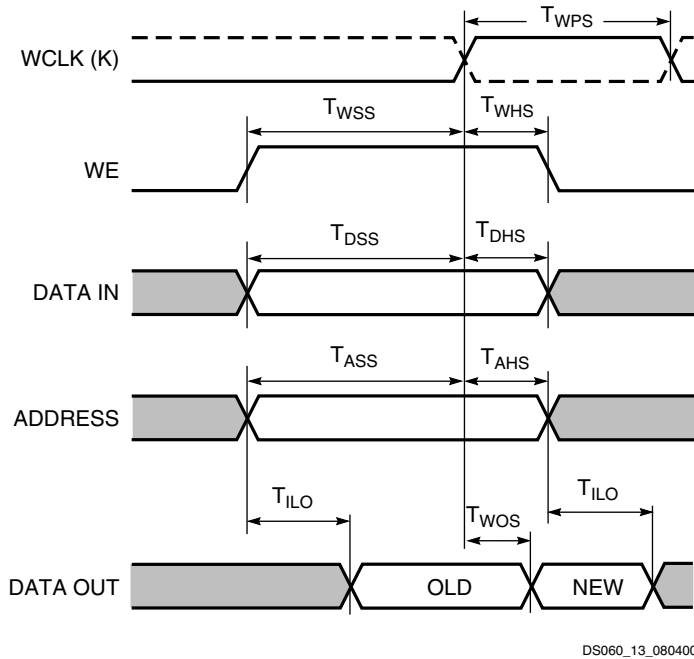


Figure 13: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be

inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO} , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS} , the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by $A[3:0]$ while the second provides only for read operations at the address specified independently by $DPRA[3:0]$. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the

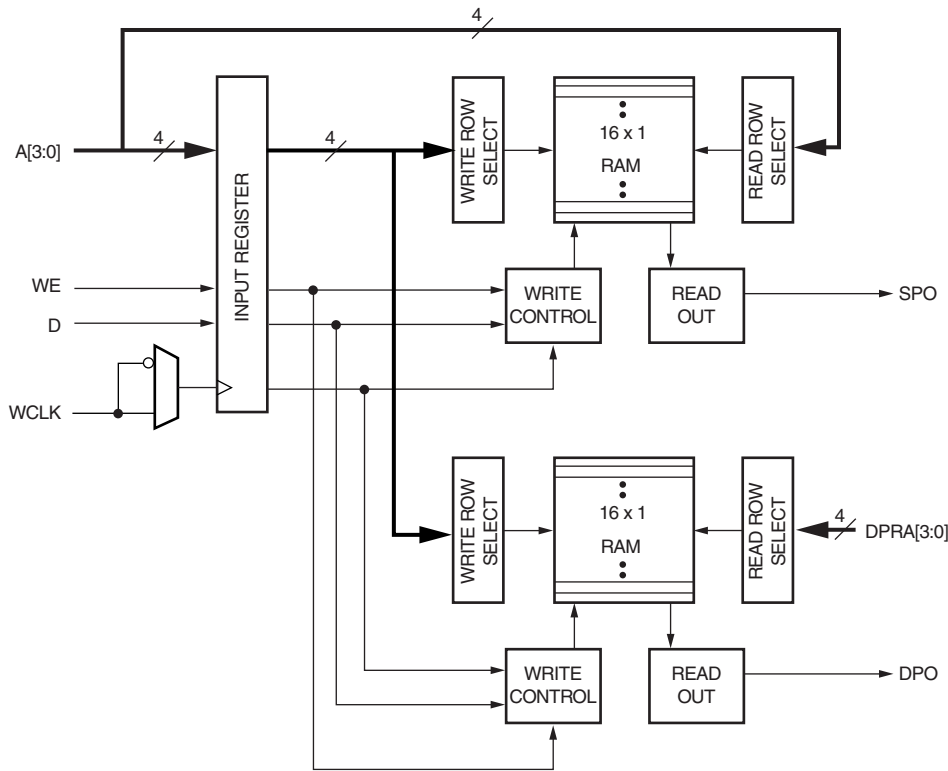


Figure 14: Logic Diagram for the Dual-Port RAM

CLB signals from which they are originally derived are shown in [Table 10](#).

Table 10: Dual-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F _{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G _{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in [Figure 13](#).

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

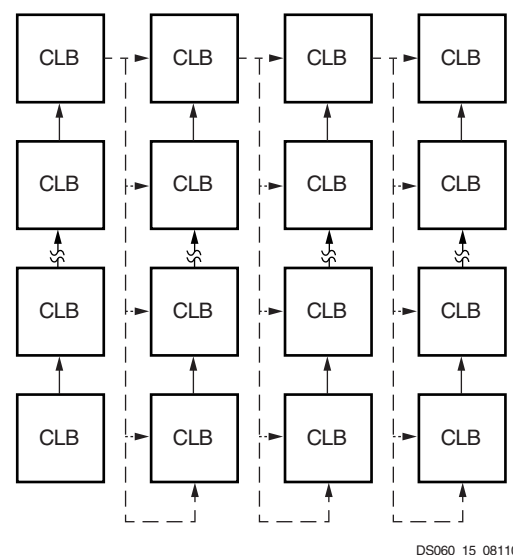
Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See [Figure 15](#).)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in micro-processor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan



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Figure 15: Available Spartan/XL Carry Propagation Paths

and Spartan-XL families, speeding up arithmetic and counting functions.

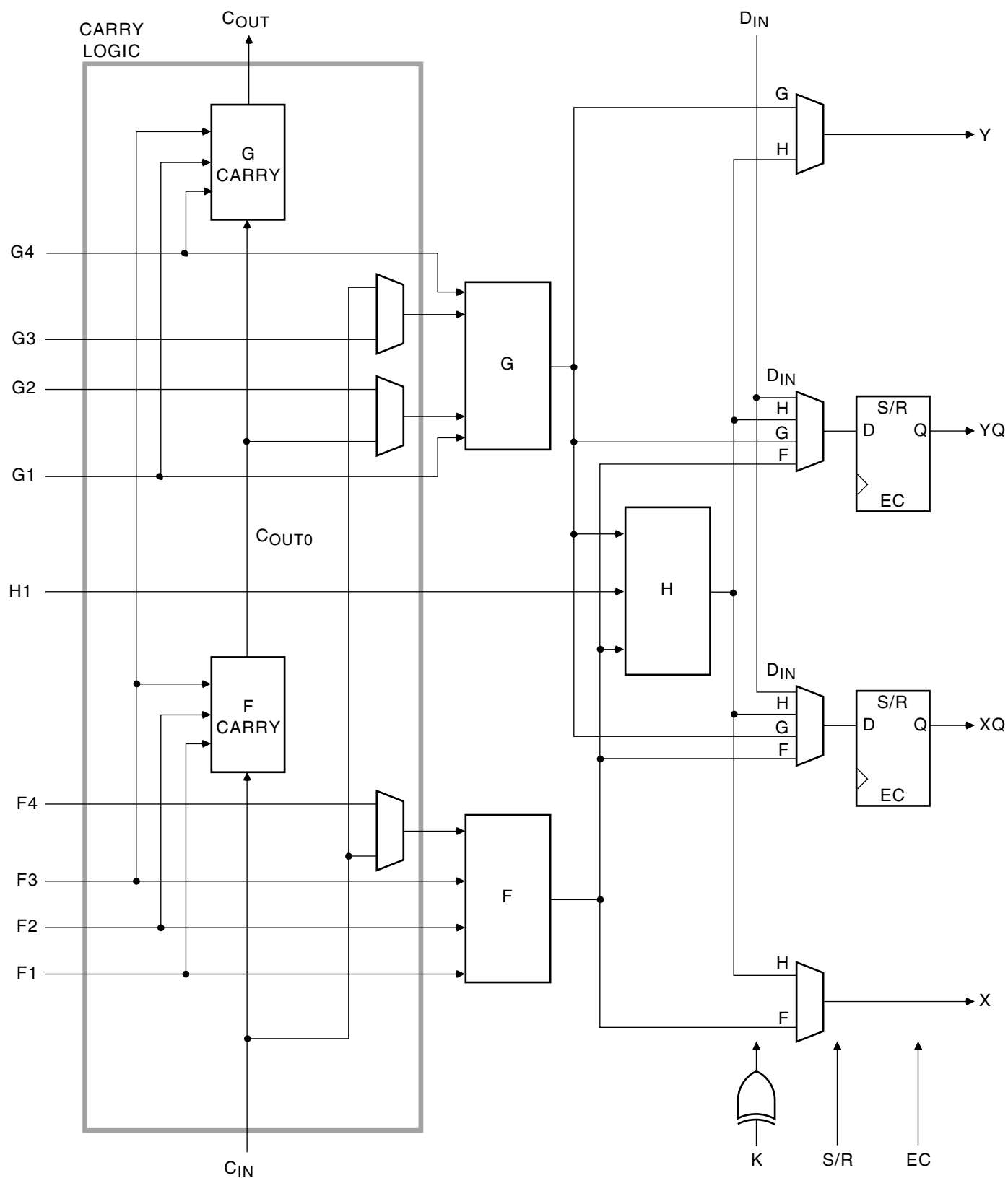
The carry chain in 5V Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in Spartan-XL devices can only run up the column, providing even higher speed.

Figure 16, page 18 shows a Spartan/XL FPGA CLB with dedicated fast carry logic. The carry logic shares operand

and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

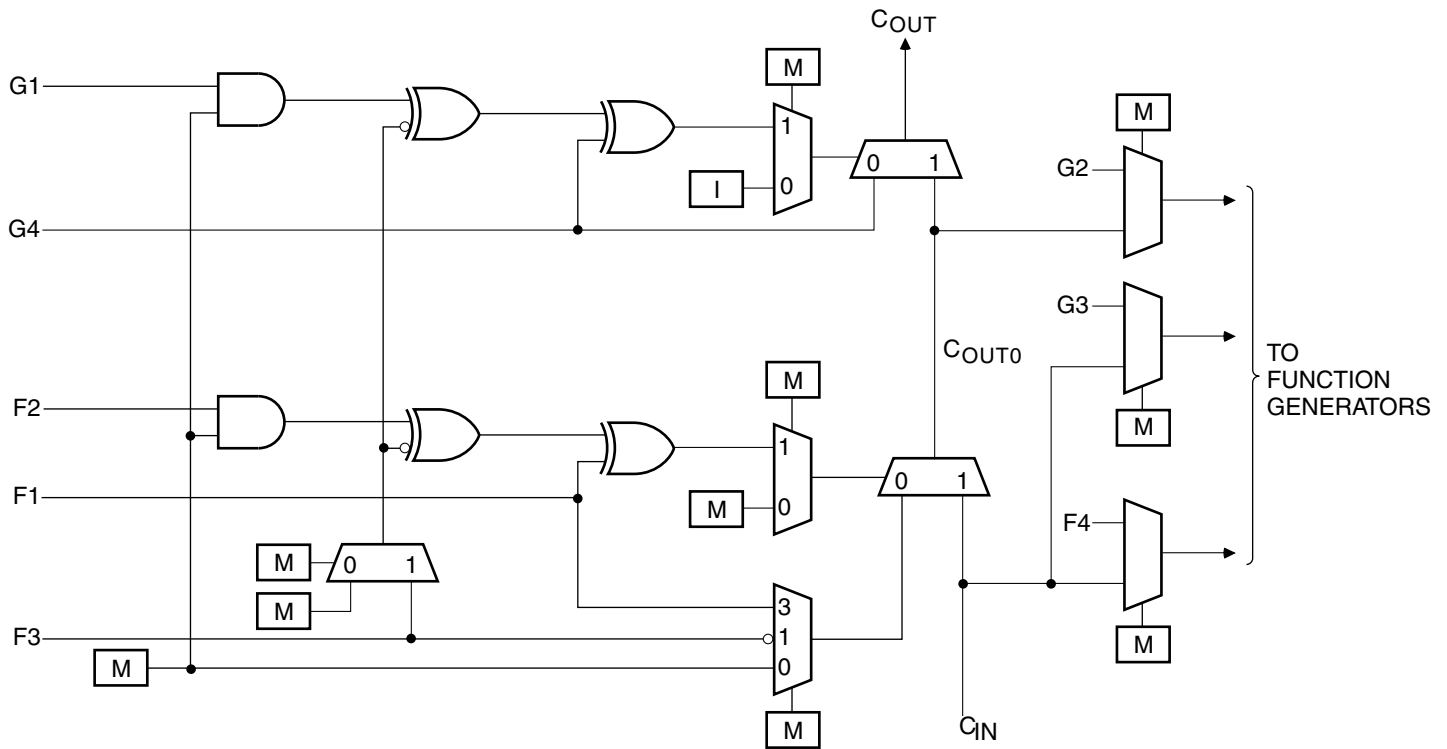
Figure 17, page 19 shows the details of the Spartan/XL FPGA carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 16.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.



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Figure 16: Fast Carry Logic in Spartan/XL CLB



DS060_17_080400

Figure 17: Detail of Spartan/XL Dedicated Carry Logic

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

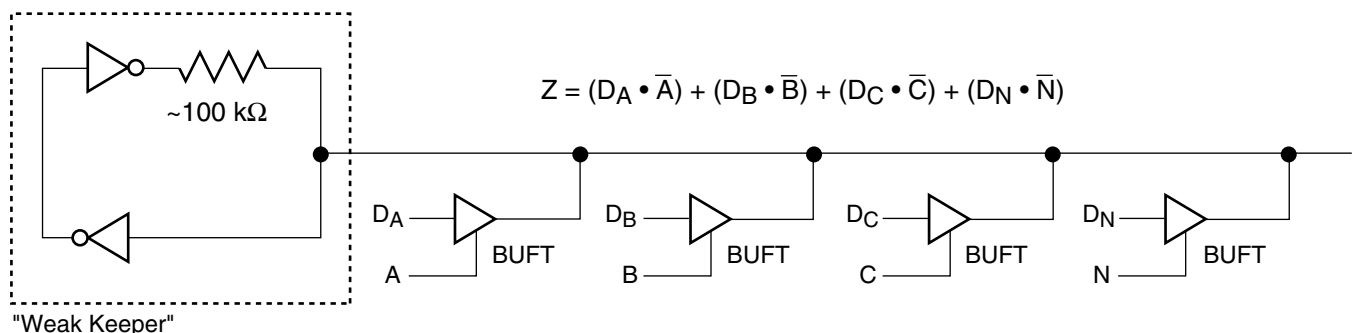
Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

Table 11: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN



DS060_18_080400

Figure 18: 3-state Buffers Implement a Multiplexer

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

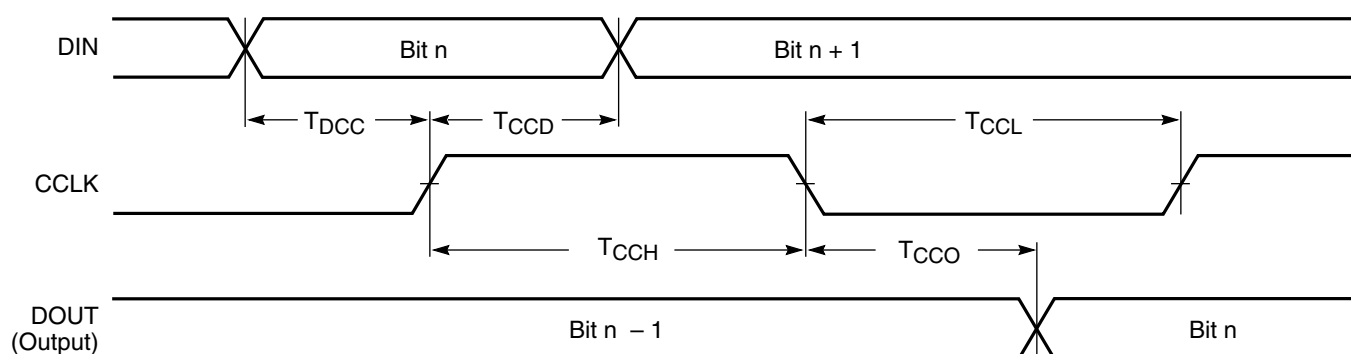
The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.



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Symbol		Description	Min	Max	Units
T_{DCC}	CCLK	DIN setup	20	-	ns
T_{CCD}		DIN hold	0	-	ns
T_{CCO}		DIN to DOUT	-	30	ns
T_{CCH}		High time	40	-	ns
T_{CCL}		Low time	40	-	ns
F_{CC}		Frequency	-	12.5	MHz

Notes:

1. Configuration must be delayed until the \overline{INIT} pins of all daisy-chained FPGAs are High.

Figure 26: Slave Serial Mode Programming Switching Characteristics

Express Mode (Spartan-XL Family Only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

Pseudo Daisy Chain

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices

are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized

Spartan Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more pre-

cise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Spartan Family Output Flip-Flop, Clock-to-Out

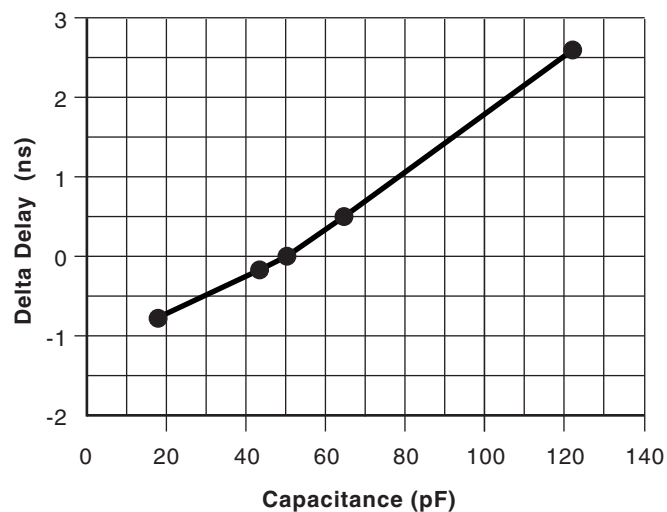
Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
Global Primary Clock to TTL Output using OFF					
T _{ICKOF}	Fast	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
T _{ICKO}	Slew-rate limited	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
T _{ICKSOF}	Fast	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
T _{ICKSO}	Slew-rate limited	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
T _{CMOSOF}	Fast	All devices	0.8	1.0	ns
T _{CMOSO}	Slew-rate limited	All devices	1.5	2.0	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see [Figure 34](#).
3. OFF = Output Flip-Flop

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.



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Figure 34: Delay Factor at Various Capacitive Loads

Spartan-XL Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For

more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
T_{GLS}	From pad through buffer, to any clock K	XCS05XL	1.4	1.5	ns
		XCS10XL	1.7	1.8	ns
		XCS20XL	2.0	2.1	ns
		XCS30XL	2.3	2.5	ns
		XCS40XL	2.6	2.8	ns

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

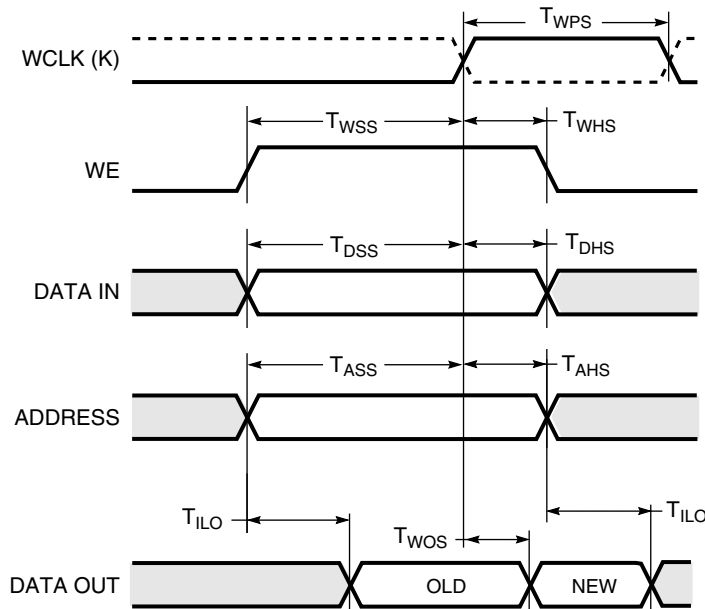
Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation ⁽¹⁾							
T _{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T _{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T _{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T _{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T _{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T _{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

Notes:

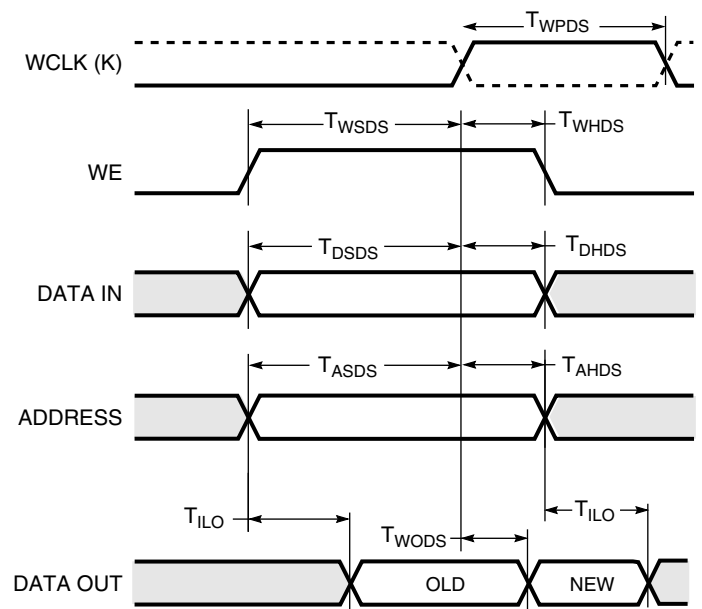
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



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Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See **Global Signals: GSR and GTS**, page 20 for more information.

Device pins for Spartan/XL devices are described in **Table 18**.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pin-outs as the standard package options.

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
V _{CC}	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 – 0.1 μ F capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See Violating the Maximum High and Low Time Specification for the Readback Clock , page 39 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an open-drain output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.

Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and Spartan-XL device. They follow the pad locations around the die, and include boundary scan register locations.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 ⁽⁴⁾	VQ100	Bndry Scan
VCC	P2	P89	-
I/O	P3	P90	32
I/O	P4	P91	35
I/O	-	P92	38
I/O	-	P93	41
I/O	P5	P94	44
I/O	P6	P95	47
I/O	P7	P96	50
I/O	P8	P97	53
I/O	P9	P98	56
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P10	P99	59
VCC	P11	P100	-
GND	P12	P1	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P13	P2	62
I/O	P14	P3	65
I/O, TDI	P15	P4	68
I/O, TCK	P16	P5	71
I/O, TMS	P17	P6	74
I/O	P18	P7	77
I/O	-	P8	83
I/O	P19	P9	86
I/O	P20	P10	89
GND	P21	P11	-
VCC	P22	P12	-
I/O	P23	P13	92
I/O	P24	P14	95
I/O	-	P15	98
I/O	P25	P16	104
I/O	P26	P17	107
I/O	P27	P18	110
I/O	-	P19	113
I/O	P28	P20	116
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P29	P21	119
Not Connected ⁽¹⁾ , M1 ⁽²⁾	P30	P22	122
GND	P31	P23	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P32	P24	125
VCC	P33	P25	-

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84 ⁽⁴⁾	VQ100	Bndry Scan
Not Connected ⁽¹⁾ , PWRDWN ⁽²⁾	P34	P26	126 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P35	P27	127 ⁽³⁾
I/O (HDC)	P36	P28	130 ⁽³⁾
I/O	-	P29	133 ⁽³⁾
I/O (LDC)	P37	P30	136 ⁽³⁾
I/O	P38	P31	139 ⁽³⁾
I/O	P39	P32	142 ⁽³⁾
I/O	-	P33	145 ⁽³⁾
I/O	-	P34	148 ⁽³⁾
I/O	P40	P35	151 ⁽³⁾
I/O (INIT)	P41	P36	154 ⁽³⁾
VCC	P42	P37	-
GND	P43	P38	-
I/O	P44	P39	157 ⁽³⁾
I/O	P45	P40	160 ⁽³⁾
I/O	-	P41	163 ⁽³⁾
I/O	-	P42	166 ⁽³⁾
I/O	P46	P43	169 ⁽³⁾
I/O	P47	P44	172 ⁽³⁾
I/O	P48	P45	175 ⁽³⁾
I/O	P49	P46	178 ⁽³⁾
I/O	P50	P47	181 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P51	P48	184 ⁽³⁾
GND	P52	P49	-
DONE	P53	P50	-
VCC	P54	P51	-
PROGRAM	P55	P52	-
I/O (D7 ⁽²⁾)	P56	P53	187 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P57	P54	190 ⁽³⁾
I/O (D6 ⁽²⁾)	P58	P55	193 ⁽³⁾
I/O	-	P56	196 ⁽³⁾
I/O (D5 ⁽²⁾)	P59	P57	199 ⁽³⁾
I/O	P60	P58	202 ⁽³⁾
I/O	-	P59	205 ⁽³⁾
I/O	-	P60	208 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	P61	211 ⁽³⁾
I/O	P62	P62	214 ⁽³⁾
VCC	P63	P63	-
GND	P64	P64	-
I/O (D3 ⁽²⁾)	P65	P65	217 ⁽³⁾
I/O	P66	P66	220 ⁽³⁾
I/O	-	P67	223 ⁽³⁾
I/O (D2 ⁽²⁾)	P67	P68	229 ⁽³⁾
I/O	P68	P69	232 ⁽³⁾
I/O (D1 ⁽²⁾)	P69	P70	235 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC ⁽²⁾	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P21	L2	P33	P49	239
Not Connected ⁽¹⁾ M1 ⁽²⁾	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected ⁽¹⁾ PWRDWN ⁽²⁾	P26	N2	P38	P54	246 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P27	M3	P39	P55	247 ⁽³⁾
I/O (HDC)	P28	N3	P40	P56	250 ⁽³⁾
I/O	-	K4	P41	P57	253 ⁽³⁾
I/O	-	L4	P42	P58	256 ⁽³⁾
I/O	P29	M4	P43	P59	259 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O (LDC)	P30	N4	P44	P60	262 ⁽³⁾
I/O	-	-	-	P61	265 ⁽³⁾
I/O	-	-	-	P62	268 ⁽³⁾
I/O	-	-	-	P63	271 ⁽³⁾
I/O	-	-	-	P64	274 ⁽³⁾
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 ⁽³⁾
I/O	-	M5	P47	P68	280 ⁽³⁾
I/O	P31	N5	P48	P69	283 ⁽³⁾
I/O	P32	K6	P49	P70	286 ⁽³⁾
VCC ⁽²⁾	-	-	-	P71	-
I/O	-	-	-	P72	289 ⁽³⁾
I/O	-	-	-	P73	292 ⁽³⁾
I/O	P33	L6	P50	P74	295 ⁽³⁾
I/O	P34	M6	P51	P75	298 ⁽³⁾
I/O	P35	N6	P52	P76	301 ⁽³⁾
I/O (INIT)	P36	M7	P53	P77	304 ⁽³⁾
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 ⁽³⁾
I/O	P40	N8	P57	P81	310 ⁽³⁾
I/O	P41	M8	P58	P82	313 ⁽³⁾
I/O	P42	L8	P59	P83	316 ⁽³⁾
I/O	-	-	-	P84	319 ⁽³⁾
I/O	-	-	-	P85	322 ⁽³⁾
VCC ⁽²⁾	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 ⁽³⁾
I/O	P44	N9	P61	P88	328 ⁽³⁾
I/O	-	M9	P62	P89	331 ⁽³⁾
I/O	-	L9	P63	P90	334 ⁽³⁾
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 ⁽³⁾
I/O	-	-	-	P94	340 ⁽³⁾
I/O	-	-	-	P95	343 ⁽³⁾
I/O	-	-	-	P96	346 ⁽³⁾
I/O	P45	N10	P65	P97	349 ⁽³⁾
I/O	P46	M10	P66	P98	352 ⁽³⁾
I/O	-	L10	P67	P99	355 ⁽³⁾
I/O	-	N11	P68	P100	358 ⁽³⁾
I/O	P47	M11	P69	P101	361 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P48	L11	P70	P102	364 ⁽³⁾
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7 ⁽²⁾)	P53	L12	P75	P107	367 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P54	L13	P76	P108	370 ⁽³⁾
I/O	-	K10	P77	P109	373 ⁽³⁾
I/O	-	K11	P78	P110	376 ⁽³⁾
I/O (D6 ⁽²⁾)	P55	K12	P79	P112	379 ⁽³⁾
I/O	P56	K13	P80	P113	382 ⁽³⁾
I/O	-	-	-	P114	385 ⁽³⁾
I/O	-	-	-	P115	388 ⁽³⁾
I/O	-	-	-	P116	391 ⁽³⁾
I/O	-	-	-	P117	394 ⁽³⁾
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 ⁽³⁾
I/O	-	J12	P83	P120	400 ⁽³⁾
VCC ⁽²⁾	-	-	-	P121	-
I/O (D5 ⁽²⁾)	P57	J13	P84	P122	403 ⁽³⁾
I/O	P58	H10	P85	P123	406 ⁽³⁾
I/O	-	-	-	P124	409 ⁽³⁾
I/O	-	-	-	P125	412 ⁽³⁾
I/O	P59	H11	P86	P126	415 ⁽³⁾
I/O	P60	H12	P87	P127	418 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	H13	P88	P128	421 ⁽³⁾
I/O	P62	G12	P89	P129	424 ⁽³⁾
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3 ⁽²⁾)	P65	G10	P92	P132	427 ⁽³⁾
I/O	P66	F13	P93	P133	430 ⁽³⁾
I/O	P67	F12	P94	P134	433 ⁽³⁾
I/O	-	F11	P95	P135	436 ⁽³⁾
I/O	-	-	-	P136	439 ⁽³⁾
I/O	-	-	-	P137	442 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	F10	P96	P138	445 ⁽³⁾
I/O	P69	E13	P97	P139	448 ⁽³⁾
VCC ⁽²⁾	-	-	-	P140	-
I/O	-	E12	P98	P141	451 ⁽³⁾
I/O	-	E11	P99	P142	454 ⁽³⁾
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 ⁽³⁾
I/O	-	-	-	P146	460 ⁽³⁾
I/O	-	-	-	P147	463 ⁽³⁾
I/O	-	-	-	P148	466 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	D13	P101	P149	469 ⁽³⁾
I/O	P71	D12	P102	P150	472 ⁽³⁾
I/O	-	D11	P103	P151	475 ⁽³⁾

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 ^(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	C12	P105	P153	481 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	C11	P106	P154	484 ⁽³⁾
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1 ⁽²⁾)	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC ⁽²⁾	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

2/8/00

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	P18	P28	P44	P52	V1	T1	272
I/O	P19	P29	P45	P53	T4	T2	275
I/O	-	P30	P46	P54	U3	T3	278
I/O	-	P31	P47	P55	V2	U1	281
I/O	P20	P32	P48	P56	W1	V1	284
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P21	P33	P49	P57	V3	U2	287
Not Connected ⁽¹⁾ , M1 ⁽²⁾	P22	P34	P50	P58	W2	V2	290
GND	P23	P35	P51	P59	GND ⁽⁴⁾	GND ⁽⁴⁾	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P24	P36	P52	P60	Y1	W1	293
VCC	P25	P37	P53	P61	VCC ⁽⁴⁾	U3	-
Not Connected ⁽¹⁾ , PWRDWN ⁽²⁾	P26	P38	P54	P62	W3	V3	294 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P27	P39	P55	P63	Y2	W2	295 ⁽³⁾
I/O (HDC)	P28	P40	P56	P64	W4	W3	298 ⁽³⁾
I/O	-	P41	P57	P65	V4	T4	301 ⁽³⁾
I/O	-	P42	P58	P66	U5	U4	304 ⁽³⁾
I/O	P29	P43	P59	P67	Y3	V4	307 ⁽³⁾
I/O (LDC)	P30	P44	P60	P68	Y4	W4	310 ⁽³⁾
I/O	-	-	P61	P69	V5	T5	313 ⁽³⁾
I/O	-	-	P62	P70	W5	W5	316 ⁽³⁾
I/O	-	-	P63	P71	Y5	R6	319 ⁽³⁾
I/O	-	-	P64	P72	V6	U6	322 ⁽³⁾
I/O	-	-	P65	P73	W6	V6	325 ⁽³⁾
I/O	-	-	-	P74	Y6	T6	328 ⁽³⁾
GND	-	P45	P66	P75	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P46	P67	P76	W7	W6	331 ⁽³⁾
I/O	-	P47	P68	P77	Y7	U7	334 ⁽³⁾
I/O	P31	P48	P69	P78	V8	V7	337 ⁽³⁾
I/O	P32	P49	P70	P79	W8	W7	340 ⁽³⁾
VCC	-	-	P71	P80	VCC ⁽⁴⁾	T7	-
I/O	-	-	P72	P81	Y8	W8	343 ⁽³⁾
I/O	-	-	P73	P82	U9	U8	346 ⁽³⁾
I/O	-	-	-	P84	Y9	W9	349 ⁽³⁾
I/O	-	-	-	P85	W10	V9	352 ⁽³⁾
I/O	P33	P50	P74	P86	V10	U9	355 ⁽³⁾
I/O	P34	P51	P75	P87	Y10	T9	358 ⁽³⁾
I/O	P35	P52	P76	P88	Y11	W10	361 ⁽³⁾
I/O (INIT)	P36	P53	P77	P89	W11	V10	364 ⁽³⁾
VCC	P37	P54	P78	P90	VCC ⁽⁴⁾	U10	-
GND	P38	P55	P79	P91	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P39	P56	P80	P92	V11	T10	367 ⁽³⁾
I/O	P40	P57	P81	P93	U11	R10	370 ⁽³⁾
I/O	P41	P58	P82	P94	Y12	W11	373 ⁽³⁾
I/O	P42	P59	P83	P95	W12	V11	376 ⁽³⁾
I/O	-	-	P84	P96	V12	U11	379 ⁽³⁾

CS280

VCC Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-
Not Connected Pins					
A4	A12	C8	C12	C15	D1
D2	D5	D8	D17	D18	E15
H2	H3	H18	H19	L4	M1
M16	M18	R2	R4	R5	R15
R17	T8	T15	U5	V8	V12
W12	W16	-	-	-	-
Not Connected Pins (VCC in XCS40XL)					
B5	B15	E3	E18	R3	R18
V5	V15	-	-	-	-

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XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
VCC	P183	P212	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P184	P213	C10	D10	86
I/O	P185	P214	D10	E10	89
I/O	P186	P215	A9	A9	92
I/O	P187	P216	B9	B9	95
I/O	P188	P217	C9	C9	98
I/O	P189	P218	D9	D9	101
I/O	P190	P220	A8	A8	104
I/O	P191	P221	B8	B8	107
I/O	-	-	C8	C8	110
I/O	-	-	A7	D8	113
VCC	P192	P222	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	P223	A6	B7	116
I/O	-	P224	C7	C7	119
I/O	P193	P225	B6	D7	122
I/O	P194	P226	A5	A6	125
GND	P195	P227	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P196	P228	C6	B6	128
I/O	P197	P229	B5	C6	131
I/O	P198	P230	A4	D6	134
I/O	P199	P231	C5	E6	137

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
I/O	P200	P232	B4	A5	140
I/O	P201	P233	A3	C5	143
I/O	-	-	-	D5	146
I/O	-	-	-	A4	149
I/O	P202	P234	D5	B4	152
I/O	P203	P235	C4	C4	155
I/O	P204	P236	B3	A3	158
I/O	P205	P237	B2	A2	161
I/O	P206	P238	A2	B3	164
I/O, SGCK1 ⁽¹⁾ , GCK8 ⁽²⁾	P207	P239	C3	B2	167
VCC	P208	P240	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
GND	P1	P1	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O, PGCK1 ⁽¹⁾ , GCK1 ⁽²⁾	P2	P2	B1	C3	170
I/O	P3	P3	C2	C2	173
I/O	P4	P4	D2	B1	176
I/O	P5	P5	D3	C1	179
I/O, TDI	P6	P6	E4	D4	182
I/O, TCK	P7	P7	C1	D3	185
I/O	-	-	-	D2	188
I/O	-	-	-	D1	191
I/O	P8	P8	D1	E2	194
I/O	P9	P9	E3	E4	197
I/O	P10	P10	E2	E1	200
I/O	P11	P11	E1	F5	203
I/O	P12	P12	F3	F3	206
I/O	-	P13	F2	F2	209
GND	P13	P14	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P14	P15	G3	F4	212
I/O	P15	P16	G2	F1	215
I/O, TMS	P16	P17	G1	G3	218
I/O	P17	P18	H3	G2	221
VCC	P18	P19	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	-	P20	H2	G4	224
I/O	-	P21	H1	H1	227
I/O	-	-	J4	H3	230
I/O	-	-	J3	H2	233
I/O	P19	P23	J2	H4	236
I/O	P20	P24	J1	J1	239
I/O	P21	P25	K2	J2	242
I/O	P22	P26	K3	J3	245
I/O	P23	P27	K1	J4	248
I/O	P24	P28	L1	K1	251

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
I/O	P90	P105	Y16	W14	466 ⁽³⁾
GND	P91	P106	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P107	V15	V14	469 ⁽³⁾
I/O	P92	P108	W16	U14	472 ⁽³⁾
I/O	P93	P109	Y17	T14	475 ⁽³⁾
I/O	P94	P110	V16	R14	478 ⁽³⁾
I/O	P95	P111	W17	W15	481 ⁽³⁾
I/O	P96	P112	Y18	U15	484 ⁽³⁾
I/O	-	-	-	T15	487 ⁽³⁾
I/O	-	-	-	W16	490 ⁽³⁾
I/O	P97	P113	U16	V16	493 ⁽³⁾
I/O	P98	P114	V17	U16	496 ⁽³⁾
I/O	P99	P115	W18	W17	499 ⁽³⁾
I/O	P100	P116	Y19	W18	502 ⁽³⁾
I/O	P101	P117	V18	V17	505 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P102	P118	W19	V18	508 ⁽³⁾
GND	P103	P119	GND ⁽⁴⁾	GND ⁽⁴⁾	-
DONE	P104	P120	Y20	W19	-
VCC	P105	P121	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
PROGRAM	P106	P122	V19	U18	-
I/O (D7 ⁽²⁾)	P107	P123	U19	V19	511 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P108	P124	U18	U19	514 ⁽³⁾
I/O	P109	P125	T17	T16	517 ⁽³⁾
I/O	P110	P126	V20	T17	520 ⁽³⁾
I/O	-	P127	U20	T18	523 ⁽³⁾
I/O	P111	P128	T18	T19	526 ⁽³⁾
I/O	-	-	-	R15	529 ⁽³⁾
I/O	-	-	-	R17	523 ⁽³⁾
I/O (D6 ⁽²⁾)	P112	P129	T19	R16	535 ⁽³⁾
I/O	P113	P130	T20	R19	538 ⁽³⁾
I/O	P114	P131	R18	P15	541 ⁽³⁾
I/O	P115	P132	R19	P17	544 ⁽³⁾
I/O	P116	P133	R20	P18	547 ⁽³⁾
I/O	P117	P134	P18	P16	550 ⁽³⁾
GND	P118	P135	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P136	P20	P19	553 ⁽³⁾
I/O	-	P137	N18	N17	556 ⁽³⁾
I/O	P119	P138	N19	N18	559 ⁽³⁾
I/O	P120	P139	N20	N19	562 ⁽³⁾
VCC	P121	P140	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O (D5 ⁽²⁾)	P122	P141	M17	M19	565 ⁽³⁾
I/O	P123	P142	M18	M17	568 ⁽³⁾

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
I/O	-	-	-	M18	571 ⁽³⁾
I/O	-	-	M19	M16	574 ⁽³⁾
I/O	P124	P144	M20	L19	577 ⁽³⁾
I/O	P125	P145	L19	L18	580 ⁽³⁾
I/O	P126	P146	L18	L17	583 ⁽³⁾
I/O	P127	P147	L20	L16	586 ⁽³⁾
I/O (D4 ⁽²⁾)	P128	P148	K20	K19	589 ⁽³⁾
I/O	P129	P149	K19	K18	592 ⁽³⁾
VCC	P130	P150	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
GND	P131	P151	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O (D3 ⁽²⁾)	P132	P152	K18	K16	595 ⁽³⁾
I/O	P133	P153	K17	K15	598 ⁽³⁾
I/O	P134	P154	J20	J19	601 ⁽³⁾
I/O	P135	P155	J19	J18	604 ⁽³⁾
I/O	P136	P156	J18	J17	607 ⁽³⁾
I/O	P137	P157	J17	J16	610 ⁽³⁾
I/O	-	-	H20	H19	613 ⁽³⁾
I/O	-	-	-	H18	616 ⁽³⁾
I/O (D2 ⁽²⁾)	P138	P159	H19	H17	619 ⁽³⁾
I/O	P139	P160	H18	H16	622 ⁽³⁾
VCC	P140	P161	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P141	P162	G19	G18	625 ⁽³⁾
I/O	P142	P163	F20	G17	628 ⁽³⁾
I/O	-	P164	G18	G16	631 ⁽³⁾
I/O	-	P165	F19	F19	634 ⁽³⁾
GND	P143	P166	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P167	F18	F18	637 ⁽³⁾
I/O	P144	P168	E19	F17	640 ⁽³⁾
I/O	P145	P169	D20	F16	643 ⁽³⁾
I/O	P146	P170	E18	F15	646 ⁽³⁾
I/O	P147	P171	D19	E19	649 ⁽³⁾
I/O	P148	P172	C20	E17	652 ⁽³⁾
I/O (D1 ⁽²⁾)	P149	P173	E17	E16	655 ⁽³⁾
I/O	P150	P174	D18	D19	658 ⁽³⁾
I/O	-	-	-	D18	661 ⁽³⁾
I/O	-	-	-	D17	664 ⁽³⁾
I/O	P151	P175	C19	C19	667 ⁽³⁾
I/O	P152	P176	B20	B19	670 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P153	P177	C18	C18	673 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P154	P178	B19	B18	676 ⁽³⁾
CCLK	P155	P179	A20	A19	-
VCC	P156	P180	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-

Table 20: User I/O Chart for Spartan/XL FPGAs

Device	Max I/O	Package Type							
		PC84 ⁽¹⁾	VQ100 ⁽¹⁾	CS144 ⁽¹⁾	TQ144	PQ208	PQ240	BG256 ⁽¹⁾	CS280 ⁽¹⁾
XCS05	80	61 ⁽¹⁾	77	-	-	-	-	-	-
XCS10	112	61 ⁽¹⁾	77	-	112	-	-	-	-
XCS20	160	-	77	-	113	160	-	-	-
XCS30	192	-	77 ⁽¹⁾	-	113	169	192	192 ⁽¹⁾	-
XCS40	224	-	-	-	-	169	192	205	-
XCS05XL	80	61 ⁽¹⁾	77 ⁽²⁾	-	-	-	-	-	-
XCS10XL	112	61 ⁽¹⁾	77 ⁽²⁾	112 ⁽¹⁾	112 ⁽²⁾	-	-	-	-
XCS20XL	160	-	77 ⁽²⁾	113 ⁽¹⁾	113 ⁽²⁾	160 ⁽²⁾	-	-	-
XCS30XL	192	-	77 ⁽²⁾	-	113 ⁽²⁾	169 ⁽²⁾	192 ⁽²⁾	192 ⁽²⁾	192 ⁽¹⁾
XCS40XL	224	-	-	-	-	169 ⁽²⁾	192 ⁽²⁾	205 ⁽²⁾	224 ⁽¹⁾

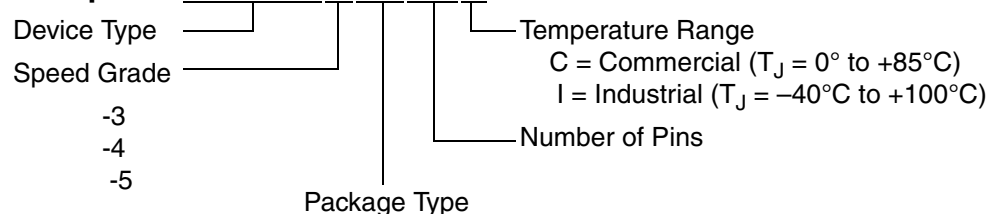
6/25/08

Notes:

1. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
2. These Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Ordering Information

Example: XCS20XL-4 PQ208C



BG = Ball Grid Array

BGG = Ball Grid Array (Pb-free)

PC = Plastic Lead Chip Carrier

PQ = Plastic Quad Flat Pack

PQG = Plastic Quad Flat Pack (Pb-free)

VQ = Very Thin Quad Flat Pack

VQG = Very Thin Quad Flat Pack (Pb-free)

TQ = Thin Quad Flat Pack

TQG = Thin Quad Flat Pack (Pb-free)

CS = Chip Scale