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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	169
Number of Gates	40000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xcs40-4pq208c">https://www.e-xfl.com/product-detail/xilinx/xcs40-4pq208c</a>

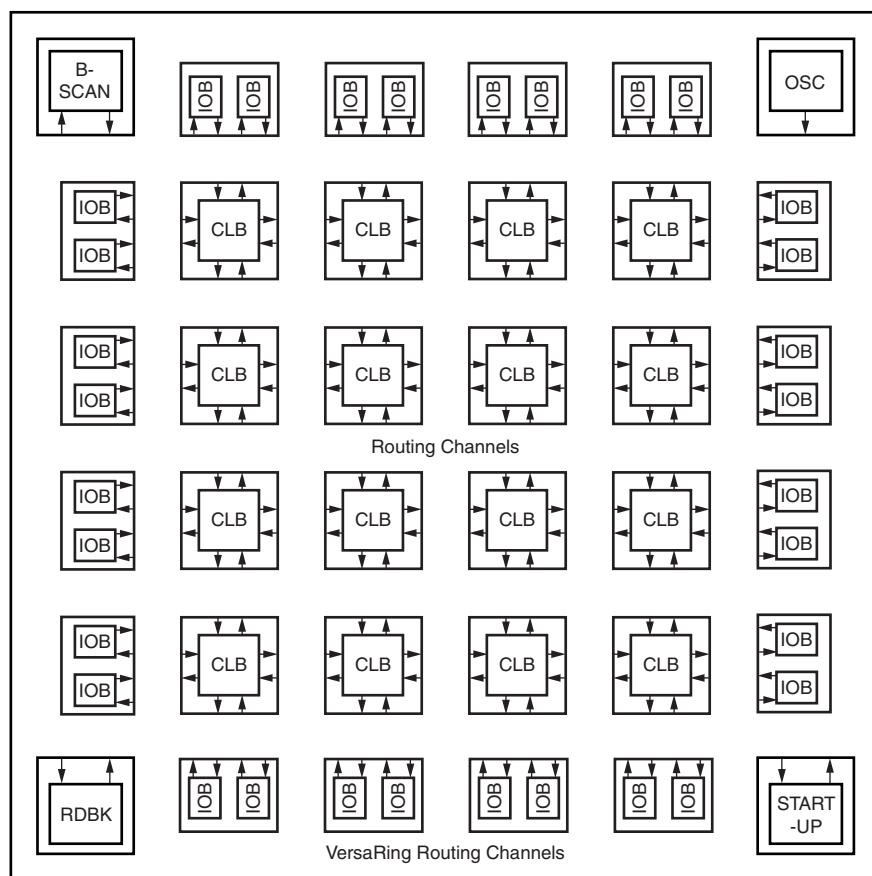
## General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in **Figure 1**. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these

memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.



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Figure 1: Basic FPGA Block Diagram

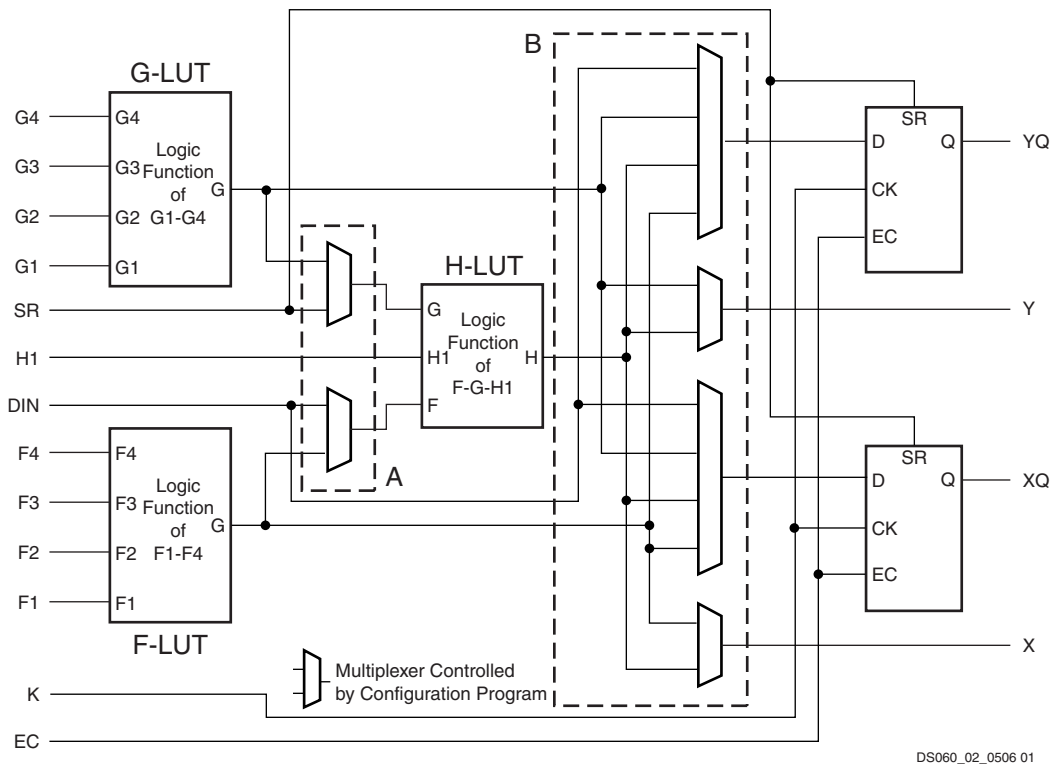


Figure 2: Spartan/XL Simplified CLB Logic Diagram (some features not shown)

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables
- Note:** When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.
- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

### Flip-Flops


Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see [Figure 2](#)). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in [Global Signals: GSR and GTS, page 20](#).


### Latches (Spartan-XL Family Only)

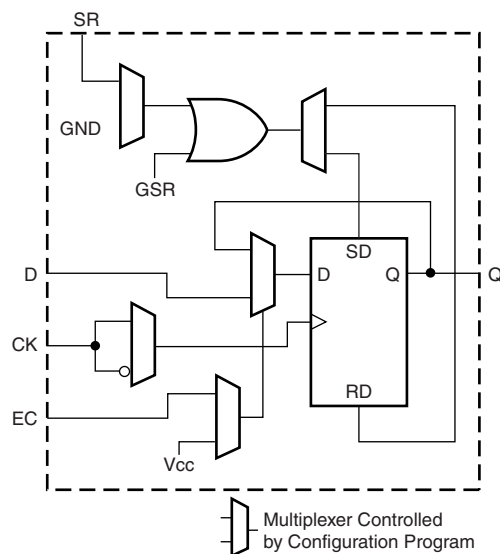
The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in [Table 2](#).

Table 2: CLB Storage Element Functionality

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
		1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (Spartan-XL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

**Legend:**

- X Don't care
-  Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0\* Input is Low or unconnected (default value)
- 1\* Input is High or unconnected (default value)



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Figure 3: CLB Flip-Flop Functional Block Diagram

## Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

## Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

## Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

## CLB Signal Flow Control

In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2, page 4) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinational CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinational output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

## Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1-C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

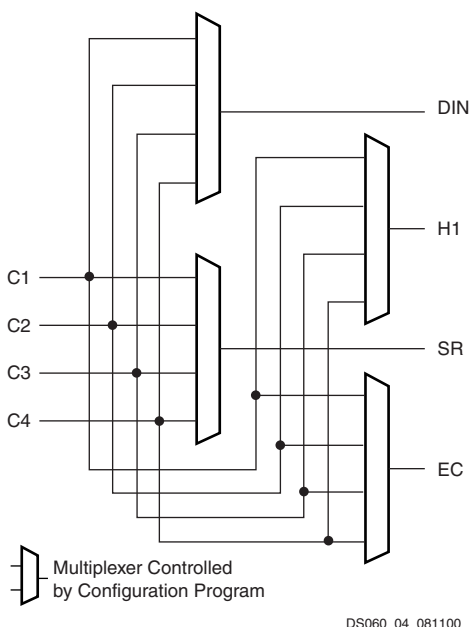


Figure 4: CLB Control Signal Interface

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

## Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

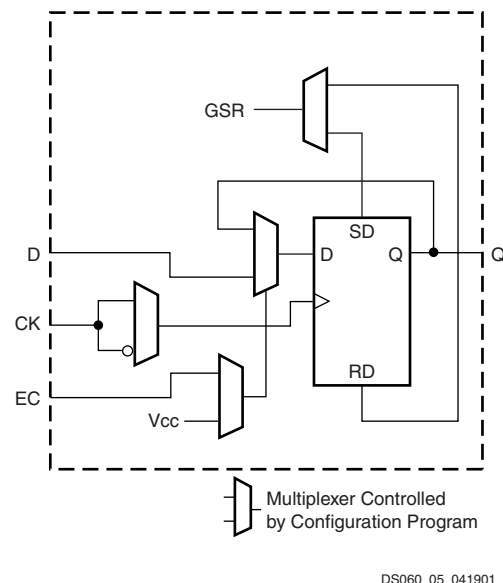


Figure 5: IOB Flip-Flop/Latch Functional Block Diagram

## IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: Input Register Functionality

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop		1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

### Legend:

- X Don't care.
- Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0\* Input is Low or unconnected (default value)
- 1\* Input is High or unconnected (default value)

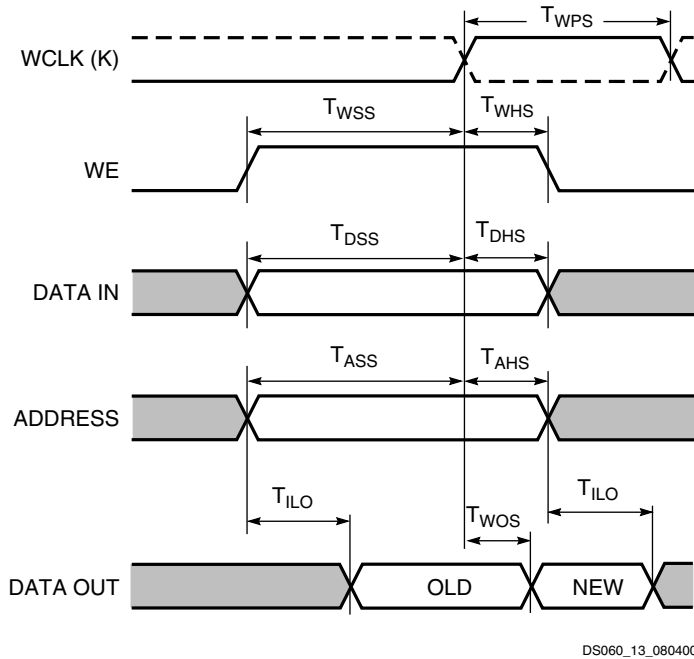


Figure 13: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be

inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay  $T_{ILO}$ , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay  $T_{WOS}$ , the new data will appear on SPO.

### Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by  $A[3:0]$  while the second provides only for read operations at the address specified independently by  $DPRA[3:0]$ . As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the

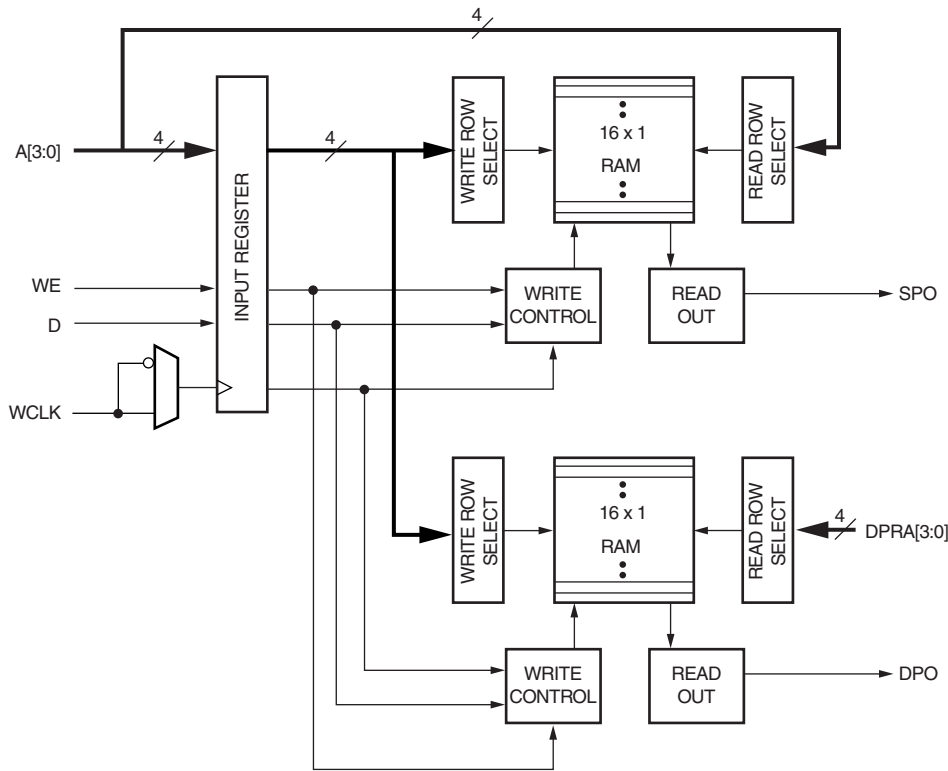
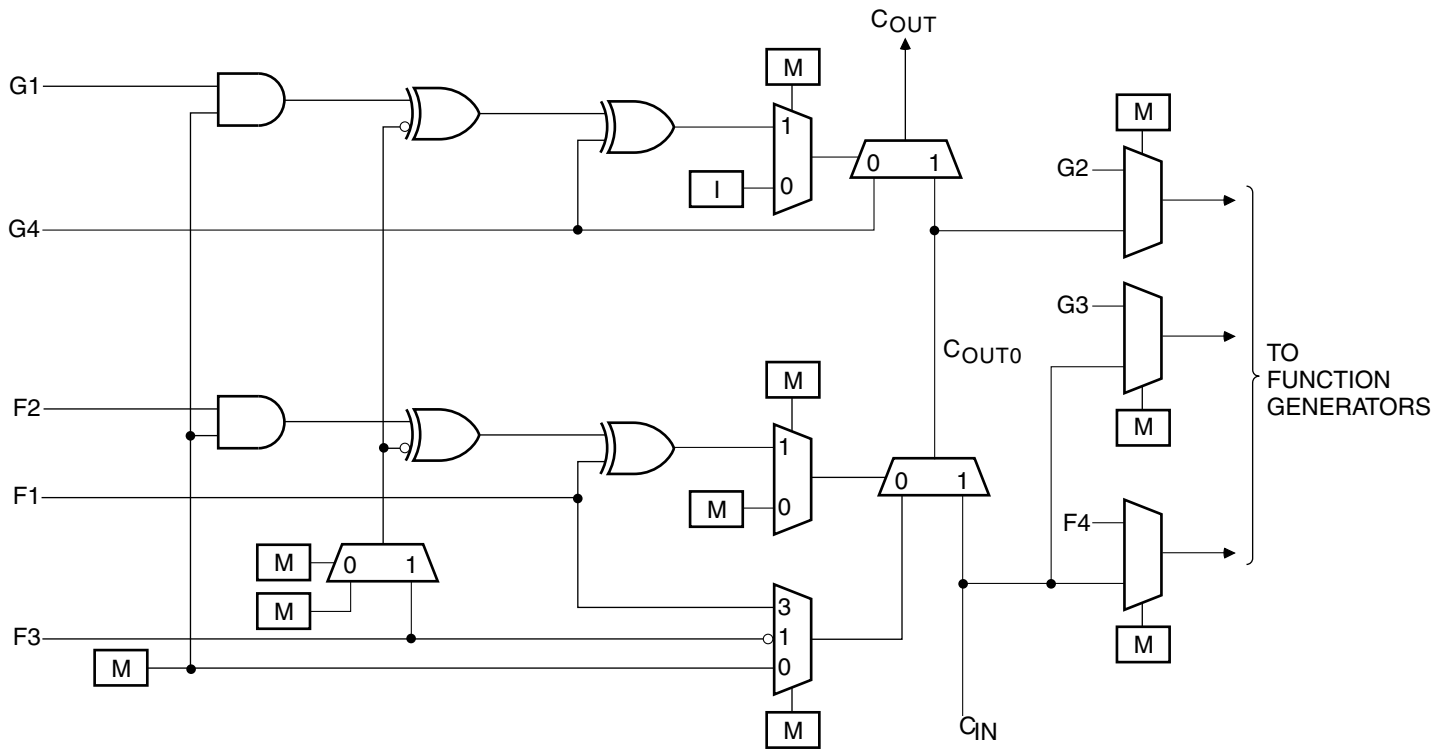


Figure 14: Logic Diagram for the Dual-Port RAM



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Figure 17: Detail of Spartan/XL Dedicated Carry Logic

### 3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

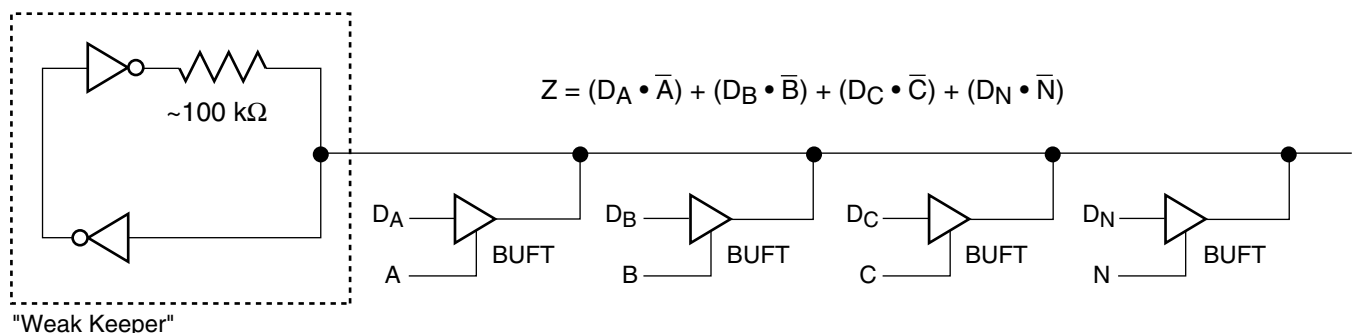
### Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

Table 11: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN



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Figure 18: 3-state Buffers Implement a Multiplexer



Even if the boundary scan symbol is used in a design, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

### Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state.
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "Boundary Scan in FPGA Devices."

### Boundary Scan Enhancements (Spartan-XL Family Only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

**IDCODE:** The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

c = the company code (49h for Xilinx)

a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)

f = the family code (02h for Spartan-XL family)

v = the die version number

Table 13: IDCODEs Assigned to Spartan-XL FPGAs

FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

**Configuration State:** The configuration state is available to JTAG controllers.

**Configuration Disable:** The JTAG port can be prevented from configuring the FPGA.

**TCK Startup:** TCK can now be used to clock the start-up block in addition to other user clocks.

**CCLK Holdoff:** Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

**Reissue Configure:** The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

**Bypass FF:** Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

### Power-Down (Spartan-XL Family Only)

All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low power-down pin (PWRDWN) to reduce supply current to 100  $\mu$ A typical. The PWRDWN pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The PWRDWN pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

$V_{CC}$  must continue to be supplied during Power-down, and configuration data is maintained. When the PWRDWN pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The PROGRAM pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

PWRDWN has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before PWRDWN to affect the order of events. When the PWRDWN signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of PWRDWN before using the device.



Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

## Serial Daisy Chain

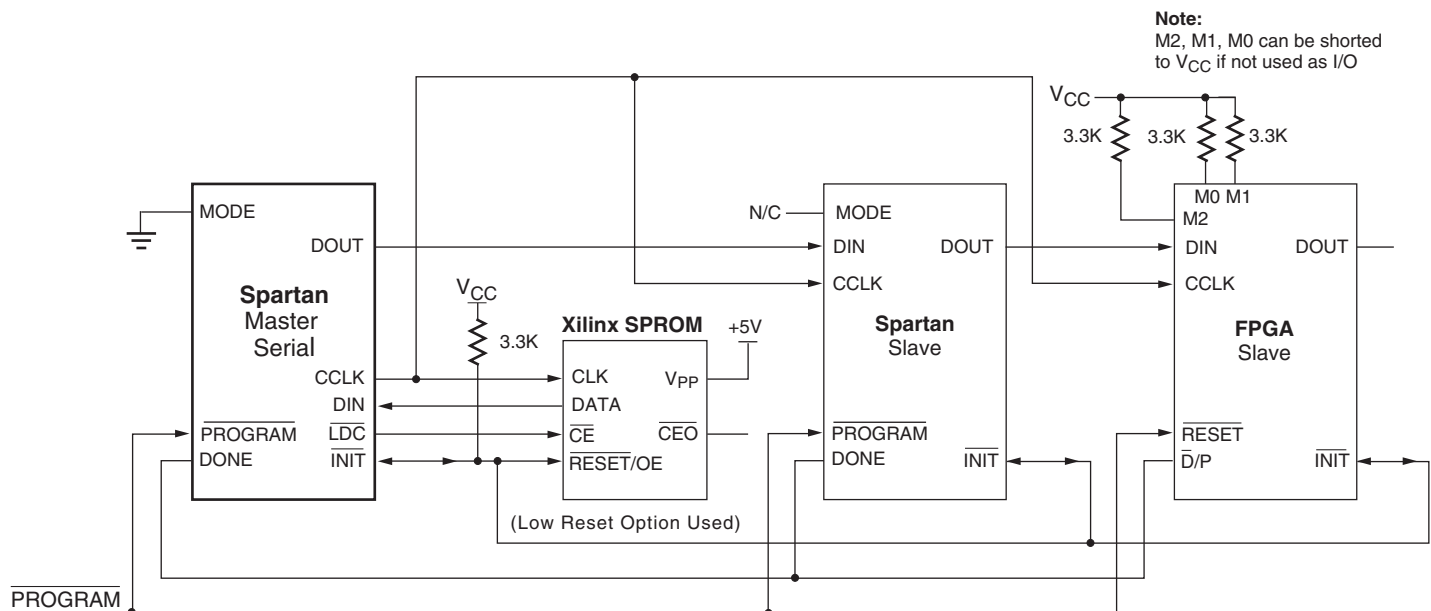
Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through

and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

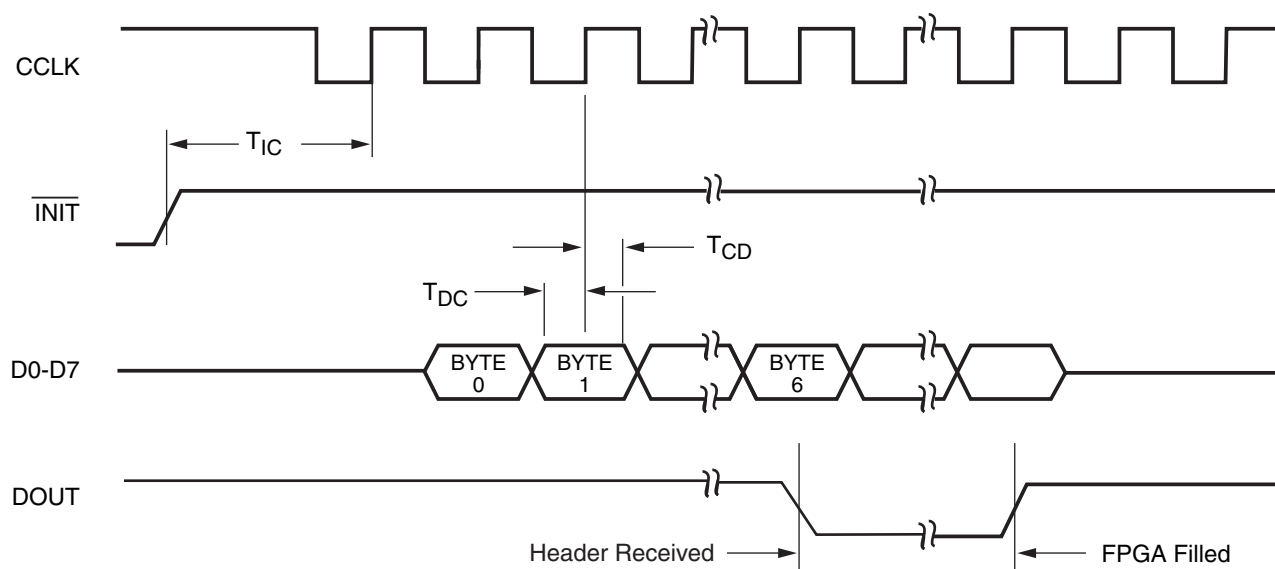
After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.



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Figure 25: Master/Slave Serial Mode Circuit Diagram



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Symbol		Description	Min	Max	Units
$T_{IC}$	CCLK	$\overline{INIT}$ (High) setup time	5	-	$\mu s$
$T_{DC}$		D0-D7 setup time	20	-	ns
$T_{CD}$		D0-D7 hold time	0	-	ns
$T_{CCH}$		CCLK High time	45	-	ns
$T_{CCL}$		CCLK Low time	45	-	ns
$F_{CC}$		CCLK Frequency	-	10	MHz

**Notes:**

1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: Express Mode Programming Switching Characteristics

## Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

## Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right.

Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

Table 17: Spartan/XL Program Data

Device	XCS05		XCS10		XCS20		XCS30		XCS40	
Max System Gates	5,000		10,000		20,000		30,000		40,000	
CLBs (Row x Col.)	100 (10 x 10)		196 (14 x 14)		400 (20 x 20)		576 (24 x 24)		784 (28 x 28)	
I/Os	80		112		160		192		205 <sup>(4)</sup>	
Part Number	XCS05	XCS05XL	XCS10	XCS10XL	XCS20	XCS20XL	XCS30	XCS30XL	XCS40	XCS40XL
Supply Voltage	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V
Bits per Frame	126	127	166	167	226	227	266	267	306	307
Frames	428	429	572	573	788	789	932	933	1,076	1,077
Program Data	53,936	54,491	94,960	95,699	178,096	179,111	247,920	249,119	329,264	330,647
PROM Size (bits)	53,984	54,544	95,008	95,752	178,144	179,160	247,968	249,168	329,312	330,696
Express Mode PROM Size (bits)	-	79,072	-	128,488	-	221,056	-	298,696	-	387,856

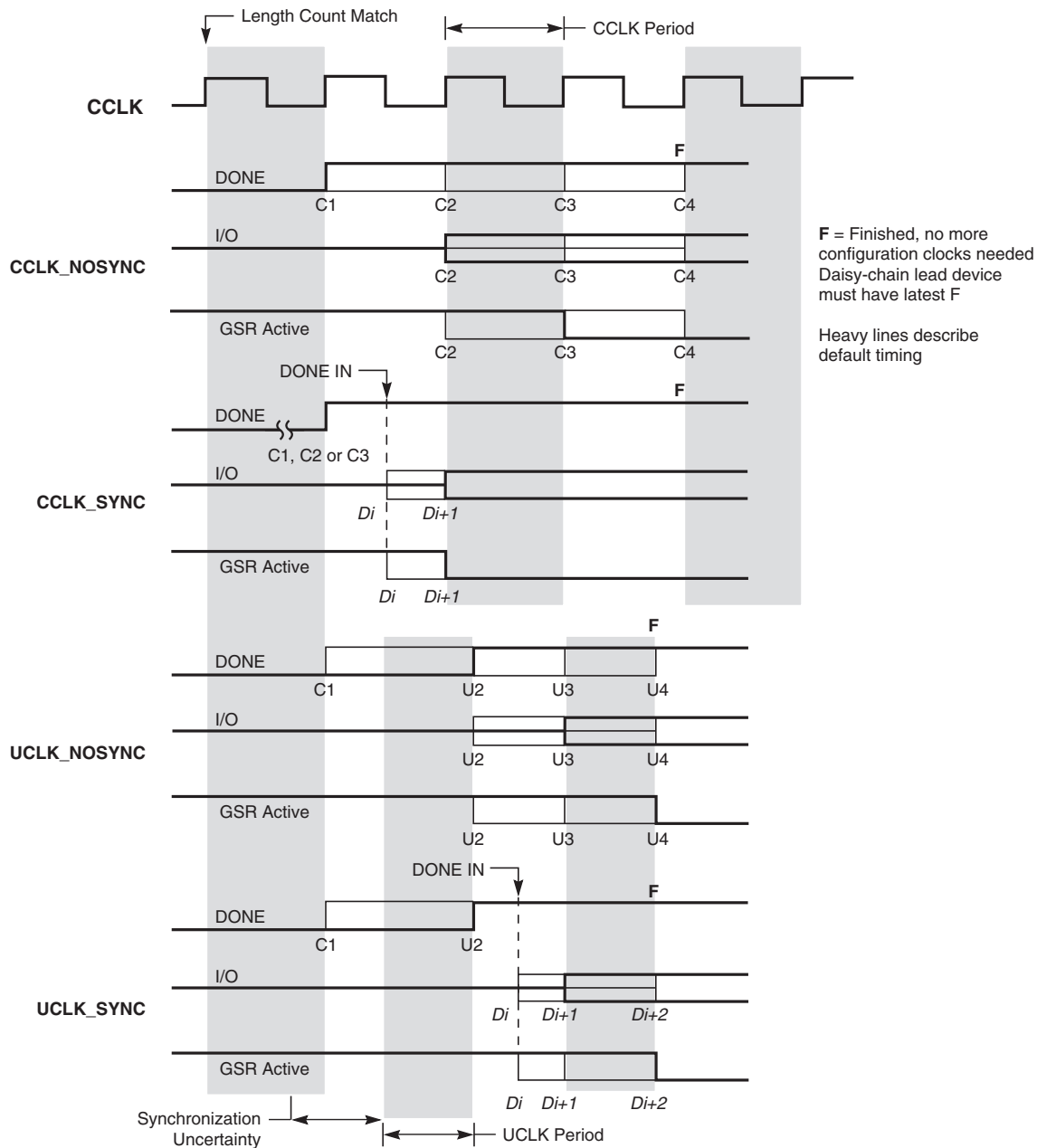
### Notes:

- Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits (+1 for Spartan-XL device)  
 Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1 (+ 1 for Spartan-XL device)  
 Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits  
 PROM Size = Program Data + 40 (header) + 8, rounded up to the nearest byte
- The user can add more "1" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.
- Express mode adds 57 (XCS05XL, XCS10XL), or 53 (XCS20XL, XCS30XL, XCS40XL) bits per frame, + additional start-up bits.
- XCS40XL provided 224 max I/O in CS280 package discontinued by [PDN2004-01](#).

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in [Figure 29](#). The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback

data is independent of the current device state. CLB outputs should not be included (Readback Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.



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Figure 31: Start-up Timing

## Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with  $\overline{\text{INIT}}$  held Low (or drive the PROGRAM pin Low for more than 300 ns followed by a High while holding  $\overline{\text{INIT}}$  Low). Holding  $\overline{\text{INIT}}$  Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold  $\overline{\text{INIT}}$  Low.
- Issue the CONFIG command to the TMS input.

- Wait for  $\overline{\text{INIT}}$  to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after  $\overline{\text{INIT}}$  goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "Boundary Scan in FPGA Devices." This application note applies to Spartan and Spartan-XL devices.

### Spartan Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0$ mA, $V_{CC}$ min	TTL outputs	2.4	-	V
	High-level output voltage @ $I_{OH} = -1.0$ mA, $V_{CC}$ min	CMOS outputs	$V_{CC} - 0.5$	-	V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0$ mA, $V_{CC}$ min <sup>(1)</sup>	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
$V_{DR}$	Data retention supply voltage (below which configuration data may be lost)		3.0	-	V
$I_{CCO}$	Quiescent FPGA supply current <sup>(2)</sup>	Commercial	-	3.0	mA
		Industrial	-	6.0	mA
$I_L$	Input or output leakage current		-10	+10	$\mu$ A
$C_{IN}$	Input capacitance (sample tested)		-	10	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{IN} = 0$ V (sample tested)		0.02	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{IN} = 5$ V (sample tested)		0.02	-	mA

#### Notes:

1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input pull-up resistors, all package pins at  $V_{CC}$  or GND, and the FPGA configured with a Tie option.

### Spartan Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For

more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
$T_{PG}$	From pad through Primary buffer, to any clock K	XCS05	2.0	4.0	ns
		XCS10	2.4	4.3	ns
		XCS20	2.8	5.4	ns
		XCS30	3.2	5.8	ns
		XCS40	3.5	6.4	ns
$T_{SG}$	From pad through Secondary buffer, to any clock K	XCS05	2.5	4.4	ns
		XCS10	2.9	4.7	ns
		XCS20	3.3	5.8	ns
		XCS30	3.6	6.2	ns
		XCS40	3.9	6.7	ns

### Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Typ.	Max	Units
V <sub>OH</sub>	High-level output voltage @ I <sub>OH</sub> = −4.0 mA, V <sub>CC</sub> min (LVTTL)		2.4	-	-	V
	High-level output voltage @ I <sub>OH</sub> = −500 μA, (LVCMOS)		90% V <sub>CC</sub>	-	-	V
V <sub>OL</sub>	Low-level output voltage @ I <sub>OL</sub> = 12.0 mA, V <sub>CC</sub> min (LVTTL) <sup>(1)</sup>		-	-	0.4	V
	Low-level output voltage @ I <sub>OL</sub> = 24.0 mA, V <sub>CC</sub> min (LVTTL) <sup>(2)</sup>		-	-	0.4	V
	Low-level output voltage @ I <sub>OL</sub> = 1500 μA, (LVCMOS)		-	-	10% V <sub>CC</sub>	V
V <sub>DR</sub>	Data retention supply voltage (below which configuration data may be lost)		2.5	-	-	V
I <sub>CCO</sub>	Quiescent FPGA supply current <sup>(3,4)</sup>	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I <sub>CCPD</sub>	Power Down FPGA supply current <sup>(3,5)</sup>	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I <sub>L</sub>	Input or output leakage current		−10	-	10	μA
C <sub>IN</sub>	Input capacitance (sample tested)		-	-	10	pF
I <sub>RPU</sub>	Pad pull-up (when selected) @ V <sub>IN</sub> = 0V (sample tested)		0.02	-	0.25	mA
I <sub>RPD</sub>	Pad pull-down (when selected) @ V <sub>IN</sub> = 3.3V (sample tested)		0.02	-	-	mA

#### Notes:

1. With up to 64 pins simultaneously sinking 12 mA (default mode).
2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
4. With no output current loads, no active input resistors, and all package pins at  $V_{CC}$  or GND.
5. With  $\overline{PWRDWN}$  active.

### Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current  $I_{CCPO}$  be provided to the  $V_{CC}$  lines for a successful power on. If more current is available, the FPGA can consume more than  $I_{CCPO}$  min., though this cannot adversely affect reliability.

A maximum limit for  $I_{CCPO}$  is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of  $I_{CCPO}$  by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Max	Units
$I_{CCPO}$	Total $V_{CC}$ supply current required during power-on	100	-	mA
$T_{CCPO}$	$V_{CC}$ ramp time <sup>(2,3)</sup>	-	50	ms

#### Notes:

1. The  $I_{CCPO}$  requirement applies for a brief time (commonly only a few milliseconds) when  $V_{CC}$  ramps from 0 to 3.3V.
2. The ramp time is measured from GND to  $V_{CC}$  max on a fully loaded board.
3.  $V_{CC}$  must not dip in the negative direction during power on.

## Spartan-XL Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case oper-

ating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

### Spartan-XL Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-5	-4	
			Max	Max	
Global Clock to Output using OFF					
T <sub>ICKOF</sub>	Fast	XCS05XL	4.6	5.2	ns
		XCS10XL	4.9	5.5	ns
		XCS20XL	5.2	5.8	ns
		XCS30XL	5.5	6.2	ns
		XCS40XL	5.8	6.5	ns
Slew Rate Adjustment					
T <sub>SLOW</sub>	For Output SLOW option add	All Devices	1.5	1.7	ns

#### Notes:

1. Output delays are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V<sub>CC</sub> threshold with 50 pF external capacitive load.
3. OFF = Output Flip Flop



## Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol		Device	Speed Grade				Units
			-5		-4		
	Description		Min	Max	Min	Max	
Setup Times							
T <sub>ECIK</sub>	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T <sub>PICK</sub>	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T <sub>POCK</sub>	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T <sub>PID</sub>	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T <sub>PLI</sub>	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T <sub>IKRI</sub>	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T <sub>IKLI</sub>	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T <sub>Delay</sub>	T <sub>PICKD</sub> = T <sub>PICK</sub> + T <sub>Delay</sub> T <sub>PDLI</sub> = T <sub>PLI</sub> + T <sub>Delay</sub>	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T <sub>MRW</sub>	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T <sub>RRI</sub>	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

### Notes:

- Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
- Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	<p>Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin.</p> <p>The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.</p>
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	<p>Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin.</p> <p>The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.</p>
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	<p>During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input.</p> <p>In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices.</p> <p>After configuration, DOUT is a user-programmable I/O pin.</p>
<b>Unrestricted User-Programmable I/O Pins</b>			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

### XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 <sup>(2,4)</sup>	TQ144	PQ208	Bndry Scan
I/O	-	F4	P13	P21	170
I/O	P8	F3	P14	P22	173
I/O	P9	F2	P15	P23	176
I/O	P10	F1	P16	P24	179
GND	P11	G2	P17	P25	-
VCC	P12	G1	P18	P26	-
I/O	P13	G3	P19	P27	182
I/O	P14	G4	P20	P28	185
I/O	P15	H1	P21	P29	188
I/O	-	H2	P22	P30	191
I/O	-	-	-	P31	194
I/O	-	-	-	P32	197
VCC <sup>(2)</sup>	-	-	-	P33	-
I/O	P16	H3	P23	P34	200
I/O	P17	H4	P24	P35	203
I/O	-	J1	P25	P36	206
I/O	-	J2	P26	P37	209
GND	-	J3	P27	P38	-
I/O	-	-	-	P40	212
I/O	-	-	-	P41	215
I/O	-	-	-	P42	218
I/O	-	-	-	P43	221
I/O	P18	J4	P28	P44	224
I/O	P19	K1	P29	P45	227
I/O	-	K2	P30	P46	230
I/O	-	K3	P31	P47	233
I/O	P20	L1	P32	P48	236
I/O, SGCK2 <sup>(1)</sup> , GCK2 <sup>(2)</sup>	P21	L2	P33	P49	239
Not Connected <sup>(1)</sup> M1 <sup>(2)</sup>	P22	L3	P34	P50	242
GND	P23	M1	P35	P51	-
MODE <sup>(1)</sup> , M0 <sup>(2)</sup>	P24	M2	P36	P52	245
VCC	P25	N1	P37	P53	-
Not Connected <sup>(1)</sup> PWRDWN <sup>(2)</sup>	P26	N2	P38	P54	246 <sup>(1)</sup>
I/O, PGCK2 <sup>(1)</sup> , GCK3 <sup>(2)</sup>	P27	M3	P39	P55	247 <sup>(3)</sup>
I/O (HDC)	P28	N3	P40	P56	250 <sup>(3)</sup>
I/O	-	K4	P41	P57	253 <sup>(3)</sup>
I/O	-	L4	P42	P58	256 <sup>(3)</sup>
I/O	P29	M4	P43	P59	259 <sup>(3)</sup>

### XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144 <sup>(2,4)</sup>	TQ144	PQ208	Bndry Scan
I/O (LDC)	P30	N4	P44	P60	262 <sup>(3)</sup>
I/O	-	-	-	P61	265 <sup>(3)</sup>
I/O	-	-	-	P62	268 <sup>(3)</sup>
I/O	-	-	-	P63	271 <sup>(3)</sup>
I/O	-	-	-	P64	274 <sup>(3)</sup>
GND	-	K5	P45	P66	-
I/O	-	L5	P46	P67	277 <sup>(3)</sup>
I/O	-	M5	P47	P68	280 <sup>(3)</sup>
I/O	P31	N5	P48	P69	283 <sup>(3)</sup>
I/O	P32	K6	P49	P70	286 <sup>(3)</sup>
VCC <sup>(2)</sup>	-	-	-	P71	-
I/O	-	-	-	P72	289 <sup>(3)</sup>
I/O	-	-	-	P73	292 <sup>(3)</sup>
I/O	P33	L6	P50	P74	295 <sup>(3)</sup>
I/O	P34	M6	P51	P75	298 <sup>(3)</sup>
I/O	P35	N6	P52	P76	301 <sup>(3)</sup>
I/O (INIT)	P36	M7	P53	P77	304 <sup>(3)</sup>
VCC	P37	N7	P54	P78	-
GND	P38	L7	P55	P79	-
I/O	P39	K7	P56	P80	307 <sup>(3)</sup>
I/O	P40	N8	P57	P81	310 <sup>(3)</sup>
I/O	P41	M8	P58	P82	313 <sup>(3)</sup>
I/O	P42	L8	P59	P83	316 <sup>(3)</sup>
I/O	-	-	-	P84	319 <sup>(3)</sup>
I/O	-	-	-	P85	322 <sup>(3)</sup>
VCC <sup>(2)</sup>	-	-	-	P86	-
I/O	P43	K8	P60	P87	325 <sup>(3)</sup>
I/O	P44	N9	P61	P88	328 <sup>(3)</sup>
I/O	-	M9	P62	P89	331 <sup>(3)</sup>
I/O	-	L9	P63	P90	334 <sup>(3)</sup>
GND	-	K9	P64	P91	-
I/O	-	-	-	P93	337 <sup>(3)</sup>
I/O	-	-	-	P94	340 <sup>(3)</sup>
I/O	-	-	-	P95	343 <sup>(3)</sup>
I/O	-	-	-	P96	346 <sup>(3)</sup>
I/O	P45	N10	P65	P97	349 <sup>(3)</sup>
I/O	P46	M10	P66	P98	352 <sup>(3)</sup>
I/O	-	L10	P67	P99	355 <sup>(3)</sup>
I/O	-	N11	P68	P100	358 <sup>(3)</sup>
I/O	P47	M11	P69	P101	361 <sup>(3)</sup>
I/O, SGCK3 <sup>(1)</sup> , GCK4 <sup>(2)</sup>	P48	L11	P70	P102	364 <sup>(3)</sup>
GND	P49	N12	P71	P103	-
DONE	P50	M12	P72	P104	-
VCC	P51	N13	P73	P105	-

### XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 <sup>(5)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(5)</sup>	CS280 <sup>(2,5)</sup>	Bndry Scan
I/O	P18	P28	P44	P52	V1	T1	272
I/O	P19	P29	P45	P53	T4	T2	275
I/O	-	P30	P46	P54	U3	T3	278
I/O	-	P31	P47	P55	V2	U1	281
I/O	P20	P32	P48	P56	W1	V1	284
I/O, SGCK2 <sup>(1)</sup> , GCK2 <sup>(2)</sup>	P21	P33	P49	P57	V3	U2	287
Not Connected <sup>(1)</sup> , M1 <sup>(2)</sup>	P22	P34	P50	P58	W2	V2	290
GND	P23	P35	P51	P59	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
MODE <sup>(1)</sup> , M0 <sup>(2)</sup>	P24	P36	P52	P60	Y1	W1	293
VCC	P25	P37	P53	P61	VCC <sup>(4)</sup>	U3	-
Not Connected <sup>(1)</sup> , PWRDWN <sup>(2)</sup>	P26	P38	P54	P62	W3	V3	294 <sup>(1)</sup>
I/O, PGCK2 <sup>(1)</sup> , GCK3 <sup>(2)</sup>	P27	P39	P55	P63	Y2	W2	295 <sup>(3)</sup>
I/O (HDC)	P28	P40	P56	P64	W4	W3	298 <sup>(3)</sup>
I/O	-	P41	P57	P65	V4	T4	301 <sup>(3)</sup>
I/O	-	P42	P58	P66	U5	U4	304 <sup>(3)</sup>
I/O	P29	P43	P59	P67	Y3	V4	307 <sup>(3)</sup>
I/O (LDC)	P30	P44	P60	P68	Y4	W4	310 <sup>(3)</sup>
I/O	-	-	P61	P69	V5	T5	313 <sup>(3)</sup>
I/O	-	-	P62	P70	W5	W5	316 <sup>(3)</sup>
I/O	-	-	P63	P71	Y5	R6	319 <sup>(3)</sup>
I/O	-	-	P64	P72	V6	U6	322 <sup>(3)</sup>
I/O	-	-	P65	P73	W6	V6	325 <sup>(3)</sup>
I/O	-	-	-	P74	Y6	T6	328 <sup>(3)</sup>
GND	-	P45	P66	P75	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	-	P46	P67	P76	W7	W6	331 <sup>(3)</sup>
I/O	-	P47	P68	P77	Y7	U7	334 <sup>(3)</sup>
I/O	P31	P48	P69	P78	V8	V7	337 <sup>(3)</sup>
I/O	P32	P49	P70	P79	W8	W7	340 <sup>(3)</sup>
VCC	-	-	P71	P80	VCC <sup>(4)</sup>	T7	-
I/O	-	-	P72	P81	Y8	W8	343 <sup>(3)</sup>
I/O	-	-	P73	P82	U9	U8	346 <sup>(3)</sup>
I/O	-	-	-	P84	Y9	W9	349 <sup>(3)</sup>
I/O	-	-	-	P85	W10	V9	352 <sup>(3)</sup>
I/O	P33	P50	P74	P86	V10	U9	355 <sup>(3)</sup>
I/O	P34	P51	P75	P87	Y10	T9	358 <sup>(3)</sup>
I/O	P35	P52	P76	P88	Y11	W10	361 <sup>(3)</sup>
I/O (INIT)	P36	P53	P77	P89	W11	V10	364 <sup>(3)</sup>
VCC	P37	P54	P78	P90	VCC <sup>(4)</sup>	U10	-
GND	P38	P55	P79	P91	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	P39	P56	P80	P92	V11	T10	367 <sup>(3)</sup>
I/O	P40	P57	P81	P93	U11	R10	370 <sup>(3)</sup>
I/O	P41	P58	P82	P94	Y12	W11	373 <sup>(3)</sup>
I/O	P42	P59	P83	P95	W12	V11	376 <sup>(3)</sup>
I/O	-	-	P84	P96	V12	U11	379 <sup>(3)</sup>

## XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 <sup>(5)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(5)</sup>	CS280 <sup>(2,5)</sup>	Bndry Scan
I/O	-	-	-	P190	B16	A15	23
I/O	-	P117	P166	P191	A16	E14	26
I/O	-	-	P167	P192	C15	C14	29
I/O	-	-	P168	P193	B15	B14	32
I/O	-	-	P169	P194	A15	D14	35
GND	-	P118	P170	P196	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-
I/O	-	P119	P171	P197	B14	A14	38
I/O	-	P120	P172	P198	A14	C13	41
I/O	-	-	-	P199	C13	B13	44
I/O	-	-	-	P200	B13	A13	47
VCC	-	-	P173	P201	VCC <sup>(4)</sup>	D13	-
I/O	P82	P121	P174	P202	C12	B12	50
I/O	P83	P122	P175	P203	B12	D12	53
I/O	-	-	P176	P205	A12	A11	56
I/O	-	-	P177	P206	B11	B11	59
I/O	P84	P123	P178	P207	C11	C11	62
I/O	P85	P124	P179	P208	A11	D11	65
I/O	P86	P125	P180	P209	A10	A10	68
I/O	P87	P126	P181	P210	B10	B10	71
GND	P88	P127	P182	P211	GND <sup>(4)</sup>	GND <sup>(4)</sup>	-

2/8/00

### Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).
4. Pads labeled GND<sup>(4)</sup> or VCC<sup>(4)</sup> are internally bonded to Ground or VCC planes within the package.
5. CS280 package, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)

### Additional XCS30/XL Package Pins

#### PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

2/12/98

#### BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

#### GND Pins

A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

6/4/97

#### CS280

VCC Pins					
A1	A7	C10	C17	D13	G1
G1	G19	K2	K17	M4	N16
T7	U3	U10	U17	W13	-
GND Pins					

### Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: Component Availability Chart for Spartan/XL FPGAs

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84 <sup>(3)</sup>	VQ100 <sup>(3)</sup>	CS144 <sup>(3)</sup>	TQ144	PQ208	PQ240	BG256 <sup>(3)</sup>	CS280 <sup>(3)</sup>
XCS05	-3	C <sup>(3)</sup>	C, I	-	-	-	-	-	-
	-4	C <sup>(3)</sup>	C	-	-	-	-	-	-
XCS10	-3	C <sup>(3)</sup>	C, I	-	C	-	-	-	-
	-4	C <sup>(3)</sup>	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C <sup>(3)</sup>	-	C, I	C, I	C	C <sup>(3)</sup>	-
	-4	-	C <sup>(3)</sup>	-	C	C	C	C <sup>(3)</sup>	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C <sup>(3)</sup>	C, I	-	-	-	-	-	-
	-5	C <sup>(3)</sup>	C	-	-	-	-	-	-
XCS10XL	-4	C <sup>(3)</sup>	C, I	C <sup>(3)</sup>	C	-	-	-	-
	-5	C <sup>(3)</sup>	C	C <sup>(3)</sup>	C	-	-	-	-
XCS20XL	-4	-	C, I	C <sup>(3)</sup>	C, I	C, I	-	-	-
	-5	-	C	C <sup>(3)</sup>	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C <sup>(3)</sup>
	-5	-	C	-	C	C	C	C	C <sup>(3)</sup>
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C <sup>(3)</sup>
	-5	-	-	-	-	C	C	C	C <sup>(3)</sup>

6/25/08

#### Notes:

1. C = Commercial  $T_J = 0^\circ$  to  $+85^\circ\text{C}$
2. I = Industrial  $T_J = -40^\circ\text{C}$  to  $+100^\circ\text{C}$
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

### Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

[www.xilinx.com/support/documentation/spartan-xl.htm#19687](http://www.xilinx.com/support/documentation/spartan-xl.htm#19687)

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

[www.xilinx.com/cgi-bin/thermal/thermal.pl](http://www.xilinx.com/cgi-bin/thermal/thermal.pl)