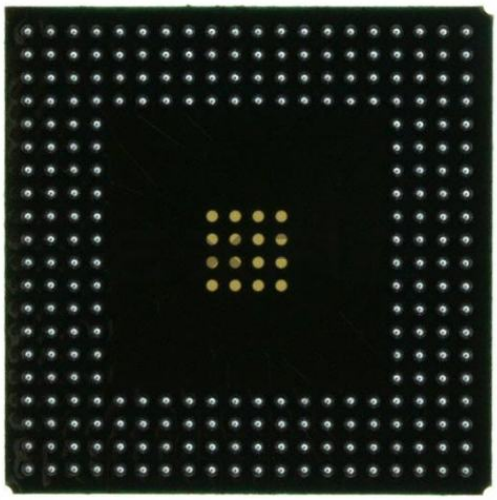

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	205
Number of Gates	40000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40xl-4bg256c

Spartan and Spartan-XL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In addition to the conventional benefit of high volume programmable logic solutions, Spartan series FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan/XL families leverage the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA process developments.

Logic Functional Description

The Spartan series uses a standard FPGA structure as shown in Figure 1, page 2. The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in Figure 2. There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the **Advanced Features Description**, page 13.

Function Generators

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box "A" of Figure 2). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.

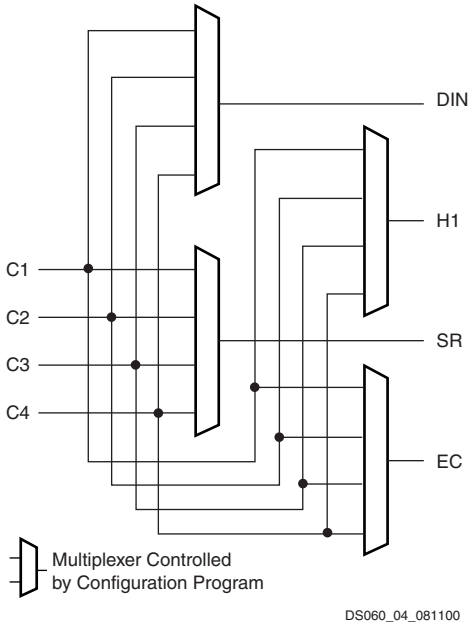


Figure 4: **CLB Control Signal Interface**

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

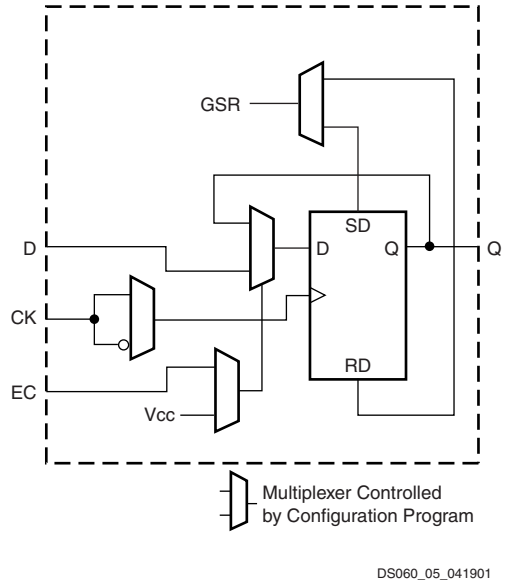


Figure 5: **IOB Flip-Flop/Latch Functional Block Diagram**

IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: **Input Register Functionality**

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	⌐	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care.
⌐	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Table 4: **Supported Sources for Spartan/XL Inputs**

Source	Spartan Inputs		Spartan-XL Inputs
	5V, TTL	5V, CMOS	3.3V CMOS
Any device, V_{CC} = 3.3V, CMOS outputs	√	Unreliable Data	√
Spartan family, V_{CC} = 5V, TTL outputs	√		√
Any device, V_{CC} = 5V, TTL outputs ($V_{OH} \leq 3.7V$)	√		√
Any device, V_{CC} = 5V, CMOS outputs	√	√	√ (default mode)

Spartan-XL Family V_{CC} Clamping

Spartan-XL FPGAs have an optional clamping diode connected from each I/O to V_{CC}. When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. V_{CC} clamping is a global option affecting all I/O pins.

Spartan-XL devices are fully 5V TTL I/O compatible if V_{CC} clamping is not enabled. With V_{CC} clamping enabled, the Spartan-XL devices will begin to clamp input voltages to one diode voltage drop above V_{CC}. If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

Spartan-XL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 5.

Table 5: **I/O Standards Supported by Spartan-XL FPGAs**

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}
LVCMOS 3V	OK	12/24 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}

Additional Fast Capture Input Latch (Spartan-XL Family Only)

The Spartan-XL family OB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active High input flip-flop. ILFLX is a transparent Low Fast Capture latch followed by a transparent High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 6.

Table 6: **Output Flip-Flop Functionality**

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	⌐	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
⌐	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

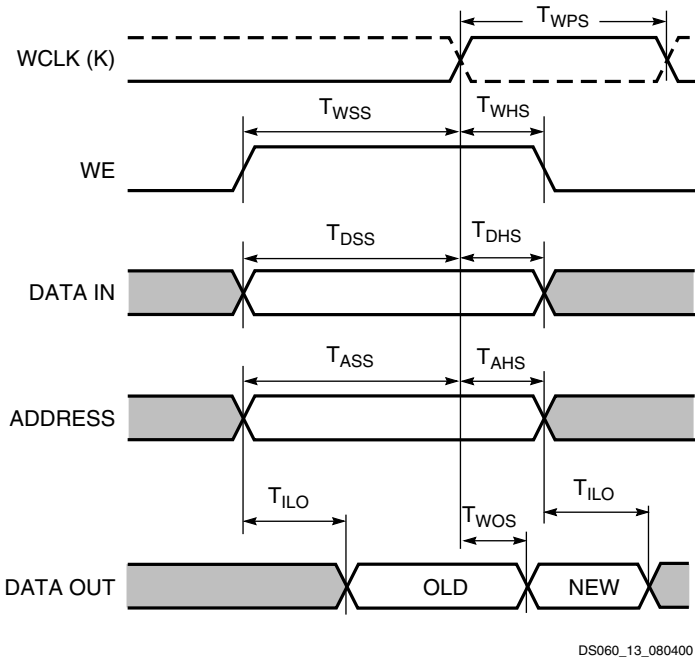


Figure 13: **Data Write and Access Timing for RAM**

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO}, the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS}, the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by A[3:0] while the second provides only for read operations at the address specified independently by DPRA[3:0]. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the

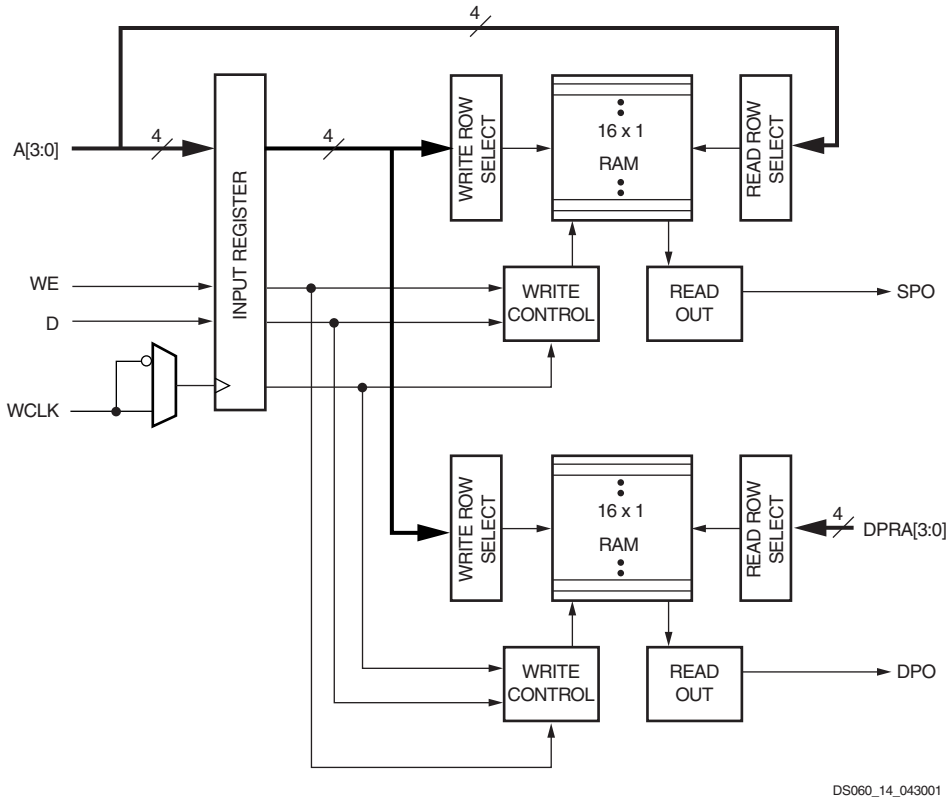


Figure 14: **Logic Diagram for the Dual-Port RAM**

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. $\overline{\text{PROGRAM}}$, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.

Table 12: **Boundary Scan Instructions**

Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	IDCODE (Spartan-XL only)	IDCODE Register	-
1	1	1	BYPASS	Bypass Register	-

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-state. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 21. The device-specific pinout tables for the Spartan/XL devices include the boundary scan locations for each IOB pin.

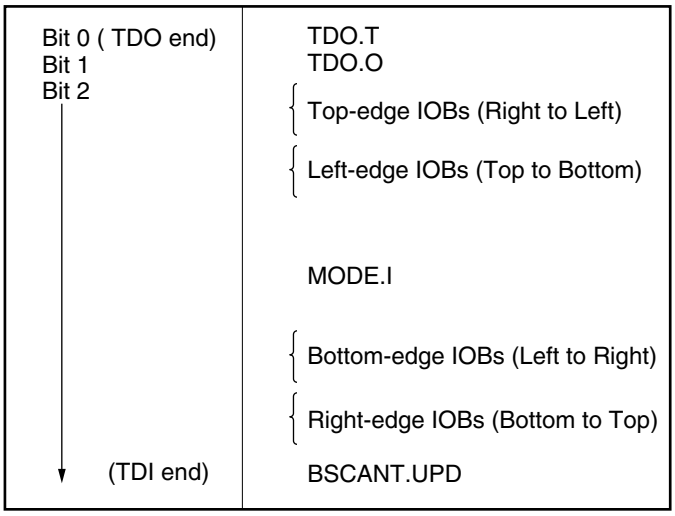


Figure 21: **Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Spartan/XL devices are available on the Xilinx website in the File Download area. Note that the 5V Spartan devices and 3V Spartan-XL devices have different BSDL files.

Including Boundary Scan in a Design

If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 22.

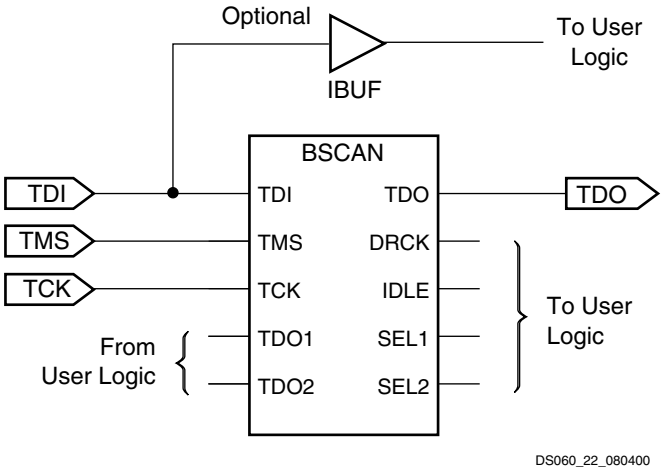
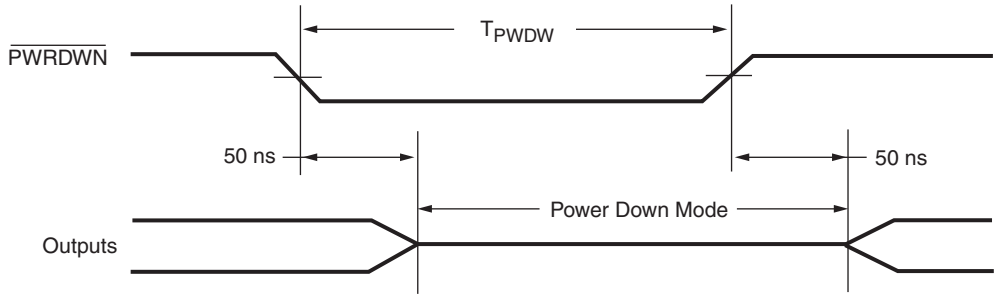


Figure 22: **Boundary Scan Example**



Description	Symbol	Min
Power Down Time	T_{PWD}	50 ns
Power Down Pulse Width	T_{PWDW}	50 ns

DS060_23_041901

Figure 23: **$\overline{\text{PWRDWN}}$ Pulse Timing**

Power-down retains the configuration, but loses all data stored in the device flip-flops. All inputs are interpreted as Low, but the internal combinatorial logic is fully functional. Make sure that the combination of all inputs Low and all flip-flops set or reset in your design will not generate internal oscillations, or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line.

During configuration, the $\overline{\text{PWRDWN}}$ pin must be High. If the Power Down state is entered before or during configuration, the device will restart configuration once the $\overline{\text{PWRDWN}}$ signal is removed. Note that the configuration pins are affected by Power Down and may not reflect their normal function. If there is an external pull-up resistor on the DONE pin, it will be High during Power Down even if the device is not yet configured. Similarly, if $\overline{\text{PWRDWN}}$ is asserted before configuration is completed, the $\overline{\text{INIT}}$ pin will not indicate status information.

Note that the $\overline{\text{PWRDWN}}$ pin is not part of the Boundary Scan chain. Therefore, the Spartan-XL family has a separate set of BSDL files than the 5V Spartan family. Boundary scan logic is not usable during Power Down.

Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan/XL devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Configuration Mode Control

5V Spartan devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

3V Spartan-XL devices have three configuration modes.

- M1/M0 = 11 sets Slave Serial mode
- M1/M0 = 10 sets Master Serial mode
- M1/M0 = 0X sets Express mode

In addition to these modes, the device can be configured through the Boundary Scan logic (See "Configuration Through the Boundary Scan Pins" on page 37.).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pin are unused. The Mode pins have a weak pull-up resistor turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the MODE/M0 pin should be connected directly to GND, or through a pull-down resistor of 1 KΩ or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during con-

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.

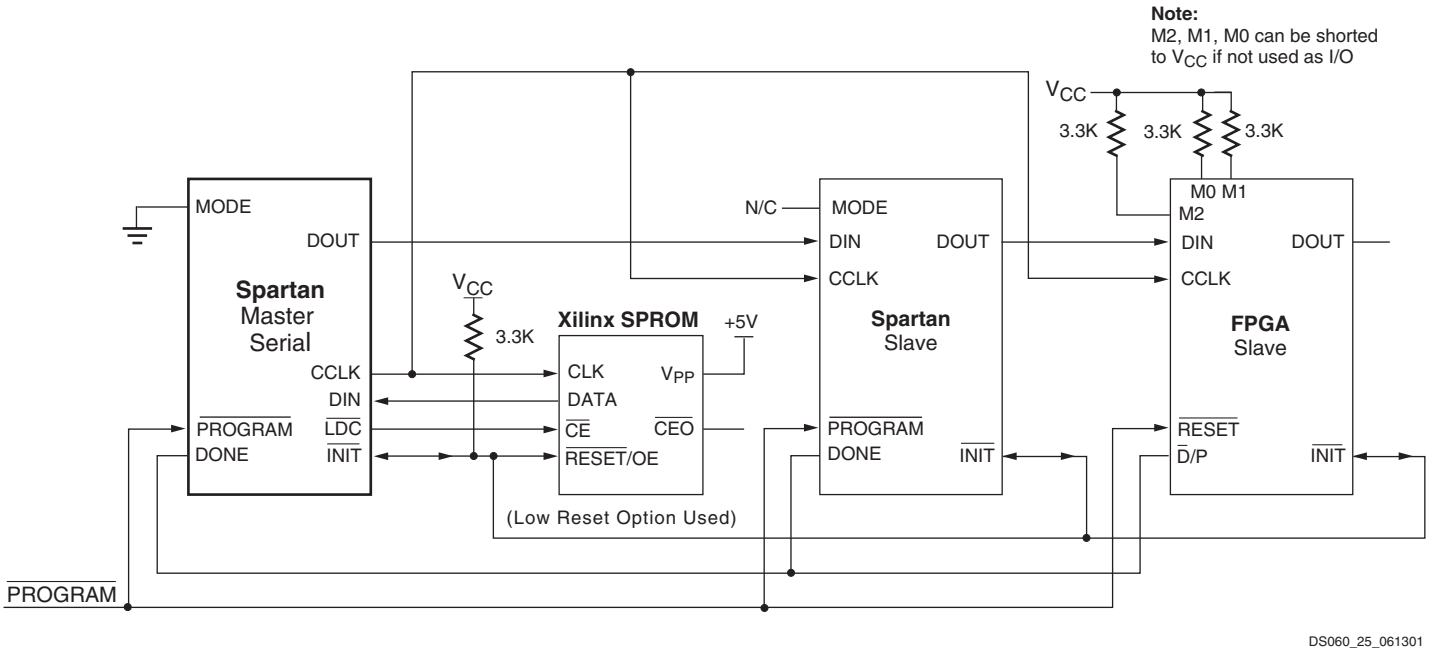


Figure 25: **Master/Slave Serial Mode Circuit Diagram**

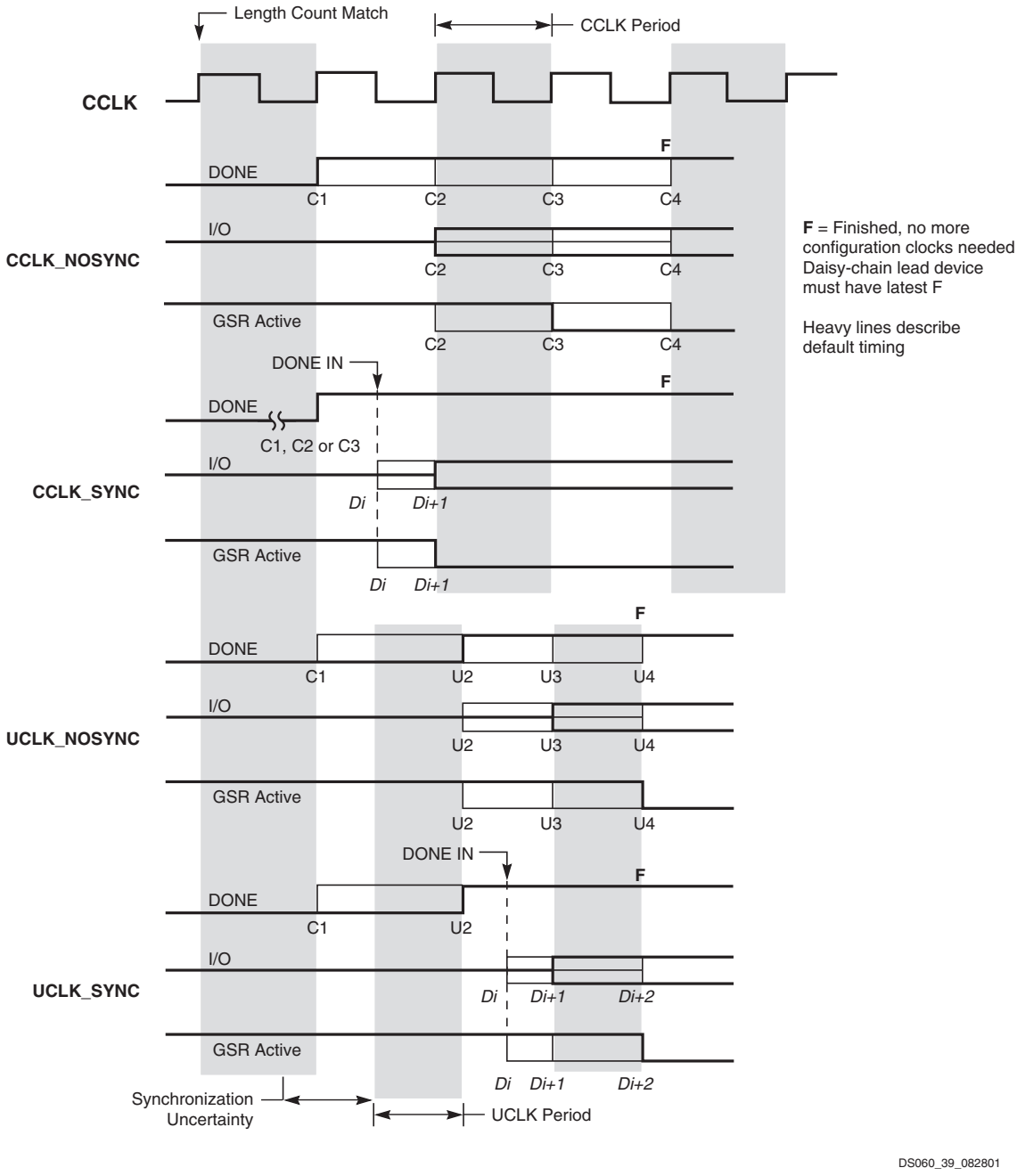


Figure 31: **Start-up Timing**

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input.
- Wait for $\overline{\text{INIT}}$ to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after $\overline{\text{INIT}}$ goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and Spartan-XL devices.

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 16 and Table 17.

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.

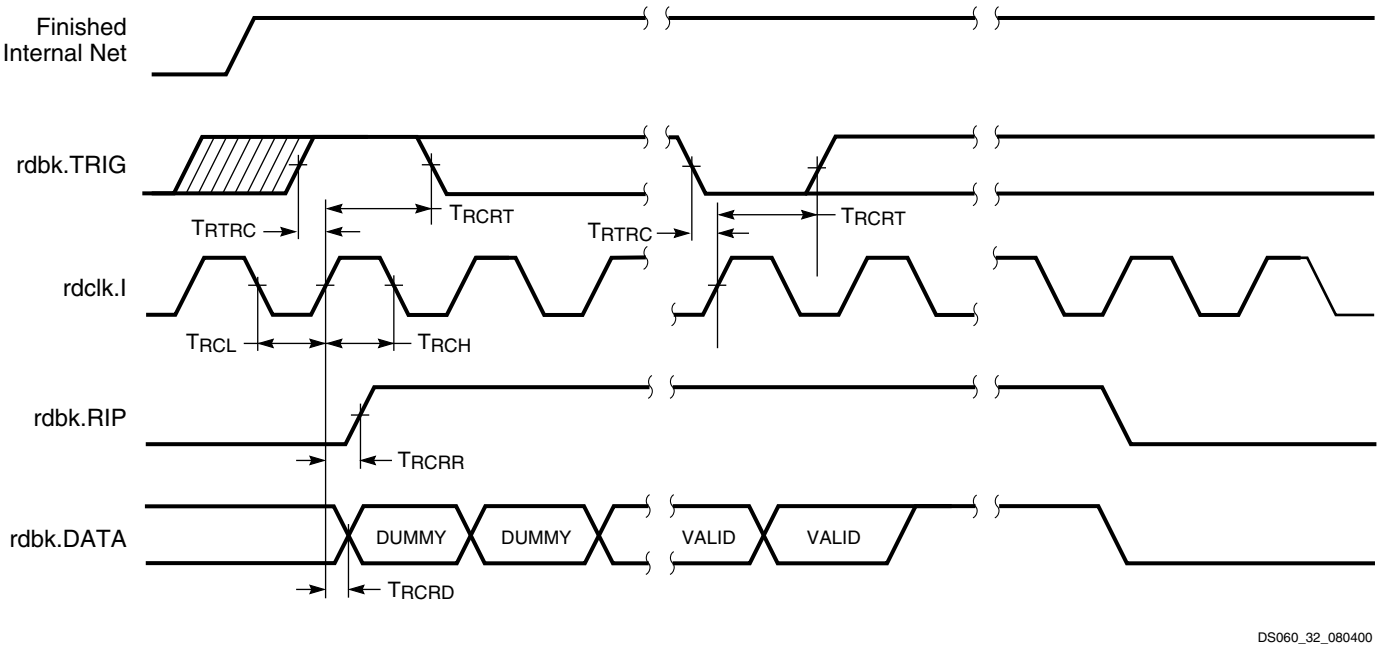


Figure 33: **Spartan and Spartan-XL Readback Timing Diagram**

Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:
1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

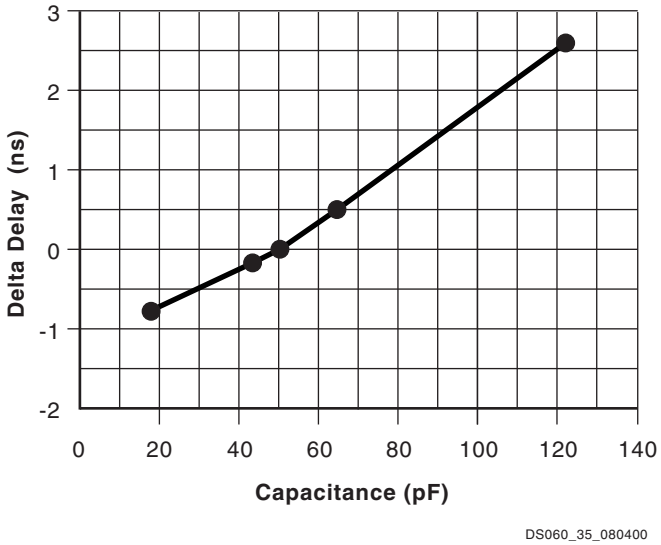


Figure 34: **Delay Factor at Various Capacitive Loads**

Spartan Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Setup Times - TTL Inputs(1)							
T_{ECIK}	Clock Enable (EC) to Clock (IK), no delay	All devices	1.6	-	2.1	-	ns
T_{PICK}	Pad to Clock (IK), no delay	All devices	1.5	-	2.0	-	ns
Hold Times							
T_{IKEC}	Clock Enable (EC) to Clock (IK), no delay	All devices	0.0	-	0.9	-	ns
	All Other Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays - TTL Inputs(1)							
T_{PID}	Pad to I1, I2	All devices	-	1.5	-	2.0	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.8	-	3.6	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	2.7	-	2.8	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	3.2	-	3.9	ns
Delay Adder for Input with Delay Option							
T_{Delay}	$T_{ECIKD} = T_{ECIK} + T_{Delay}$ $T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	XCS05	3.6	-	4.0	-	ns
		XCS10	3.7	-	4.1	-	ns
		XCS20	3.8	-	4.2	-	ns
		XCS30	4.5	-	5.0	-	ns
		XCS40	5.5	-	5.5	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	11.5	-	13.5	-	ns
T_{RRI}	Delay from GSR input to any Q	XCS05	-	9.0	-	11.3	ns
		XCS10	-	9.5	-	11.9	ns
		XCS20	-	10.0	-	12.5	ns
		XCS30	-	10.5	-	13.1	ns
		XCS40	-	11.0	-	13.8	ns

Notes:

1. Delay adder for CMOS Inputs option: for -3 speed grade, add 0.4 ns; for -4 speed grade, add 0.2 ns.
2. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
3. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Clocks							
T_{CH}	Clock High	All devices	3.0	-	4.0	-	ns
T_{CL}	Clock Low	All devices	3.0	-	4.0	-	ns
Propagation Delays - TTL Outputs(1,2)							
T_{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.3	-	4.5	ns
T_{OKPOS}	Clock (OK to Pad, slew-rate limited	All devices	-	6.9	-	7.0	ns
T_{OPF}	Output (O) to Pad, fast	All devices	-	3.6	-	4.8	ns
T_{OPS}	Output (O) to Pad, slew-rate limited	All devices	-	7.2	-	7.3	ns
T_{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	3.0	-	3.8	ns
T_{TSONF}	3-state to Pad active and valid, fast	All devices	-	6.0	-	7.3	ns
T_{TSONS}	3-state to Pad active and valid, slew-rate limited	All devices	-	9.6	-	9.8	ns
Setup and Hold Times							
T_{OOK}	Output (O) to clock (OK) setup time	All devices	2.5	-	3.8	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T_{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	2.0	-	2.7	-	ns
T_{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.0	-	0.5	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	11.5		13.5		ns
T_{RPO}	Delay from GSR input to any Pad	XCS05	-	12.0	-	15.0	ns
		XCS10	-	12.5	-	15.7	ns
		XCS20	-	13.0	-	16.2	ns
		XCS30	-	13.5	-	16.9	ns
		XCS40	-	14.0	-	17.5	ns

Notes:

1. Delay adder for CMOS Outputs option (with fast slew rate option): for -3 speed grade, add 1.0 ns; for -4 speed grade, add 0.8 ns.
2. Delay adder for CMOS Outputs option (with slow slew rate option): for -3 speed grade, add 2.0 ns; for -4 speed grade, add 1.5 ns.
3. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
4. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Setup Times							
T_{ECIK}	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T_{PICK}	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T_{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T_{PID}	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T_{Delay}	$T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T_{RRI}	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and Spartan-XL device. They follow the pad locations around the die, and include boundary scan register locations.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84(4)	VQ100	Bndry Scan
VCC	P2	P89	-
I/O	P3	P90	32
I/O	P4	P91	35
I/O	-	P92	38
I/O	-	P93	41
I/O	P5	P94	44
I/O	P6	P95	47
I/O	P7	P96	50
I/O	P8	P97	53
I/O	P9	P98	56
I/O, SGCK1(1), GCK8(2)	P10	P99	59
VCC	P11	P100	-
GND	P12	P1	-
I/O, PGCK1(1), GCK1(2)	P13	P2	62
I/O	P14	P3	65
I/O, TDI	P15	P4	68
I/O, TCK	P16	P5	71
I/O, TMS	P17	P6	74
I/O	P18	P7	77
I/O	-	P8	83
I/O	P19	P9	86
I/O	P20	P10	89
GND	P21	P11	-
VCC	P22	P12	-
I/O	P23	P13	92
I/O	P24	P14	95
I/O	-	P15	98
I/O	P25	P16	104
I/O	P26	P17	107
I/O	P27	P18	110
I/O	-	P19	113
I/O	P28	P20	116
I/O, SGCK2(1), GCK2(2)	P29	P21	119
Not Connected(1), M1(2)	P30	P22	122
GND	P31	P23	-
MODE(1), M0 (2)	P32	P24	125
VCC	P33	P25	-

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84(4)	VQ100	Bndry Scan
Not Connected(1), $\overline{\text{PWRDWN}}$(2)	P34	P26	126(1)
I/O, PGCK2(1), GCK3 (2)	P35	P27	127(3)
I/O (HDC)	P36	P28	130(3)
I/O	-	P29	133(3)
I/O ($\overline{\text{LDC}}$)	P37	P30	136(3)
I/O	P38	P31	139(3)
I/O	P39	P32	142(3)
I/O	-	P33	145(3)
I/O	-	P34	148(3)
I/O	P40	P35	151(3)
I/O ($\overline{\text{INIT}}$)	P41	P36	154(3)
VCC	P42	P37	-
GND	P43	P38	-
I/O	P44	P39	157(3)
I/O	P45	P40	160(3)
I/O	-	P41	163(3)
I/O	-	P42	166(3)
I/O	P46	P43	169(3)
I/O	P47	P44	172(3)
I/O	P48	P45	175(3)
I/O	P49	P46	178(3)
I/O	P50	P47	181(3)
I/O, SGCK3(1), GCK4(2)	P51	P48	184(3)
GND	P52	P49	-
DONE	P53	P50	-
VCC	P54	P51	-
$\overline{\text{PROGRAM}}$	P55	P52	-
I/O (D7(2))	P56	P53	187(3)
I/O, PGCK3(1), GCK5(2)	P57	P54	190(3)
I/O (D6(2))	P58	P55	193(3)
I/O	-	P56	196(3)
I/O (D5(2))	P59	P57	199(3)
I/O	P60	P58	202(3)
I/O	-	P59	205(3)
I/O	-	P60	208(3)
I/O (D4(2))	P61	P61	211(3)
I/O	P62	P62	214(3)
VCC	P63	P63	-
GND	P64	P64	-
I/O (D3(2))	P65	P65	217(3)
I/O	P66	P66	220(3)
I/O	-	P67	223(3)
I/O (D2(2))	P67	P68	229(3)
I/O	P68	P69	232(3)
I/O (D1(2))	P69	P70	235(3)

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84[4]	VQ100	Bndry Scan
I/O	P70	P71	238[3]
I/O (D0[2], DIN)	P71	P72	241[3]
I/O, SGCK4[1], GCK6[2] (DOUT)	P72	P73	244[3]
CCLK	P73	P74	-
VCC	P74	P75	-
O, TDO	P75	P76	0
GND	P76	P77	-
I/O	P77	P78	2
I/O, PGCK4[1], GCK7[2]	P78	P79	5
I/O (CS1[2])	P79	P80	8
I/O	P80	P81	11
I/O	P81	P82	14
I/O	P82	P83	17
I/O	-	P84	20
I/O	-	P85	23
I/O	P83	P86	26
I/O	P84	P87	29
GND	P1	P88	-

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS05XL is not part of the Boundary Scan chain. For the XCS05XL, subtract 1 from all Boundary Scan numbers from GCK3 on (127 and higher).
4. PC84 package discontinued by PDN2004-01

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
VCC	P2	P89	D7	P128	-
I/O	P3	P90	A6	P129	44
I/O	P4	P91	B6	P130	47
I/O	-	P92	C6	P131	50
I/O	-	P93	D6	P132	53
I/O	P5	P94	A5	P133	56
I/O	P6	P95	B5	P134	59
I/O	-	-	C5	P135	62
I/O	-	-	D5	P136	65
GND	-	-	A4	P137	-
I/O	P7	P96	B4	P138	68
I/O	P8	P97	C4	P139	71
I/O	-	-	A3	P140	74
I/O	-	-	B3	P141	77
I/O	P9	P98	C3	P142	80

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O, SGCK1[1] GCK8[2]	P10	P99	A2	P143	83
VCC	P11	P100	B2	P144	-
GND	P12	P1	A1	P1	-
I/O, PGCK1[1] GCK1[2]	P13	P2	B1	P2	86
I/O	P14	P3	C2	P3	89
I/O	-	-	C1	P4	92
I/O	-	-	D4	P5	95
I/O, TDI	P15	P4	D3	P6	98
I/O, TCK	P16	P5	D2	P7	101
GND	-	-	D1	P8	-
I/O	-	-	E4	P9	104
I/O	-	-	E3	P10	107
I/O, TMS	P17	P6	E2	P11	110
I/O	P18	P7	E1	P12	113
I/O	-	-	F4	P13	116
I/O	-	P8	F3	P14	119
I/O	P19	P9	F2	P15	122
I/O	P20	P10	F1	P16	125
GND	P21	P11	G2	P17	-
VCC	P22	P12	G1	P18	-
I/O	P23	P13	G3	P19	128
I/O	P24	P14	G4	P20	131
I/O	-	P15	H1	P21	134
I/O	-	-	H2	P22	137
I/O	P25	P16	H3	P23	140
I/O	P26	P17	H4	P24	143
I/O	-	-	J1	P25	146
I/O	-	-	J2	P26	149
GND	-	-	J3	P27	-
I/O	P27	P18	J4	P28	152
I/O	-	P19	K1	P29	155
I/O	-	-	K2	P30	158
I/O	-	-	K3	P31	161
I/O	P28	P20	L1	P32	164
I/O, SGCK2[1] GCK2[2]	P29	P21	L2	P33	167
Not Connect-ed[1] M1[2]	P30	P22	L3	P34	170
GND	P31	P23	M1	P35	-
MODE[1], M0[2]	P32	P24	M2	P36	173

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O	P80	P81	A10	P116	17
GND	-	-	C9	P118	-
I/O	-	-	B9	P119	20
I/O	-	-	A9	P120	23
I/O	P81	P82	D8	P121	26
I/O	P82	P83	C8	P122	29
I/O	-	P84	B8	P123	32
I/O	-	P85	A8	P124	35
I/O	P83	P86	B7	P125	38
I/O	P84	P87	A7	P126	41
GND	P1	P88	C7	P127	-

Notes:

1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS10XL is not part of the Boundary Scan chain. For the XCS10XL, subtract 1 from all Boundary Scan numbers from GCK3 on (175 and higher).
4. PC84 and CS144 packages discontinued by PDN2004-01

Additional XCS10/XL Package Pins

TQ144					
Not Connected Pins					
P117	-	-	-	-	-
5/5/97					

CS144					
Not Connected Pins					
D9	-	-	-	-	-
4/28/99					

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
VCC	P89	D7	P128	P183	-
I/O	P90	A6	P129	P184	62
I/O	P91	B6	P130	P185	65
I/O	P92	C6	P131	P186	68
I/O	P93	D6	P132	P187	71
I/O	-	-	-	P188	74
I/O	-	-	-	P189	77
I/O	P94	A5	P133	P190	80
I/O	P95	B5	P134	P191	83
VCC[2]	-	-	-	P192	-
I/O	-	C5	P135	P193	86
I/O	-	D5	P136	P194	89
GND	-	A4	P137	P195	-
I/O	-	-	-	P196	92
I/O	-	-	-	P197	95
I/O	-	-	-	P198	98
I/O	-	-	-	P199	101
I/O	P96	B4	P138	P200	104
I/O	P97	C4	P139	P201	107
I/O	-	A3	P140	P204	110
I/O	-	B3	P141	P205	113
I/O	P98	C3	P142	P206	116

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O, SGCK1[1], GCK8[2]	P99	A2	P143	P207	119
VCC	P100	B2	P144	P208	-
GND	P1	A1	P1	P1	-
I/O, PGCK1[1], GCK1[2]	P2	B1	P2	P2	122
I/O	P3	C2	P3	P3	125
I/O	-	C1	P4	P4	128
I/O	-	D4	P5	P5	131
I/O, TDI	P4	D3	P6	P6	134
I/O, TCK	P5	D2	P7	P7	137
I/O	-	-	-	P8	140
I/O	-	-	-	P9	143
I/O	-	-	-	P10	146
I/O	-	-	-	P11	149
GND	-	D1	P8	P13	-
I/O	-	E4	P9	P14	152
I/O	-	E3	P10	P15	155
I/O, TMS	P6	E2	P11	P16	158
I/O	P7	E1	P12	P17	161
VCC[2]	-	-	-	P18	-
I/O	-	-	-	P19	164
I/O	-	-	-	P20	167

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7[2])	P53	L12	P75	P107	367 [3]
I/O, PGCK3[1], GCK5[2]	P54	L13	P76	P108	370 [3]
I/O	-	K10	P77	P109	373 [3]
I/O	-	K11	P78	P110	376 [3]
I/O (D6[2])	P55	K12	P79	P112	379 [3]
I/O	P56	K13	P80	P113	382 [3]
I/O	-	-	-	P114	385 [3]
I/O	-	-	-	P115	388 [3]
I/O	-	-	-	P116	391 [3]
I/O	-	-	-	P117	394 [3]
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 [3]
I/O	-	J12	P83	P120	400 [3]
VCC[2]	-	-	-	P121	-
I/O (D5[2])	P57	J13	P84	P122	403 [3]
I/O	P58	H10	P85	P123	406 [3]
I/O	-	-	-	P124	409 [3]
I/O	-	-	-	P125	412 [3]
I/O	P59	H11	P86	P126	415 [3]
I/O	P60	H12	P87	P127	418 [3]
I/O (D4[2])	P61	H13	P88	P128	421 [3]
I/O	P62	G12	P89	P129	424 [3]
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3[2])	P65	G10	P92	P132	427 [3]
I/O	P66	F13	P93	P133	430 [3]
I/O	P67	F12	P94	P134	433 [3]
I/O	-	F11	P95	P135	436 [3]
I/O	-	-	-	P136	439 [3]
I/O	-	-	-	P137	442 [3]
I/O (D2[2])	P68	F10	P96	P138	445 [3]
I/O	P69	E13	P97	P139	448 [3]
VCC[2]	-	-	-	P140	-
I/O	-	E12	P98	P141	451 [3]
I/O	-	E11	P99	P142	454 [3]
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 [3]
I/O	-	-	-	P146	460 [3]
I/O	-	-	-	P147	463 [3]
I/O	-	-	-	P148	466 [3]
I/O (D1[2])	P70	D13	P101	P149	469 [3]
I/O	P71	D12	P102	P150	472 [3]
I/O	-	D11	P103	P151	475 [3]

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144[2,4]	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 [3]
I/O (D0[2], DIN)	P72	C12	P105	P153	481 [3]
I/O, SGCK4[1], GCK6[2] (DOUT)	P73	C11	P106	P154	484 [3]
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4[1], GCK7[2]	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1[2])	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC[2]	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

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XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	P5	P5	P5	D3	C1	155
I/O, TDI	P4	P6	P6	P6	E4	D4	158
I/O, TCK	P5	P7	P7	P7	C1	D3	161
I/O	-	-	P8	P8	D1	E2	164
I/O	-	-	P9	P9	E3	E4	167
I/O	-	-	P10	P10	E2	E1	170
I/O	-	-	P11	P11	E1	F5	173
I/O	-	-	P12	P12	F3	F3	176
I/O	-	-	-	P13	F2	F2	179
GND	-	P8	P13	P14	GND[4]	GND[4]	-
I/O	-	P9	P14	P15	G3	F4	182
I/O	-	P10	P15	P16	G2	F1	185
I/O, TMS	P6	P11	P16	P17	G1	G3	188
I/O	P7	P12	P17	P18	H3	G2	191
VCC	-	-	P18	P19	VCC[4]	G1	-
I/O	-	-	-	P20	H2	G4	194
I/O	-	-	-	P21	H1	H1	197
I/O	-	-	P19	P23	J2	H4	200
I/O	-	-	P20	P24	J1	J1	203
I/O	-	P13	P21	P25	K2	J2	206
I/O	P8	P14	P22	P26	K3	J3	209
I/O	P9	P15	P23	P27	K1	J4	212
I/O	P10	P16	P24	P28	L1	K1	215
GND	P11	P17	P25	P29	GND[4]	GND[4]	-
VCC	P12	P18	P26	P30	VCC[4]	K2	-
I/O	P13	P19	P27	P31	L2	K3	218
I/O	P14	P20	P28	P32	L3	K4	221
I/O	P15	P21	P29	P33	L4	K5	224
I/O	-	P22	P30	P34	M1	L1	227
I/O	-	-	P31	P35	M2	L2	230
I/O	-	-	P32	P36	M3	L3	233
I/O	-	-	-	P38	N1	M2	236
I/O	-	-	-	P39	N2	M3	239
VCC	-	-	P33	P40	VCC[4]	M4	-
I/O	P16	P23	P34	P41	P1	N1	242
I/O	P17	P24	P35	P42	P2	N2	245
I/O	-	P25	P36	P43	R1	N3	248
I/O	-	P26	P37	P44	P3	N4	251
GND	-	P27	P38	P45	GND[4]	GND[4]	-
I/O	-	-	-	P46	T1	P1	254
I/O	-	-	P39	P47	R3	P2	257
I/O	-	-	P40	P48	T2	P3	260
I/O	-	-	P41	P49	U1	P4	263
I/O	-	-	P42	P50	T3	P5	266
I/O	-	-	P43	P51	U2	R1	269