AMD Xilinx - XCS40XL-4PQ208I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	169
Number of Gates	40000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40xl-4pq208i

Table 2: **CLB Storage Element Functionality**

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
	⌐	1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (Spartan-XL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X	Don't care
⌐	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

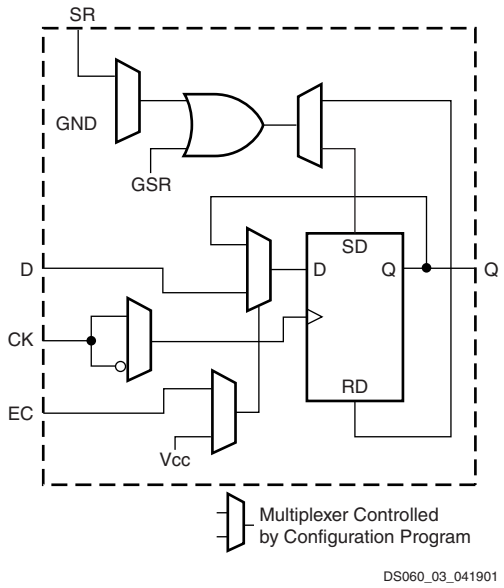


Figure 3: **CLB Flip-Flop Functional Block Diagram**

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

CLB Signal Flow Control

In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2, page 4) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinatorial CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinatorial output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1-C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

This high value makes them unsuitable as wired-AND pull-up resistors.

Table 7: **Supported Destinations for Spartan/XL Outputs**

Destination	Spartan-XL Outputs	Spartan Outputs	
	3.3V, CMOS	5V, TTL	5V, CMOS
Any device, V_{CC} = 3.3V, CMOS-threshold inputs	√	√	Some(1)
Any device, V_{CC} = 5V, TTL-threshold inputs	√	√	√
Any device, V_{CC} = 5V, CMOS-threshold inputs	Unreliable Data		√

Notes:
1. Only if destination device has 5V tolerant inputs.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops (Figure 5). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (see EC signal in Figure 5), which through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan/XL FPGA CLB. It cannot be inverted within the IOB.

Routing Channel Description

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

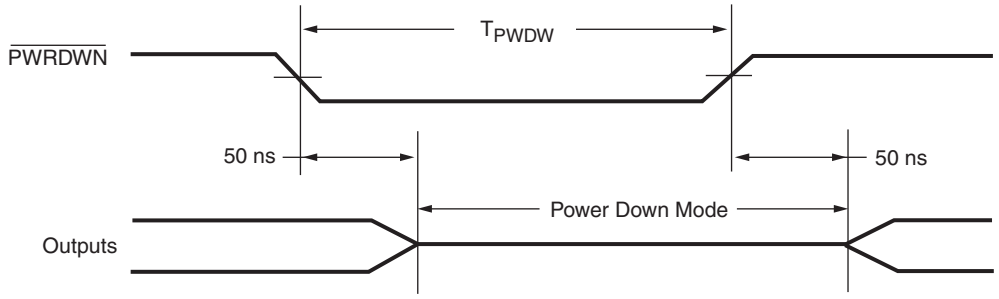
This section describes the routing channels available in Spartan/XL devices. Figure 8 shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the designer should open a design in the FPGA Editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

CLB Routing Channels

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). Figure 8 shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.



Description	Symbol	Min
Power Down Time	T_{PWD}	50 ns
Power Down Pulse Width	T_{PWDW}	50 ns

DS060_23_041901

Figure 23: **$\overline{\text{PWRDWN}}$ Pulse Timing**

Power-down retains the configuration, but loses all data stored in the device flip-flops. All inputs are interpreted as Low, but the internal combinatorial logic is fully functional. Make sure that the combination of all inputs Low and all flip-flops set or reset in your design will not generate internal oscillations, or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line.

During configuration, the $\overline{\text{PWRDWN}}$ pin must be High. If the Power Down state is entered before or during configuration, the device will restart configuration once the $\overline{\text{PWRDWN}}$ signal is removed. Note that the configuration pins are affected by Power Down and may not reflect their normal function. If there is an external pull-up resistor on the DONE pin, it will be High during Power Down even if the device is not yet configured. Similarly, if $\overline{\text{PWRDWN}}$ is asserted before configuration is completed, the $\overline{\text{INIT}}$ pin will not indicate status information.

Note that the $\overline{\text{PWRDWN}}$ pin is not part of the Boundary Scan chain. Therefore, the Spartan-XL family has a separate set of BSDL files than the 5V Spartan family. Boundary scan logic is not usable during Power Down.

Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan/XL devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Configuration Mode Control

5V Spartan devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

3V Spartan-XL devices have three configuration modes.

- M1/M0 = 11 sets Slave Serial mode
- M1/M0 = 10 sets Master Serial mode
- M1/M0 = 0X sets Express mode

In addition to these modes, the device can be configured through the Boundary Scan logic (See "Configuration Through the Boundary Scan Pins" on page 37.).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pin are unused. The Mode pins have a weak pull-up resistor turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the MODE/M0 pin should be connected directly to GND, or through a pull-down resistor of 1 KΩ or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during con-

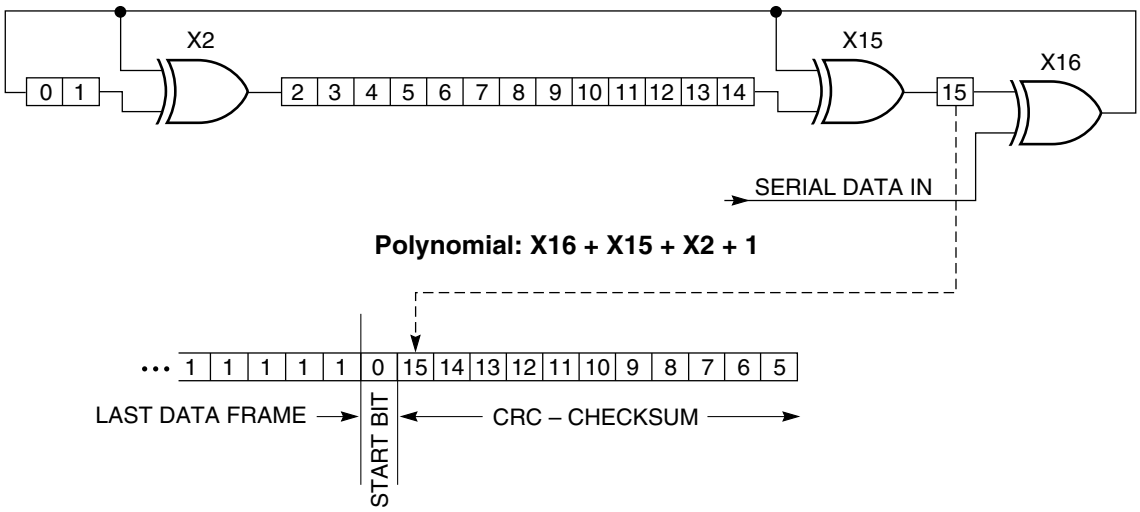


Figure 29: **Circuit for Generating CRC-16**

Configuration Sequence

There are four major steps in the Spartan/XL FPGA power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC}. When all $\overline{INIT}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{INIT}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{LDC}$, $\overline{INIT}$ and DONE provide status outputs for the system interface. The outputs $\overline{LDC}$, $\overline{INIT}$ and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain $\overline{INIT}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive $\overline{INIT}$. Two internal clocks after the $\overline{INIT}$ pin is recognized as High, the device samples the MODE pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

to wait after completing the configuration memory clear operation. When $\overline{INIT}$ is no longer held Low externally, the device determines its configuration mode by capturing the state of the Mode pins, and is ready to start the configuration process. A master device waits up to an additional 300 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{INIT}$ is High.

For more details on Configuration, refer to the Xilinx Application Note "FPGA Configuration Guidelines" (XAPP090).

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user system. Start-up must make sure that the user logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the Global Set/Reset (GSR) at the right time.

Start-Up Initiation

Two conditions have to be met in order for the start-up sequence to begin:

- The chip's internal memory must be full, and
- The configuration length count must be met, exactly.

In all configuration modes except Express mode, Spartan/XL devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

In Express mode, there is no length count. The start-up sequence for each device begins when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

Start-Up Events

The device can be programmed to control three start-up events.

- The release of the open-drain DONE output
- The termination of the Global Three-State and the change of configuration-related pins to the user function, activating all IOBs.
- The termination of the Global Set/Reset initialization of all CLB and IOB storage elements.

Figure 31 describes start-up timing in detail. The three events — DONE going High, the internal GSR being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. This relative timing is selected by options in the bitstream generation software. Heavy lines in Figure 31 show the default timing. The thin lines indicate all other possible timing options. The start-up logic must be clocked until the "F" (Finished) state is reached.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. GSR is then released another clock period later to make sure that user operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 31, but the designer can modify it to meet particular requirements.

Start-Up Clock

Normally, the start-up sequence is controlled by the internal device oscillator (CCLK), which is asynchronous to the system clock. As a configuration option, they can be triggered by an on-chip user net called UCLK. This user net can be accessed by placing the STARTUP library symbol, and the start-up modes are known as UCLK_NOSYNC or UCLK_SYNC. This allows the device to wake up in synchronism with the user system.

DONE Pin

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to the start-up control logic. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK_SYNC or UCLK_SYNC. When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK_NOSYNC or UCLK_NOSYNC. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, while the other configuration modes can use any of the four timing sequences.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

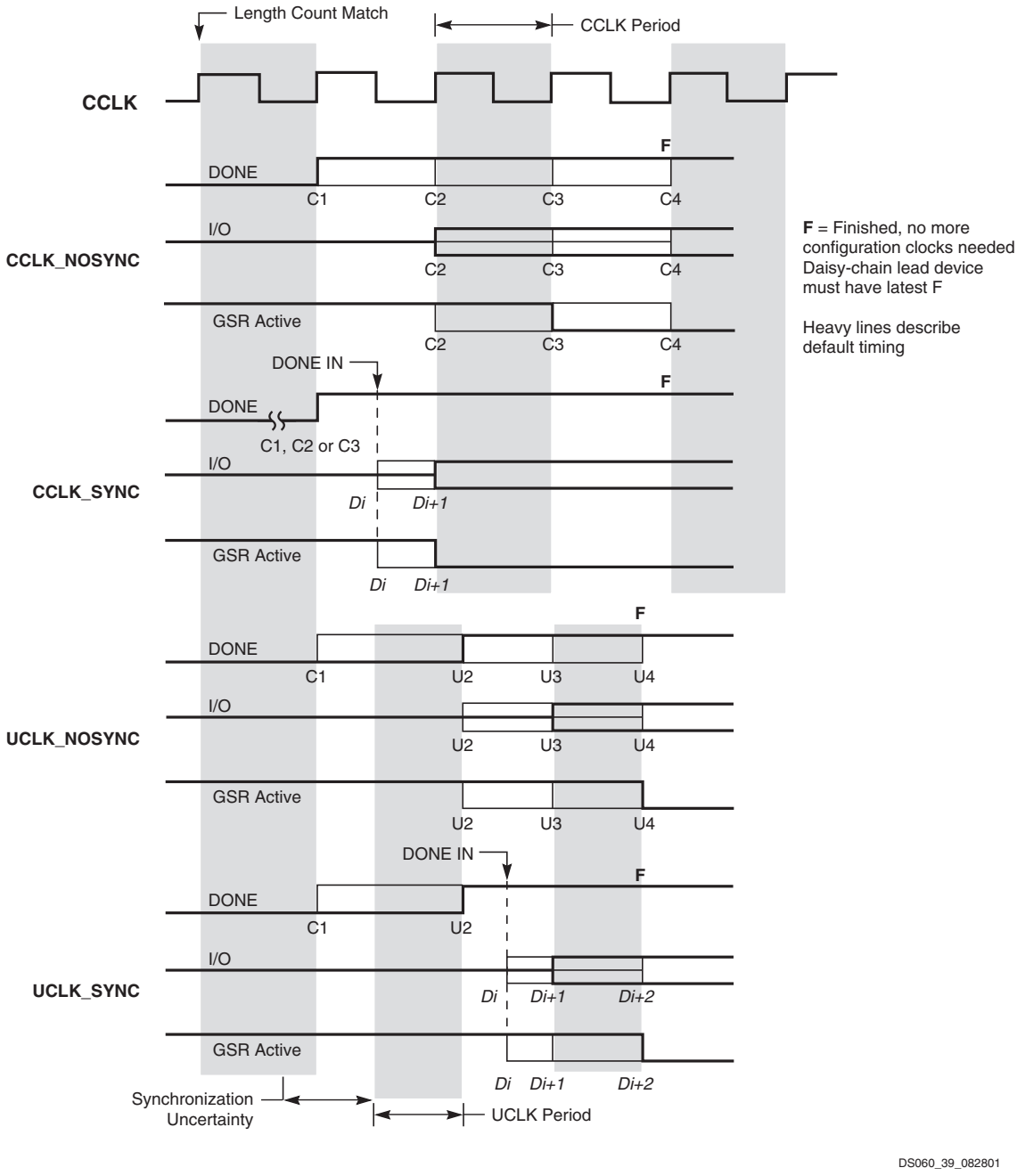


Figure 31: **Start-up Timing**

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input.
- Wait for $\overline{\text{INIT}}$ to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after $\overline{\text{INIT}}$ goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and Spartan-XL devices.

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.

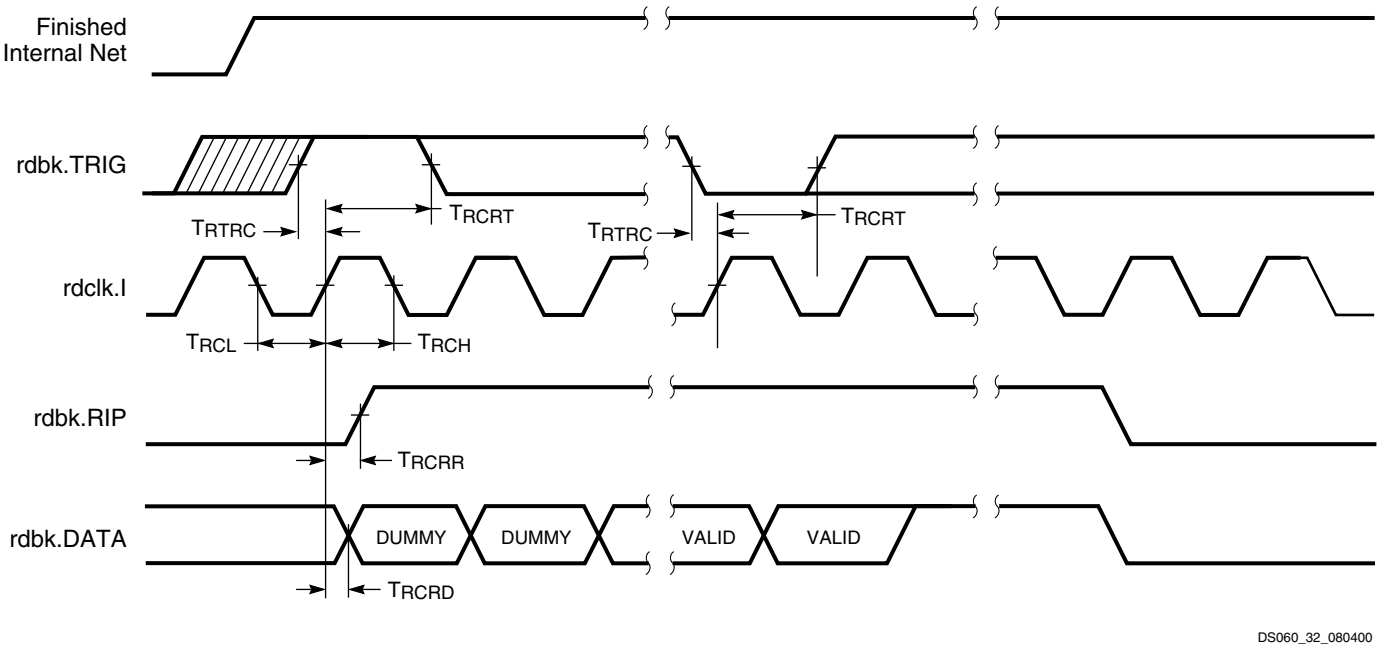


Figure 33: **Spartan and Spartan-XL Readback Timing Diagram**

Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:
1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Spartan Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan Family Absolute Maximum Ratings(1)

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND(2,3)		–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output(2,3)		–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot (above V_{CC}) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3. Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = –40°C to +100°C(1)	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage(2)	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage(2)	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Spartan Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage @ I_{OH} = –1.0 mA, V_{CC} min	CMOS outputs	V_{CC} – 0.5	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min(1)	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		3.0	-	V
I_{CCO}	Quiescent FPGA supply current(2)	Commercial	-	3.0	mA
		Industrial	-	6.0	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)		-	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 5V (sample tested)		0.02	-	mA

Notes:
1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a Tie option.

Spartan Family Global Buffer Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
T_{PG}	From pad through Primary buffer, to any clock K	XCS05	2.0	4.0	ns
		XCS10	2.4	4.3	ns
		XCS20	2.8	5.4	ns
		XCS30	3.2	5.8	ns
		XCS40	3.5	6.4	ns
T_{SG}	From pad through Secondary buffer, to any clock K	XCS05	2.5	4.4	ns
		XCS10	2.9	4.7	ns
		XCS20	3.3	5.8	ns
		XCS30	3.6	6.2	ns
		XCS40	3.9	6.7	ns

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Single Port RAM	Size[1]	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T_{WCTS}		32x1	8.0	-	11.6	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T_{WPTS}		32x1	4.0	-	5.8	-	ns
T_{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T_{ASTS}		32x1	1.5	-	2.0	-	ns
T_{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{AHTS}		32x1	0.0	-	0.0	-	ns
T_{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T_{DSTS}		32x1	1.5	-	1.7	-	ns
T_{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{DHTS}		32x1	0.0	-	0.0	-	ns
T_{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T_{WSTS}		32x1	1.5	-	1.6	-	ns
T_{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T_{WHTS}		32x1	0.0	-	0.0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T_{WOTS}		32x1	-	7.0	-	9.3	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T_{RCT}		32x1	3.8	-	3.8	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.2	-	1.6	ns
T_{IHO}		32x1	-	2.0	-	2.7	ns
T_{ICK}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T_{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:
1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Min	Min	
Input Setup/Hold Times Using Primary Clock and IFF					
T_{PSUF}/T_{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T_{PSU}/T_{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T_{SSUF}/T_{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T_{SSU}/T_{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:

1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-4		-3		
			Min	Max	Min	Max	
Clocks							
T_{CH}	Clock High	All devices	3.0	-	4.0	-	ns
T_{CL}	Clock Low	All devices	3.0	-	4.0	-	ns
Propagation Delays - TTL Outputs(1,2)							
T_{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.3	-	4.5	ns
T_{OKPOS}	Clock (OK to Pad, slew-rate limited	All devices	-	6.9	-	7.0	ns
T_{OPF}	Output (O) to Pad, fast	All devices	-	3.6	-	4.8	ns
T_{OPS}	Output (O) to Pad, slew-rate limited	All devices	-	7.2	-	7.3	ns
T_{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	3.0	-	3.8	ns
T_{TSONF}	3-state to Pad active and valid, fast	All devices	-	6.0	-	7.3	ns
T_{TSONS}	3-state to Pad active and valid, slew-rate limited	All devices	-	9.6	-	9.8	ns
Setup and Hold Times							
T_{OOK}	Output (O) to clock (OK) setup time	All devices	2.5	-	3.8	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T_{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	2.0	-	2.7	-	ns
T_{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.0	-	0.5	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	11.5		13.5		ns
T_{RPO}	Delay from GSR input to any Pad	XCS05	-	12.0	-	15.0	ns
		XCS10	-	12.5	-	15.7	ns
		XCS20	-	13.0	-	16.2	ns
		XCS30	-	13.5	-	16.9	ns
		XCS40	-	14.0	-	17.5	ns

Notes:

1. Delay adder for CMOS Outputs option (with fast slew rate option): for -3 speed grade, add 1.0 ns; for -4 speed grade, add 0.8 ns.
2. Delay adder for CMOS Outputs option (with slow slew rate option): for -3 speed grade, add 2.0 ns; for -4 speed grade, add 1.5 ns.
3. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
4. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

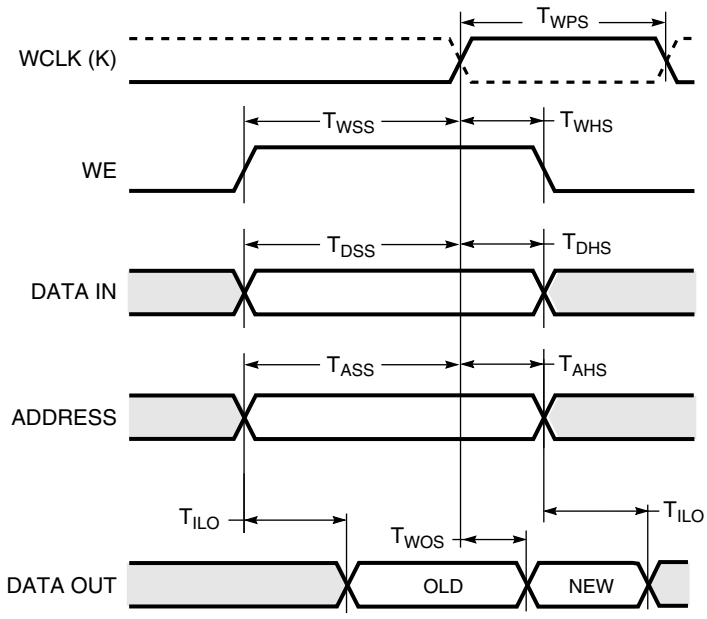
All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation(1)							
T_{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T_{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

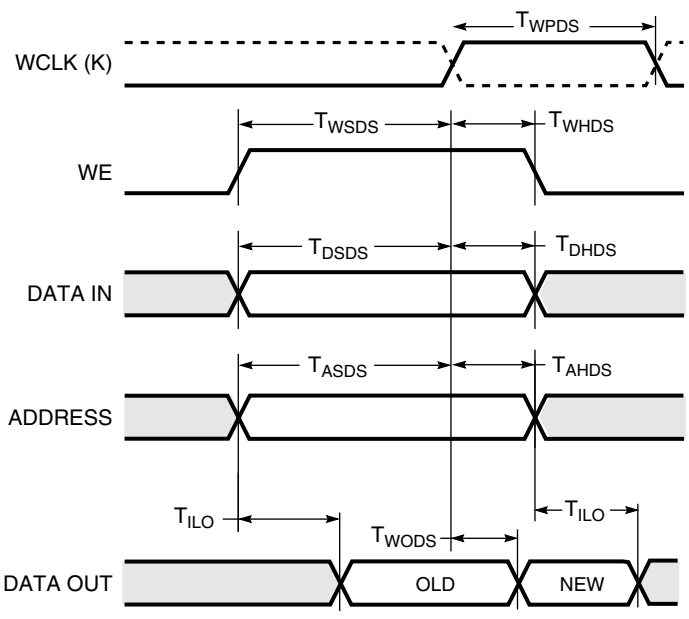
Notes:
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



DS060_34_011300

Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See **Global Signals: GSR and GTS**, page 20 for more information.

Device pins for Spartan/XL devices are described in Table 18.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pinouts as the standard package options.

Table 18: **Pin Descriptions**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
V_{CC}	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 –0.1 µF capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See **Violating the Maximum High and Low Time Specification for the Readback Clock**, page 39 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an open-drain output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.

Table 18: **Pin Descriptions *(Continued)***

Pin Name	I/O During Config.	I/O After Config.	Pin Description
$\overline{\text{PWRDWN}}$	I	I	$\overline{\text{PWRDWN}}$ is an active Low input that forces the FPGA into the Power Down state and reduces power consumption. When $\overline{\text{PWRDWN}}$ is Low, the FPGA disables all I/O and initializes all flip-flops. All inputs are interpreted as Low independent of their actual level. VCC must be maintained, and the configuration data is maintained. $\overline{\text{PWRDWN}}$ halts configuration if asserted before or during configuration, and re-starts configuration when removed. When $\overline{\text{PWRDWN}}$ returns High, the FPGA becomes operational by first enabling the inputs and flip-flops and then enabling the outputs. $\overline{\text{PWRDWN}}$ has a default internal pull-up resistor.
User I/O Pins That Can Have Special Functions			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ to 10 kΩ external pull-up resistor is recommended. As an active Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.

XCS05 and XCS05XL Device Pinouts

XCS05/XL Pad Name	PC84[4]	VQ100	Bndry Scan
I/O	P70	P71	238[3]
I/O (D0[2], DIN)	P71	P72	241[3]
I/O, SGCK4[1], GCK6[2] (DOUT)	P72	P73	244[3]
CCLK	P73	P74	-
VCC	P74	P75	-
O, TDO	P75	P76	0
GND	P76	P77	-
I/O	P77	P78	2
I/O, PGCK4[1], GCK7[2]	P78	P79	5
I/O (CS1[2])	P79	P80	8
I/O	P80	P81	11
I/O	P81	P82	14
I/O	P82	P83	17
I/O	-	P84	20
I/O	-	P85	23
I/O	P83	P86	26
I/O	P84	P87	29
GND	P1	P88	-

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The "PWRDWN" on the XCS05XL is not part of the Boundary Scan chain. For the XCS05XL, subtract 1 from all Boundary Scan numbers from GCK3 on (127 and higher).
4. PC84 package discontinued by PDN2004-01

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
VCC	P2	P89	D7	P128	-
I/O	P3	P90	A6	P129	44
I/O	P4	P91	B6	P130	47
I/O	-	P92	C6	P131	50
I/O	-	P93	D6	P132	53
I/O	P5	P94	A5	P133	56
I/O	P6	P95	B5	P134	59
I/O	-	-	C5	P135	62
I/O	-	-	D5	P136	65
GND	-	-	A4	P137	-
I/O	P7	P96	B4	P138	68
I/O	P8	P97	C4	P139	71
I/O	-	-	A3	P140	74
I/O	-	-	B3	P141	77
I/O	P9	P98	C3	P142	80

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O, SGCK1[1] GCK8[2]	P10	P99	A2	P143	83
VCC	P11	P100	B2	P144	-
GND	P12	P1	A1	P1	-
I/O, PGCK1[1] GCK1[2]	P13	P2	B1	P2	86
I/O	P14	P3	C2	P3	89
I/O	-	-	C1	P4	92
I/O	-	-	D4	P5	95
I/O, TDI	P15	P4	D3	P6	98
I/O, TCK	P16	P5	D2	P7	101
GND	-	-	D1	P8	-
I/O	-	-	E4	P9	104
I/O	-	-	E3	P10	107
I/O, TMS	P17	P6	E2	P11	110
I/O	P18	P7	E1	P12	113
I/O	-	-	F4	P13	116
I/O	-	P8	F3	P14	119
I/O	P19	P9	F2	P15	122
I/O	P20	P10	F1	P16	125
GND	P21	P11	G2	P17	-
VCC	P22	P12	G1	P18	-
I/O	P23	P13	G3	P19	128
I/O	P24	P14	G4	P20	131
I/O	-	P15	H1	P21	134
I/O	-	-	H2	P22	137
I/O	P25	P16	H3	P23	140
I/O	P26	P17	H4	P24	143
I/O	-	-	J1	P25	146
I/O	-	-	J2	P26	149
GND	-	-	J3	P27	-
I/O	P27	P18	J4	P28	152
I/O	-	P19	K1	P29	155
I/O	-	-	K2	P30	158
I/O	-	-	K3	P31	161
I/O	P28	P20	L1	P32	164
I/O, SGCK2[1] GCK2[2]	P29	P21	L2	P33	167
Not Connect-ed[1] M1[2]	P30	P22	L3	P34	170
GND	P31	P23	M1	P35	-
MODE[1], M0[2]	P32	P24	M2	P36	173

Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 (1)	P33 (1)	P39	P65	P71 (1)
P86 (1)	P92	P111	P121(1)	P140(1)	P144
P165	P173(1)	P192(1)	P202	P203	-
9/16/98					

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by PDN2004-01

XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100(5)	TQ144	PQ208	PQ240	BG256(5)	CS280(2,5)	Bndry Scan
VCC	P89	P128	P183	P212	VCC(4)	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC(4)	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND(4)	GND(4)	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1(1), GCK8(2)	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC(4)	A1	-
GND	P1	P1	P1	P1	GND(4)	GND(4)	-
I/O, PGCK1(1), GCK1(2)	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

CS280

VCC Pins					
E5	E7	E8	E9	E11	E12
E13	G5	G15	H5	H15	J5
J15	L5	L15	M5	M15	N5
N15	R7	R8	R9	R11	R12
R13	-	-	-	-	-
Not Connected Pins					
A4	A12	C8	C12	C15	D1
D2	D5	D8	D17	D18	E15
H2	H3	H18	H19	L4	M1
M16	M18	R2	R4	R5	R15
R17	T8	T15	U5	V8	V12
W12	W16	-	-	-	-
Not Connected Pins (VCC in XCS40XL)					
B5	B15	E3	E18	R3	R18
V5	V15	-	-	-	-

5/21/02

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
VCC	P183	P212	VCC(4)	VCC(4)	-
I/O	P184	P213	C10	D10	86
I/O	P185	P214	D10	E10	89
I/O	P186	P215	A9	A9	92
I/O	P187	P216	B9	B9	95
I/O	P188	P217	C9	C9	98
I/O	P189	P218	D9	D9	101
I/O	P190	P220	A8	A8	104
I/O	P191	P221	B8	B8	107
I/O	-	-	C8	C8	110
I/O	-	-	A7	D8	113
VCC	P192	P222	VCC(4)	VCC(4)	-
I/O	-	P223	A6	B7	116
I/O	-	P224	C7	C7	119
I/O	P193	P225	B6	D7	122
I/O	P194	P226	A5	A6	125
GND	P195	P227	GND(4)	GND(4)	-
I/O	P196	P228	C6	B6	128
I/O	P197	P229	B5	C6	131
I/O	P198	P230	A4	D6	134
I/O	P199	P231	C5	E6	137

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O	P200	P232	B4	A5	140
I/O	P201	P233	A3	C5	143
I/O	-	-	-	D5	146
I/O	-	-	-	A4	149
I/O	P202	P234	D5	B4	152
I/O	P203	P235	C4	C4	155
I/O	P204	P236	B3	A3	158
I/O	P205	P237	B2	A2	161
I/O	P206	P238	A2	B3	164
I/O, SGCK1(1), GCK8(2)	P207	P239	C3	B2	167
VCC	P208	P240	VCC(4)	VCC(4)	-
GND	P1	P1	GND(4)	GND(4)	-
I/O, PGCK1(1), GCK1(2)	P2	P2	B1	C3	170
I/O	P3	P3	C2	C2	173
I/O	P4	P4	D2	B1	176
I/O	P5	P5	D3	C1	179
I/O, TDI	P6	P6	E4	D4	182
I/O, TCK	P7	P7	C1	D3	185
I/O	-	-	-	D2	188
I/O	-	-	-	D1	191
I/O	P8	P8	D1	E2	194
I/O	P9	P9	E3	E4	197
I/O	P10	P10	E2	E1	200
I/O	P11	P11	E1	F5	203
I/O	P12	P12	F3	F3	206
I/O	-	P13	F2	F2	209
GND	P13	P14	GND(4)	GND(4)	-
I/O	P14	P15	G3	F4	212
I/O	P15	P16	G2	F1	215
I/O, TMS	P16	P17	G1	G3	218
I/O	P17	P18	H3	G2	221
VCC	P18	P19	VCC(4)	VCC(4)	-
I/O	-	P20	H2	G4	224
I/O	-	P21	H1	H1	227
I/O	-	-	J4	H3	230
I/O	-	-	J3	H2	233
I/O	P19	P23	J2	H4	236
I/O	P20	P24	J1	J1	239
I/O	P21	P25	K2	J2	242
I/O	P22	P26	K3	J3	245
I/O	P23	P27	K1	J4	248
I/O	P24	P28	L1	K1	251

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
GND	P25	P29	GND(4)	GND(4)	-
VCC	P26	P30	VCC(4)	VCC(4)	-
I/O	P27	P31	L2	K3	254
I/O	P28	P32	L3	K4	257
I/O	P29	P33	L4	K5	260
I/O	P30	P34	M1	L1	263
I/O	P31	P35	M2	L2	266
I/O	P32	P36	M3	L3	269
I/O	-	-	M4	L4	272
I/O	-	-	-	M1	275
I/O	-	P38	N1	M2	278
I/O	-	P39	N2	M3	281
VCC	P33	P40	VCC(4)	VCC(4)	-
I/O	P34	P41	P1	N1	284
I/O	P35	P42	P2	N2	287
I/O	P36	P43	R1	N3	290
I/O	P37	P44	P3	N4	293
GND	P38	P45	GND(4)	GND(4)	-
I/O	-	P46	T1	P1	296
I/O	P39	P47	R3	P2	299
I/O	P40	P48	T2	P3	302
I/O	P41	P49	U1	P4	305
I/O	P42	P50	T3	P5	308
I/O	P43	P51	U2	R1	311
I/O	-	-	-	R2	314
I/O	-	-	-	R4	317
I/O	P44	P52	V1	T1	320
I/O	P45	P53	T4	T2	323
I/O	P46	P54	U3	T3	326
I/O	P47	P55	V2	U1	329
I/O	P48	P56	W1	V1	332
I/O, SGCK2(1), GCK2 (2)	P49	P57	V3	U2	335
Not Connected(1) M1(2)	P50	P58	W2	V2	338
GND	P51	P59	GND(4)	GND(4)	-
MODE(1), M0(2)	P52	P60	Y1	W1	341
VCC	P53	P61	VCC(4)	VCC(4)	-
Not Connected(1) $\overline{\text{PWRDWN}}$(2)	P54	P62	W3	V3	342(1)
I/O, PGCK2(1), GCK3(2)	P55	P63	Y2	W2	343 (3)

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280(2,5)	Bndry Scan
I/O (HDC)	P56	P64	W4	W3	346 (3)
I/O	P57	P65	V4	T4	349 (3)
I/O	P58	P66	U5	U4	352 (3)
I/O	P59	P67	Y3	V4	355 (3)
I/O ($\overline{\text{LDC}}$)	P60	P68	Y4	W4	358 (3)
I/O	-	-	-	R5	361 (3)
I/O	-	-	-	U5	364 (3)
I/O	P61	P69	V5	T5	367 (3)
I/O	P62	P70	W5	W5	370 (3)
I/O	P63	P71	Y5	R6	373 (3)
I/O	P64	P72	V6	U6	376 (3)
I/O	P65	P73	W6	V6	379 (3)
I/O	-	P74	Y6	T6	382 (3)
GND	P66	P75	GND(4)	GND(4)	-
I/O	P67	P76	W7	W6	385 (3)
I/O	P68	P77	Y7	U7	388 (3)
I/O	P69	P78	V8	V7	391 (3)
I/O	P70	P79	W8	W7	394 (3)
VCC	P71	P80	VCC(4)	VCC(4)	-
I/O	P72	P81	Y8	W8	397 (3)
I/O	P73	P82	U9	U8	400 (3)
I/O	-	-	V9	V8	403 (3)
I/O	-	-	W9	T8	406 (3)
I/O	-	P84	Y9	W9	409 (3)
I/O	-	P85	W10	V9	412 (3)
I/O	P74	P86	V10	U9	415 (3)
I/O	P75	P87	Y10	T9	418 (3)
I/O	P76	P88	Y11	W10	421 (3)
I/O ($\overline{\text{INIT}}$)	P77	P89	W11	V10	424 (3)
VCC	P78	P90	VCC(4)	VCC(4)	VCC(4)
GND	P79	P91	GND(4)	GND(4)	-
I/O	P80	P92	V11	T10	427 (3)
I/O	P81	P93	U11	R10	430 (3)
I/O	P82	P94	Y12	W11	433 (3)
I/O	P83	P95	W12	V11	436 (3)
I/O	P84	P96	V12	U11	439 (3)
I/O	P85	P97	U12	T11	442 (3)
I/O	-	-	Y13	W12	445 (3)
I/O	-	-	W13	V12	448 (3)
I/O	-	P99	V13	U12	451 (3)
I/O	-	P100	Y14	T12	454 (3)
VCC	P86	P101	VCC(4)	VCC(4)	-
I/O	P87	P102	Y15	V13	457 (3)
I/O	P88	P103	V14	U13	460 (3)
I/O	P89	P104	W15	T13	463 (3)

Product Availability

Table 19 shows the packages and speed grades for Spartan/XL devices. Table 20 shows the number of user I/Os available for each device/package combination.

Table 19: **Component Availability Chart for Spartan/XL FPGAs**

Device	Pins	84	100	144	144	208	240	256	280
	Type	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	Code	PC84(3)	VQ100(3)	CS144(3)	TQ144	PQ208	PQ240	BG256(3)	CS280(3)
XCS05	-3	C(3)	C, I	-	-	-	-	-	-
	-4	C(3)	C	-	-	-	-	-	-
XCS10	-3	C(3)	C, I	-	C	-	-	-	-
	-4	C(3)	C	-	C	-	-	-	-
XCS20	-3	-	C	-	C, I	C, I	-	-	-
	-4	-	C	-	C	C	-	-	-
XCS30	-3	-	C(3)	-	C, I	C, I	C	C(3)	-
	-4	-	C(3)	-	C	C	C	C(3)	-
XCS40	-3	-	-	-	-	C, I	C	C	-
	-4	-	-	-	-	C	C	C	-
XCS05XL	-4	C(3)	C, I	-	-	-	-	-	-
	-5	C(3)	C	-	-	-	-	-	-
XCS10XL	-4	C(3)	C, I	C(3)	C	-	-	-	-
	-5	C(3)	C	C(3)	C	-	-	-	-
XCS20XL	-4	-	C, I	C(3)	C, I	C, I	-	-	-
	-5	-	C	C(3)	C	C	-	-	-
XCS30XL	-4	-	C, I	-	C, I	C, I	C	C	C(3)
	-5	-	C	-	C	C	C	C	C(3)
XCS40XL	-4	-	-	-	-	C, I	C	C, I	C(3)
	-5	-	-	-	-	C	C	C	C(3)

6/25/08

Notes:

1. C = Commercial T_J = 0° to +85°C
2. I = Industrial T_J = –40°C to +100°C
3. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by PDN2004-01
4. Some Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Package Specifications

Package drawings and material declaration data sheets for the Spartan/XL devices can be found on the Xilinx website at:

www.xilinx.com/support/documentation/spartan-xl.htm#19687

Thermal data for the Spartan/XL packages can be found using the thermal query tool on the Xilinx website at:

www.xilinx.com/cgi-bin/thermal/thermal.pl