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AMD Xilinx - XCS40XL-4PQ240C Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	192
Number of Gates	40000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40xl-4pq240c

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This high value makes them unsuitable as wired-AND pull-up resistors.

Table 7: Supported Destinations for Spartan/XL Outputs

	Spartan-XL Outputs	Spa Out	rtan puts
Destination	3.3V, CMOS	5V, TTL	5V, CMOS
Any device, V _{CC} = 3.3V, CMOS-threshold inputs	V	\checkmark	Some ⁽¹⁾
Any device, V _{CC} = 5V, TTL-threshold inputs	\checkmark	\checkmark	\checkmark
Any device, V _{CC} = 5V, CMOS-threshold inputs	Unreliable Data		V

Notes:

1. Only if destination device has 5V tolerant inputs.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULL-DOWN library component to the net attached to the pad.

Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops (Figure 5). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (see EC signal in Figure 5), which through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan/XL FPGA CLB. It cannot be inverted within the IOB.

Routing Channel Description

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

This section describes the routing channels available in Spartan/XL devices. Figure 8 shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the designer should open a design in the FPGA Editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

CLB Routing Channels

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). Figure 8 shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.



DS060 13 080400

Figure 13: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO} , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS} , the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by A[3:0] while the second provides only for read operations at the address specified independently by DPRA[3:0]. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the



Figure 14: Logic Diagram for the Dual-Port RAM

CLB signals from which they are originally derived are shown in Table 10.

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port.	F[4:1]
	Write Address for Single-Port and Dual-Port.	
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	К
SPO	Single Port Out (addressed by A[3:0])	F _{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G _{OUT}

Table 10: Dual-Port RAM Signals

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

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RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan



Figure 15: Available Spartan/XL Carry Propagation Paths

On-Chip Oscillator

Spartan/XL devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, V_{CC} , and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8-MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in Figure 3, page 5 for the CLB and Figure 5, page 6 for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 19.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

Global 3-State

A separate Global 3-state line (GTS) as shown in Figure 6, page 7 forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in Figure 19 for GSR except the IBUF would be

connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-state signal. Alternatively, GTS can be driven from any internal node.



Figure 19: Symbols for Global Set/Reset

Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan compatible device. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan and Spartan-XL families implement IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Spartan/XL devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "*Boundary Scan in FPGA Devices*."

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. PRO-GRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.

Even if the boundary scan symbol is used in a design, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state.
- TCK: Tie High or Low-do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "*Boundary Scan in FPGA Devices*."

Boundary Scan Enhancements (Spartan-XL Family Only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

IDCODE: The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc1
```

where

c = the company code (49h for Xilinx)

a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)

f = the family code (02h for Spartan-XL family)

v = the die version number

Table	13:	IDCODEs	Assigned to	Spartan-XL	FPGAs
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FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

Configuration State: The configuration state is available to JTAG controllers.

Configuration Disable: The JTAG port can be prevented from configuring the FPGA.

TCK Startup: TCK can now be used to clock the start-up block in addition to other user clocks.

CCLK Holdoff: Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

Reissue Configure: The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

Bypass FF: Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

Power-Down (Spartan-XL Family Only)

All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low power-down pin (PWRDWN) to reduce supply current to 100 μ A typical. The PWRDWN pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The PWRDWN pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

 V_{CC} must continue to be supplied during Power-down, and configuration data is maintained. When the PWRDWN pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The PROGRAM pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

PWRDWN has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before PWRDWN to affect the order of events. When the PWRDWN signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of PWRDWN before using the device. figuration are shown in Table 14 and Table 15.

Table 14: Pin Functions During Configuration (Spartan Family Only)

Configuration Mo		
Slave Serial (High)	Master Serial (Low)	User Operation
MODE (I)	MODE (I)	MODE
HDC (High)	HDC (High)	I/O
LDC (Low)	LDC (Low)	I/O
INIT	INIT	I/O
DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	ТСК	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
	·	ALL OTHERS

Notes:

- A shaded table cell represents the internal pull-up used 1. before and during configuration.
- 2. (I) represents an input; (O) represents an output.
- **INIT** is an open-drain output during configuration. З.

Table 15: Pin Functions During Configuration (Spartan-XL Family Only)

CONFIGU			
Slave Serial [1:1]	Master Serial [1:0]	Express [0:X]	User Operation
M1 (High) (I)	M1 (High) (I)	M1(Low) (I)	M1
M0 (High) (I)	M0 (Low) (I)	M0 (I)	MO
HDC (High)	HDC (High)	HDC (High)	I/O
LDC (Low)	LDC (Low)	LDC (Low)	I/O
INIT	INIT	INIT	I/O
DONE	DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

Notes:

- A shaded table cell represents the internal pull-up used 1. before and during configuration.
- (I) represents an input; (O) represents an output. INIT is an open-drain output during configuration. 2.
- 3.

Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the

falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in Figure 24.

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Earlier families such as the XC3000 series do not support the Fast Configuration Rate option.

The SPROM <u>CE</u> input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

Figure 25 shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Symbol	Description	Min	Units
CCLK	T _{DSCK}	DIN setup	20	ns
COLK	T _{CKDS}	DIN hold	0	ns

Notes:

- 1. At power-up, V_{CC} must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling PROGRAM Low until V_{CC} is valid.
- 2. Master Serial mode timing is based on testing in slave mode.

Figure 24: Master Serial Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 25 shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.



Figure 25: Master/Slave Serial Mode Circuit Diagram



DS060 28 080400

Symbol		Description	Min	Max	Units
T _{IC}		INIT (High) setup time	5	-	μs
T _{DC}		D0-D7 setup time	20	-	ns
T _{CD}	CCLK	D0-D7 hold time	0	-	ns
Т _{ССН}	COLK	CCLK High time	45	-	ns
T _{CCL}		CCLK Low time	45	-	ns
F _{CC}		CCLK Frequency	-	10	MHz

Notes:

1. If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: Express Mode Programming Switching Characteristics

Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL family Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 16. Bit-serial data is read from left to right. Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL family Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 17). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

Table 16: Spartan/XL Data Stream Formats

Data Type	Serial Modes (D0)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0] ⁽¹⁾
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	1111110b ⁽²⁾
Data Frame	DATA[n-1:0]	DATA[n-1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes ⁽³⁾	FFh	FFFFFFFFFFFF

Legend:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Notes:

- 1. Not used by configuration logic.
- 2. 11111111b for XCS40XL only.
- 3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the INIT pin. In Master serial mode, CCLK continues to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the PROGRAM pin Low or cycling V_{CC} .

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the INIT pin Low and goes into a Wait state.



DS060_39_082801



Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with INIT held Low (or drive the PROGRAM pin Low for more than 300 ns followed by a High while holding INIT Low). Holding INIT Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold INIT Low.
- Issue the CONFIG command to the TMS input.

- Wait for INIT to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after $\overline{\rm INIT}$ goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and Spartan-XL devices.

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Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be

met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 16 and Table 17.

Configuration Switching Characteristics



DS060_33_080400

Master Mode

Symbol	Description	Min	Мах	Units
T _{POR}	Power-on reset	40	130	ms
T _{PI}	Program Latency	30	200	μs per CLB column
T _{ICCK}	CCLK (output) delay	40	250	μs
T _{CCLK}	CCLK (output) period, slow	640	2000	ns
T _{CCLK}	CCLK (output) period, fast	100	250	ns

Slave Mode

Symbol	Description	Min	Мах	Units
T _{POR}	Power-on reset	10	33	ms
T _{PI}	Program latency	30	200	μs per CLB column
Т _{ІССК}	CCLK (input) delay (required)	4	-	μs
T _{CCLK}	CCLK (input) period (required)	80	-	ns

Spartan and Spartan-XL FPGA Families Data Sheet

Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

	Description	-	-4	-	3	
Symbol	Description	Min	Max	Min	Мах	Units
Clocks	· · · · · · · · · · · · · · · · · · ·		<u></u>		·	·
Т _{СН}	Clock High time	3.0	-	4.0	-	ns
T _{CL}	Clock Low time	3.0	-	4.0	-	ns
Combina	torial Delays					
T _{ILO}	F/G inputs to X/Y outputs	-	1.2	-	1.6	ns
Т _{ІНО}	F/G inputs via H to X/Y outputs	-	2.0	-	2.7	ns
T _{HH10}	C inputs via H1 via H to X/Y outputs	-	1.7	-	2.2	ns
CLB Fast	Carry Logic					
T _{OPCY}	Operand inputs (F1, F2, G1, G4) to C _{OUT}	-	1.7	-	2.1	ns
T _{ASCY}	Add/Subtract input (F3) to C _{OUT}	-	2.8	-	3.7	ns
T _{INCY}	Initialization inputs (F1, F3) to C _{OUT}	-	1.2	-	1.4	ns
T _{SUM}	C _{IN} through function generators to X/Y outputs	-	2.0	-	2.6	ns
T _{BYP}	C _{IN} to C _{OUT} , bypass function generators	-	0.5	-	0.6	ns
Sequentia	al Delays		1	1		
Т _{СКО}	Clock K to Flip-Flop outputs Q	-	2.1	-	2.8	ns
Setup Tin	ne before Clock K		1	1		
Т _{ІСК}	F/G inputs	1.8	-	2.4	-	ns
T _{IHCK}	F/G inputs via H	2.9	-	3.9	-	ns
T _{HH1CK}	C inputs via H1 through H	2.3	-	3.3	-	ns
T _{DICK}	C inputs via DIN	1.3	-	2.0	-	ns
T _{ECCK}	C inputs via EC	2.0	-	2.6	-	ns
T _{RCK}	C inputs via S/R, going Low (inactive)	2.5	-	4.0	-	ns
Hold Tim	e after Clock K		1	1		
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset	t Direct					
T _{RPW}	Width (High)	3.0	-	4.0	-	ns
T _{RIO}	Delay from C inputs via S/R, going High to Q	-	3.0	-	4.0	ns
Global Se	et/Reset					
T _{MRW}	Minimum GSR pulse width	11.5	-	13.5	-	ns
T _{MRQ}	Delay from GSR input to any Q	See <mark>pa</mark>	ge 50 for T _{RI}	_{RI} values per	r device.	
F _{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	166	-	125	MHz

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

			-	4	-	3	
Symbol	Single Port RAM	Size ⁽¹⁾	Min	Max	Min	Max	Units
Write Ope	ration	<u> </u>					
T _{WCS}	Address write cycle time (clock K period)	16x2	8.0	-	11.6	-	ns
T _{WCTS}		32x1	8.0	-	11.6	-	ns
T _{WPS}	Clock K pulse width (active edge)	16x2	4.0	-	5.8	-	ns
T _{WPTS}		32x1	4.0	-	5.8	-	ns
T _{ASS}	Address setup time before clock K	16x2	1.5	-	2.0	-	ns
T _{ASTS}		32x1	1.5	-	2.0	-	ns
T _{AHS}	Address hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{AHTS}		32x1	0.0	-	0.0	-	ns
T _{DSS}	DIN setup time before clock K	16x2	1.5	-	2.7	-	ns
T _{DSTS}		32x1	1.5	-	1.7	-	ns
T _{DHS}	DIN hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{DHTS}		32x1	0.0	-	0.0	-	ns
T _{WSS}	WE setup time before clock K	16x2	1.5	-	1.6	-	ns
T _{WSTS}		32x1	1.5	-	1.6	-	ns
T _{WHS}	WE hold time after clock K	16x2	0.0	-	0.0	-	ns
T _{WHTS}		32x1	0.0	-	0.0	-	ns
T _{WOS}	Data valid after clock K	16x2	-	6.5	-	7.9	ns
T _{WOTS}		32x1	-	7.0	-	9.3	ns
Read Ope	ration	<u>.</u>					
T _{RC}	Address read cycle time	16x2	2.6	-	2.6	-	ns
T _{RCT}		32x1	3.8	-	3.8	-	ns
T _{ILO}	Data valid after address change (no Write	16x2	-	1.2	-	1.6	ns
T _{IHO}	Enable)	32x1	-	2.0	-	2.7	ns
Т _{ІСК}	Address setup time before clock K	16x2	1.8	-	2.4	-	ns
T _{IHCK}		32x1	2.9	-	3.9	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings⁽¹⁾

Symbol	Descrip	Value	Units	
V _{CC}	Supply voltage relative to GND		-0.5 to 4.0	V
V _{IN}	Input voltage relative to GND	5V Tolerant I/O Checked ^(2, 3)	-0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	–0.5 to V _{CC} + 0.5	V
V _{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked ^(2, 3)	-0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	–0.5 to V _{CC} + 0.5	V
T _{STG}	Storage temperature (ambient)		-65 to +150	°C
Т _Ј	Junction temperature	Plastic packages	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

2. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.

 With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to -2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

4. Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.

 Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0V or overshoot to V_{CC} + 2.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

6. For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V _{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}C$ to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}C$ to $+100^{\circ}C^{(1)}$	Industrial	3.0	3.6	V
V _{IH}	High-level input voltage ⁽²⁾		50% of V_{CC}	5.5	V
V _{IL}	Low-level input voltage ⁽²⁾		0	30% of V_{CC}	V
T _{IN}	Input signal transition time		-	250	ns

Notes:

1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

2. Input and output measurement threshold is ~50% of V_{CC}.

Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Тур.	Max	Units
V _{OH}	High-level output voltage @ $I_{OH} = -4.0$ mA, V _C	_C min (LVTTL)	2.4	-	-	V
	High-level output voltage @ $I_{OH} = -500 \ \mu$ A, (LV	CMOS)	90% V _{CC}	-	-	V
V _{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CO}	min (LVTTL) ⁽¹⁾	-	-	0.4	V
	Low-level output voltage @ I _{OL} = 24.0 mA, V _{CC}	min (LVTTL) ⁽²⁾	-	-	0.4	V
	Low-level output voltage @ $I_{OL} = 1500 \ \mu$ A, (LVC	$I_{OL} = 1500 \ \mu$ A, (LVCMOS) ge (below which configuration data		-	10% V _{CC}	V
V _{DR}	Data retention supply voltage (below which cor may be lost)	bltage (below which configuration data		-	-	V
I _{CCO}	Quiescent FPGA supply current ^(3,4)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I _{CCPD}	Power Down FPGA supply current ^(3,5)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
١L	Input or output leakage current	rrent		-	10	μA
C _{IN}	Input capacitance (sample tested)		-	-	10	pF
I _{RPU}	Pad pull-up (when selected) @ V _{IN} = 0V (samp	le tested)	0.02	-	0.25	mA
I _{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3V$ (s	sample tested)	0.02	-	-	mA

Notes:

1. With up to 64 pins simultaneously sinking 12 mA (default mode).

2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).

3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.

4. With no output current loads, no active input resistors, and all package pins at V_{CC} or GND.

5. With PWRDWN active.

Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CC} lines for a successful power on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Мах	Units
I _{CCPO}	Total V _{CC} supply current required during power-on	100	-	mA
T _{CCPO}	V _{CC} ramp time ^(2,3)	-	50	ms

Notes:

1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CC} ramps from 0 to 3.3V.

2. The ramp time is measured from GND to V_{CC} max on a fully loaded board.

3. V_{CC} must not dip in the negative direction during power on.

Spartan and Spartan-XL FPGA Families Data Sheet

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

			-	5	-	4	
Symbol	Single Port RAM	Size ⁽¹⁾	Min	Max	Min	Max	Units
Write Oper	ration		<u>.</u>	·			
T _{WCS}	Address write cycle time (clock K period)	16x2	7.7	-	8.4	-	ns
T _{WCTS}		32x1	7.7	-	8.4	-	ns
T _{WPS}	Clock K pulse width (active edge)	16x2	3.1	-	3.6	-	ns
T _{WPTS}		32x1	3.1	-	3.6	-	ns
T _{ASS}	Address setup time before clock K	16x2	1.3	-	1.5	-	ns
T _{ASTS}		32x1	1.5	-	1.7	-	ns
T _{DSS}	DIN setup time before clock K	16x2	1.5	-	1.7	-	ns
T _{DSTS}		32x1	1.8	-	2.1	-	ns
T _{WSS}	WE setup time before clock K	16x2	1.4	-	1.6	-	ns
T _{WSTS}		32x1	1.3	-	1.5	-	ns
	All hold times after clock K	16x2	0.0	-	0.0	-	ns
T _{WOS}	Data valid after clock K	32x1	-	4.5	-	5.3	ns
T _{WOTS}		16x2	-	5.4	-	6.3	ns
Read Oper	ration						
T _{RC}	Address read cycle time	16x2	2.6	-	3.1	-	ns
T _{RCT}		32x1	3.8	-	5.5	-	ns
T _{ILO}	Data Valid after address change (no Write	16x2	-	1.0	-	1.1	ns
Τ _{ΙΗΟ}	Enable)	32x1	-	1.7	-	2.0	ns
Т _{ІСК}	Address setup time before clock K	16x2	0.6	-	0.7	-	ns
T _{IHCK}		32x1	1.3	-	1.6	-	ns

Notes:

1. Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

			Speed Grade				
				5	-	4	
Symbol	Description	Device	Min	Max	Min	Max	Units
Propagation	Delays		<u></u>	·	·	<u></u>	
T _{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.2	-	3.7	ns
T _{OPF}	Output (O) to Pad, fast	All devices	-	2.5	-	2.9	ns
T _{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	2.8	-	3.3	ns
T _{TSONF}	3-state to Pad active and valid, fast	All devices	-	2.6	-	3.0	ns
T _{OFPF}	Output (O) to Pad via Output MUX, fast	All devices	-	3.7	-	4.4	ns
T _{OKFPF}	Select (OK) to Pad via Output MUX, fast	All devices	-	3.3	-	3.9	ns
T _{SLOW}	For Output SLOW option add	All devices	-	1.5	-	1.7	ns
Setup and H	old Times			L	L.		
т _{оок}	Output (O) to clock (OK) setup time	All devices	0.5	-	0.5	-	ns
т _{око}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T _{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	0.0	-	0.0	-	ns
T _{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.1	-	0.2	-	ns
Global Set/R	eset			L	Ľ		
T _{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T _{RPO}	Delay from GSR input to any Pad	XCS05XL	-	11.9	-	14.0	ns
		XCS10XL	-	12.4	-	14.5	ns
		XCS20XL	-	12.9	-	15.0	ns
		XCS30XL	-	13.9	-	16.0	ns
		XCS40XL	-	14.9	-	17.0	ns

Notes:

1. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.

2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.