AMD Xilinx - XCS40XL-4PQG208C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	169
Number of Gates	40000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40xl-4pqg208c

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 5 on the CK line.

The Spartan family IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL family IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See **Global Nets and Buffers**, page 12 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.The output of the input register goes to the routing channels (via I1 and I2 in Figure 6). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan family input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds, using an option in the bitstream generation software. The Spartan family output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan family inputs are in TTL mode. Input and output thresholds are TTL on all configuration pins until the configuration has been loaded into the device and specifies how they are to be used. Spartan-XL family inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 4.

Spartan-XL family I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL family inputs without damage, as shown in Table 4. In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.

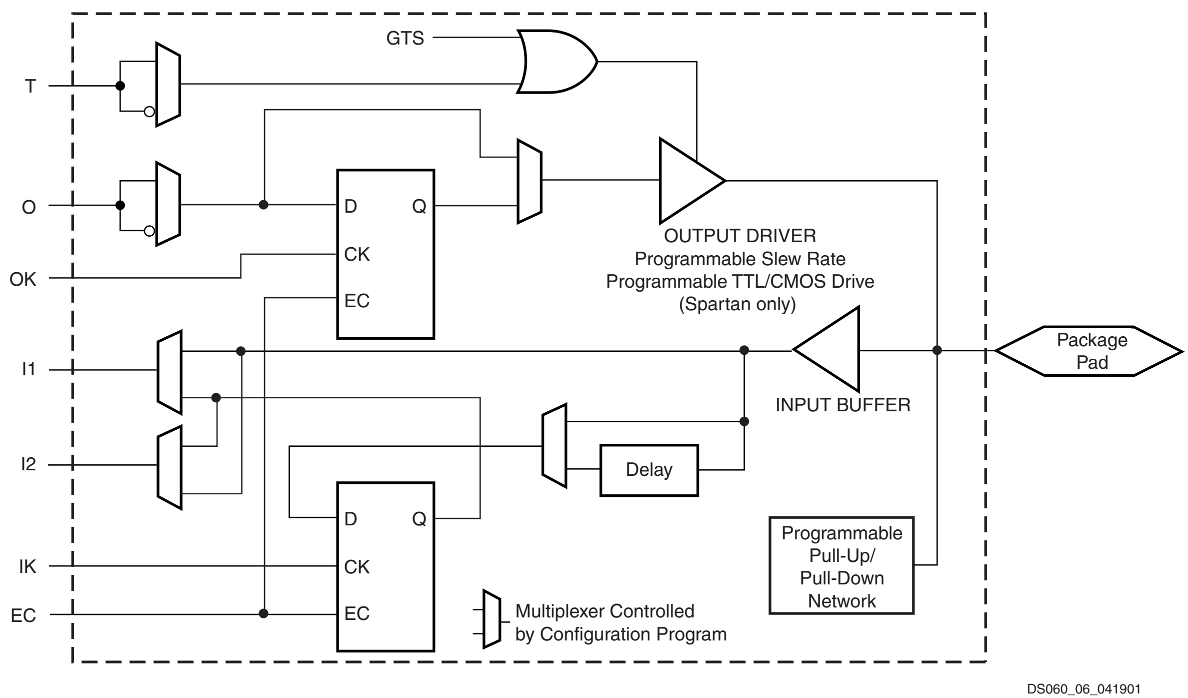

Figure 6: **Simplified Spartan/XL IOB Block Diagram**

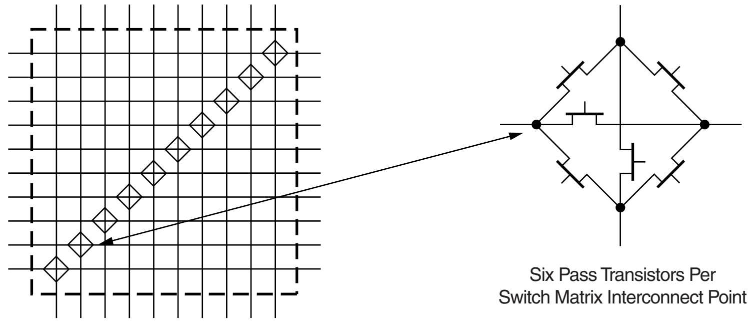

Figure 10: **Programmable Switch Matrix**

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 8).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 8. The longlines also interface to some 3-state buffers which is described later in **3-State Long Line Drivers**, page 19.

I/O Routing

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 11. In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.

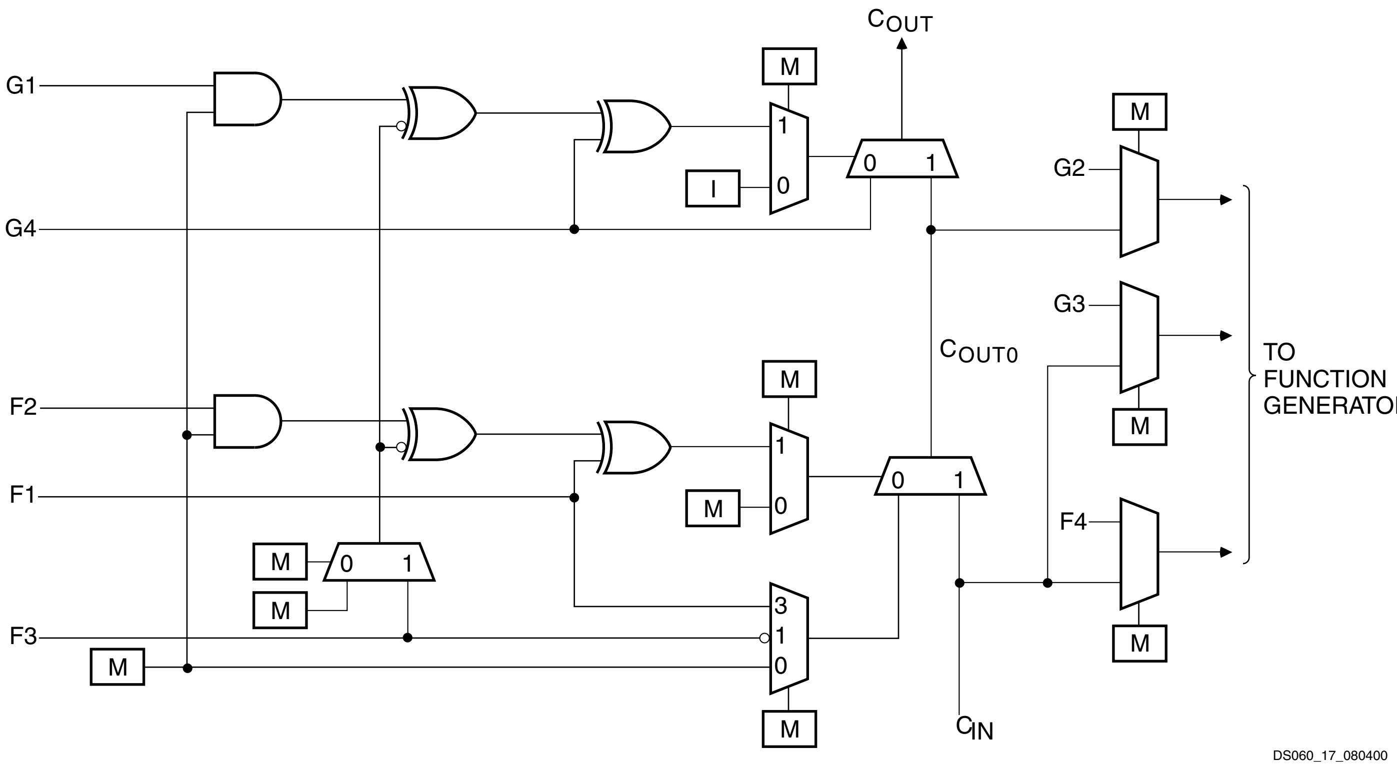

Figure 17: **Detail of Spartan/XL Dedicated Carry Logic**

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal long-lines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

Table 11: **Three-State Buffer Functionality**

IN	T	OUT
X	1	Z
IN	0	IN

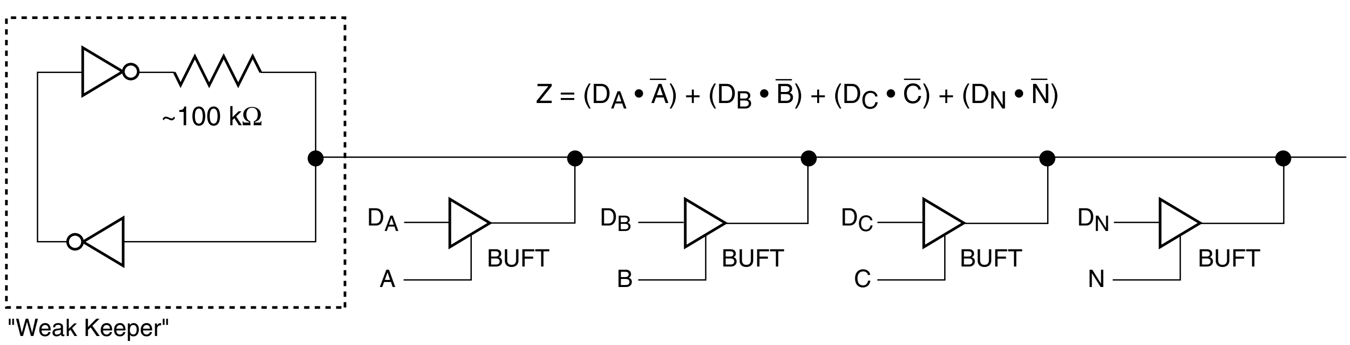

Figure 18: **3-state Buffers Implement a Multiplexer**

On-Chip Oscillator

Spartan/XL devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, V_{CC}, and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8-MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in Figure 3, page 5 for the CLB and Figure 5, page 6 for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 19.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

Global 3-State

A separate Global 3-state line (GTS) as shown in Figure 6, page 7 forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in Figure 19 for GSR except the IBUF would be connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-state signal. Alternatively, GTS can be driven from any internal node.

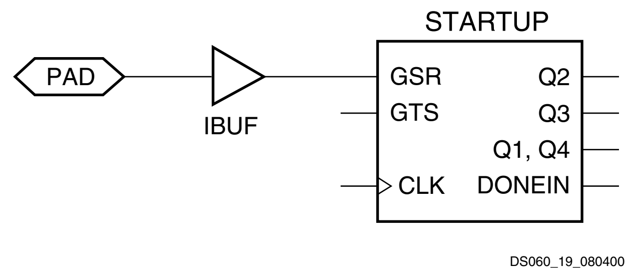

Figure 19: **Symbols for Global Set/Reset**

Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan compatible device. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan and Spartan-XL families implement IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Spartan/XL devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "*Boundary Scan in FPGA Devices*."

Even if the boundary scan symbol is used in a design, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state.
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "*Boundary Scan in FPGA Devices*."

Boundary Scan Enhancements (Spartan-XL Family Only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

IDCODE: The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

c = the company code (49h for Xilinx)

a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)

f = the family code (02h for Spartan-XL family)

v = the die version number

Table 13: **IDCODEs Assigned to Spartan-XL FPGAs**

FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

Configuration State: The configuration state is available to JTAG controllers.

Configuration Disable: The JTAG port can be prevented from configuring the FPGA.

TCK Startup: TCK can now be used to clock the start-up block in addition to other user clocks.

CCLK Holdoff: Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

Reissue Configure: The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

Bypass FF: Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

Power-Down (Spartan-XL Family Only)

All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low power-down pin (PWRDWN) to reduce supply current to 100 µA typical. The PWRDWN pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The PWRDWN pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

V_{CC} must continue to be supplied during Power-down, and configuration data is maintained. When the PWRDWN pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The PROGRAM pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

PWRDWN has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before PWRDWN to affect the order of events. When the PWRDWN signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of PWRDWN before using the device.

figuration are shown in Table 14 and Table 15.

Table 14: **Pin Functions During Configuration (Spartan Family Only)**

Configuration Mode (MODE Pin)		User Operation
Slave Serial (High)	**Master Serial (Low)**	
MODE (I)	MODE (I)	MODE
HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

Notes:
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Table 15: **Pin Functions During Configuration (Spartan-XL Family Only)**

CONFIGURATION MODE <M1:M0>			User Operation
Slave Serial [1:1]	**Master Serial [1:0]**	**Express [0:X]**	
M1 (High) (I)	M1 (High) (I)	M1(Low) (I)	M1
M0 (High) (I)	M0 (Low) (I)	M0 (I)	M0
HDC (High)	HDC (High)	HDC (High)	I/O
$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	$\overline{\text{LDC}}$ (Low)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

Notes:
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.

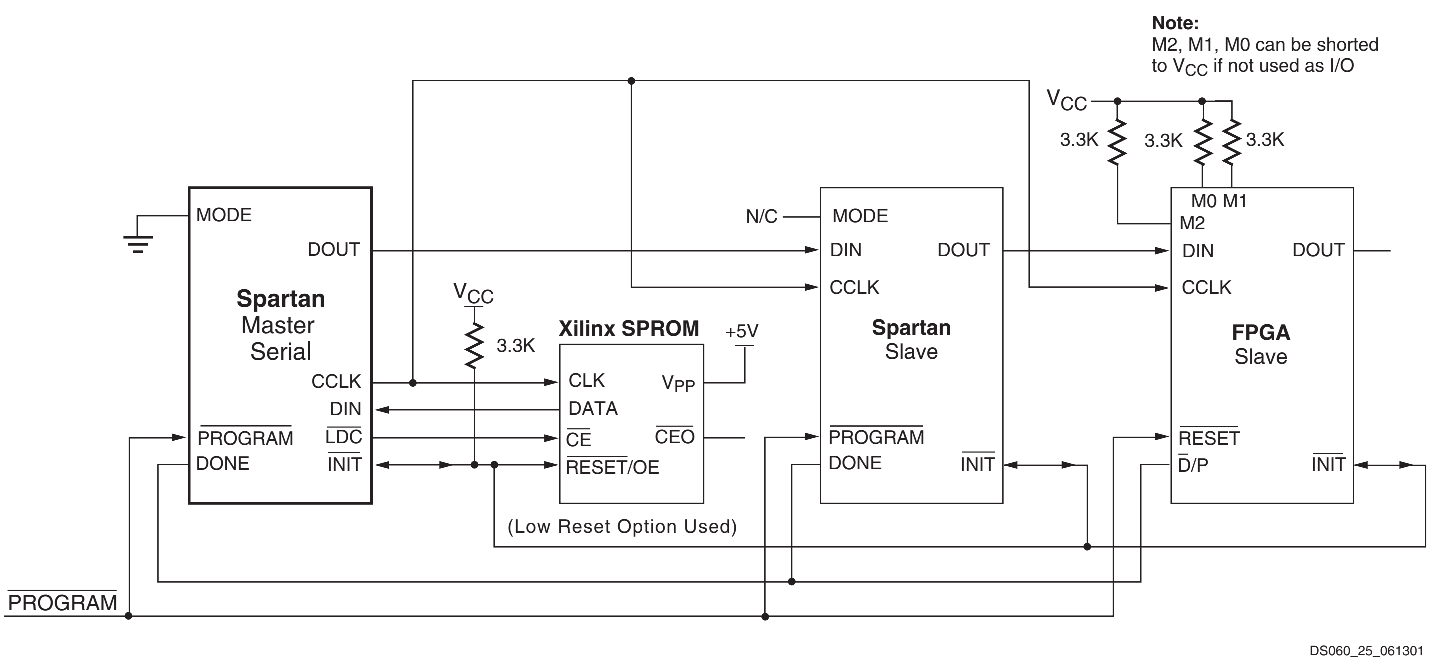

Figure 25: **Master/Slave Serial Mode Circuit Diagram**

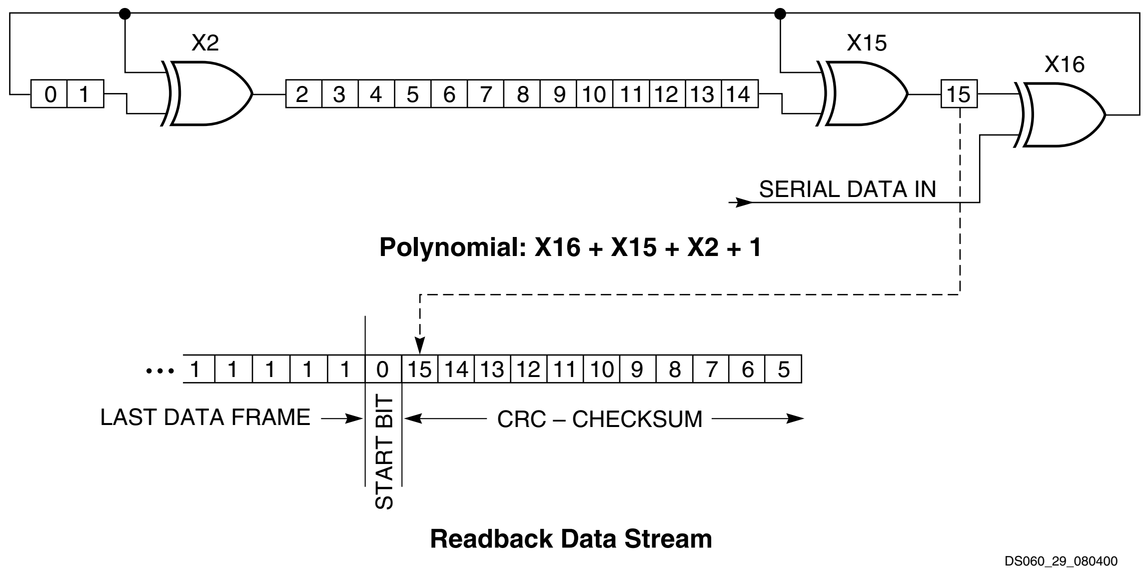

Figure 29: **Circuit for Generating CRC-16**

Configuration Sequence

There are four major steps in the Spartan/XL FPGA power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC}. When all $\overline{\text{INIT}}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{\text{PROGRAM}}$ pin Low. During this time delay, or as long as the $\overline{\text{PROGRAM}}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{\text{PROGRAM}}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{\text{INIT}}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{\text{LDC}}$, $\overline{\text{INIT}}$ and DONE provide status outputs for the system interface. The outputs $\overline{\text{LDC}}$, $\overline{\text{INIT}}$ and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain $\overline{\text{INIT}}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive $\overline{\text{INIT}}$. Two internal clocks after the $\overline{\text{INIT}}$ pin is recognized as High, the device samples the MODE pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

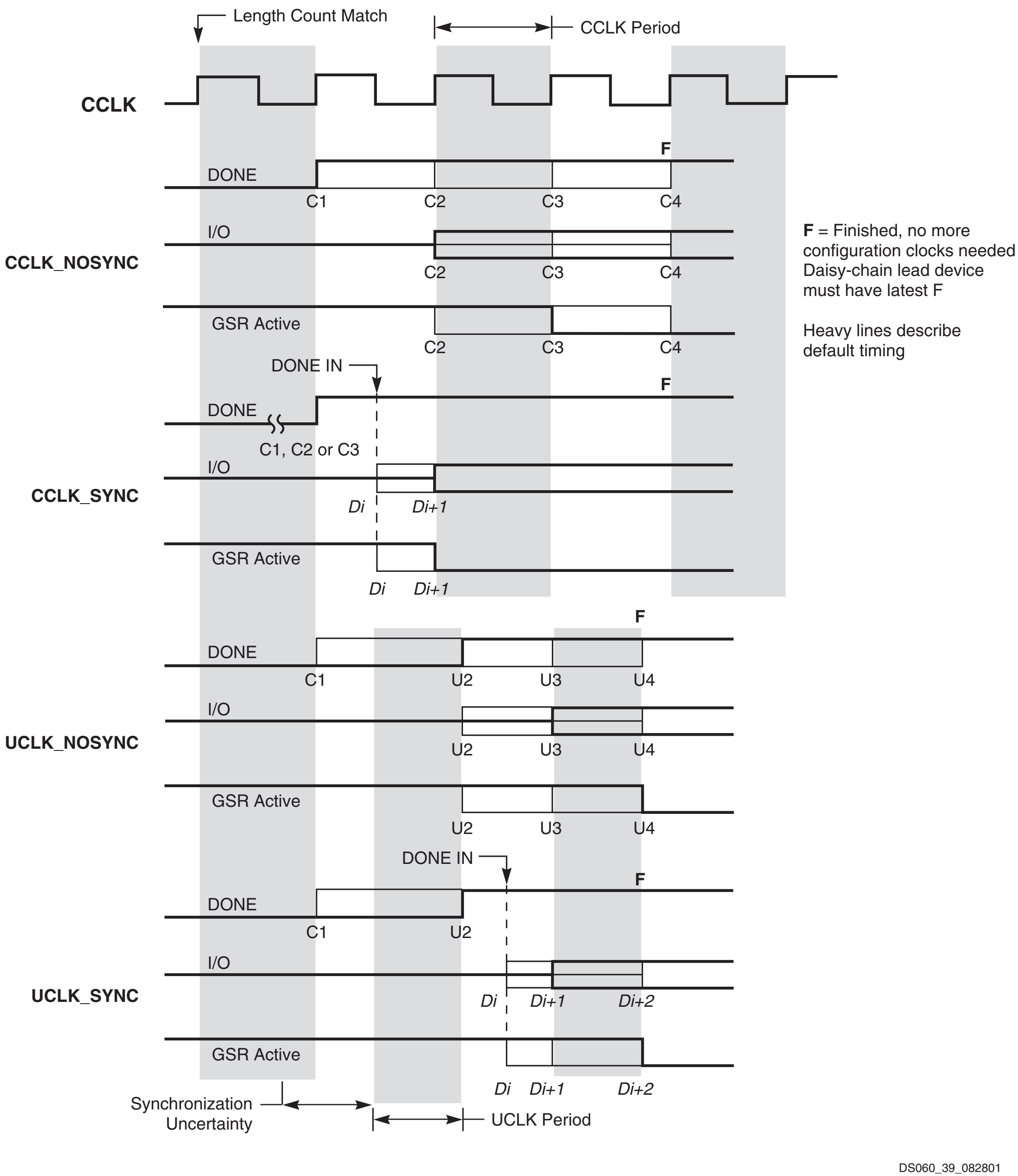

Figure 31: **Start-up Timing**

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with INIT held Low (or drive the PROGRAM pin Low for more than 300 ns followed by a High while holding INIT Low). Holding INIT Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold INIT Low.
- Issue the CONFIG command to the TMS input.
- Wait for INIT to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and Spartan-XL devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 32.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

Readback Capture

When the Readback Capture option is selected, the data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.

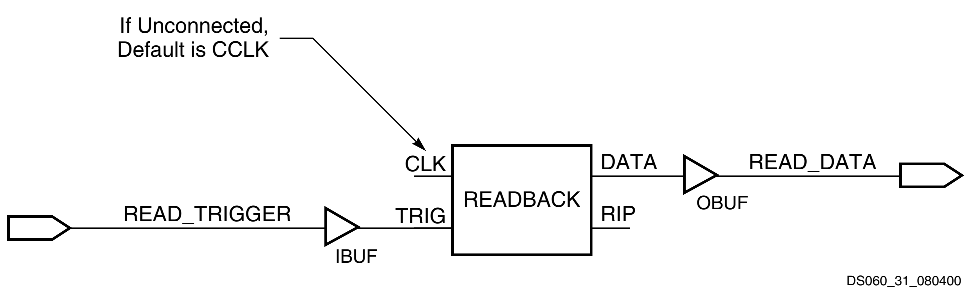

Figure 32: **Readback Example**

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 16 and Table 17.

Readback Switching Characteristics Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions.

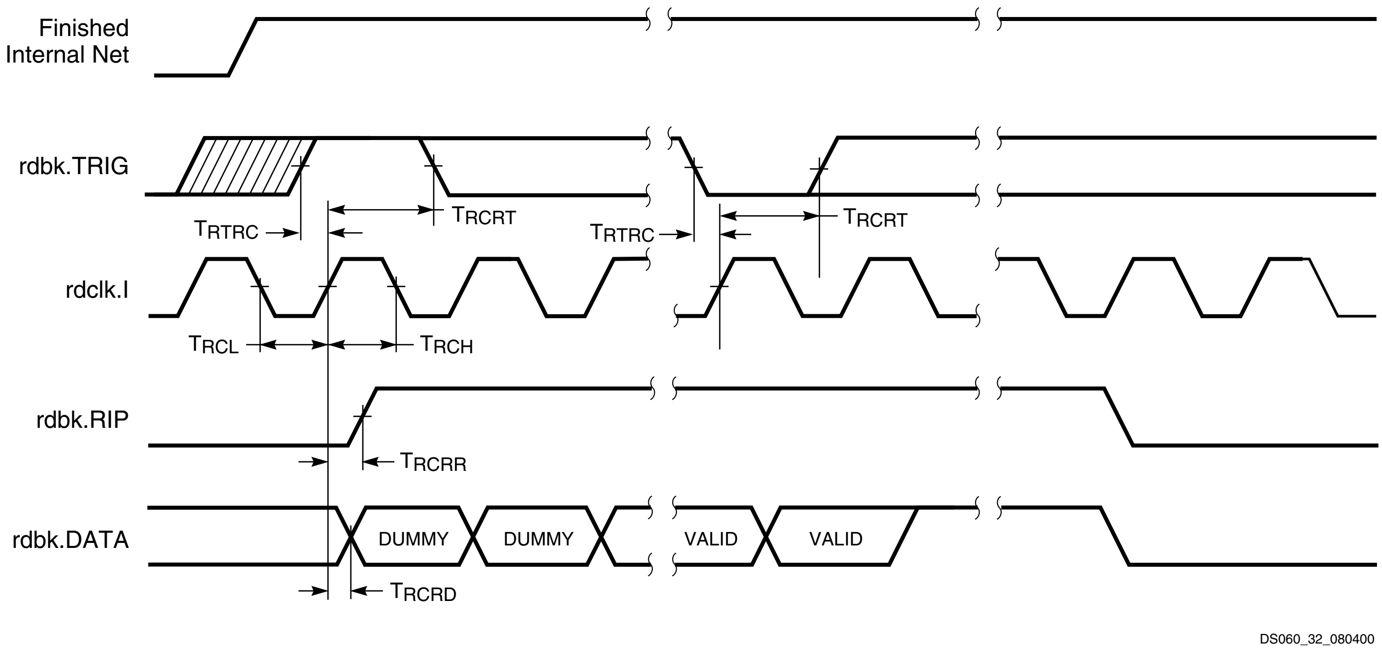

Figure 33: **Spartan and Spartan-XL Readback Timing Diagram**

Spartan and Spartan-XL Readback Switching Characteristics

Symbol		Description	Min	Max	Units
T_{RTRC}	rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	200	-	ns
T_{RCRT}		rdbk.TRIG hold to initiate and abort Readback	50	-	ns
T_{RCRD}	rdclk.I	rdbk.DATA delay	-	250	ns
T_{RCRR}		rdbk.RIP delay	-	250	ns
T_{RCH}		High time	250	500	ns
T_{RCL}		Low time	250	500	ns

Notes:
1. Timing parameters apply to all speed grades.
2. If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Spartan Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Spartan Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade -4 Max	Speed Grade -3 Max	Units
Global Primary Clock to TTL Output using OFF					
T_{ICKOF}	Fast	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
T_{ICKO}	Slew-rate limited	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
T_{ICKSOF}	Fast	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
T_{ICKSO}	Slew-rate limited	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
T_{CMOSOF}	Fast	All devices	0.8	1.0	ns
T_{CMOSO}	Slew-rate limited	All devices	1.5	2.0	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column,and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 34.
3. OFF = Output Flip-Flop

Capacitive Load Factor

Figure 34 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 34 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

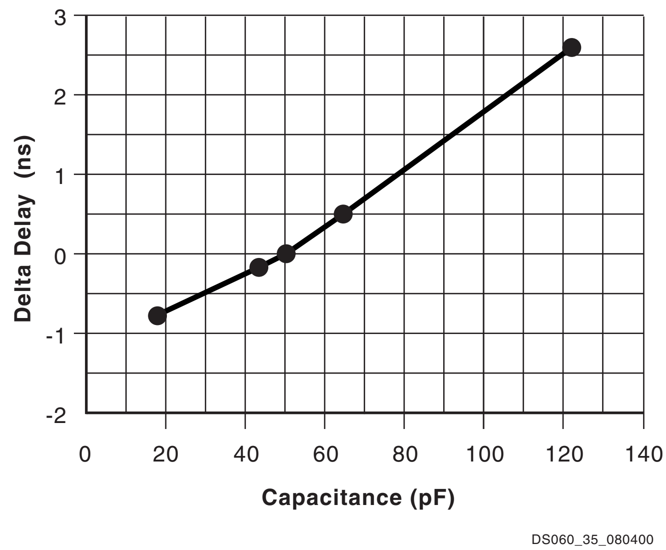

Figure 34: **Delay Factor at Various Capacitive Loads**

Spartan Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Family Primary and Secondary Setup and Hold

Symbol	Description	Device	Speed Grade -4 Min	Speed Grade -3 Min	Units
Input Setup/Hold Times Using Primary Clock and IFF					
T_{PSUF}/T_{PHF}	No Delay	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
T_{PSU}/T_{PH}	With Delay	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
T_{SSUF}/T_{SHF}	No Delay	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
T_{SSU}/T_{SH}	With Delay	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

Notes:
1. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.
2. IFF = Input Flip-flop or Latch

Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Typ.	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min (LVTTL)		2.4	-	-	V
	High-level output voltage @ I_{OH} = –500 µA, (LVCMOS)		90% V_{CC}	-	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (LVTTL)(1)		-	-	0.4	V
	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL)(2)		-	-	0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)		-	-	10% V_{CC}	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		2.5	-	-	V
I_{CCO}	Quiescent FPGA supply current(3,4)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I_{CCPD}	Power Down FPGA supply current(3,5)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I_L	Input or output leakage current		–10	-	10	µA
C_{IN}	Input capacitance (sample tested)		-	-	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V (sample tested)		0.02	-	-	mA

Notes:
1. With up to 64 pins simultaneously sinking 12 mA (default mode).
2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
4. With no output current loads, no active input resistors, and all package pins at V_{CC} or GND.
5. With $\overline{\text{PWRDWN}}$ active.

Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CC} lines for a successful power on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Max	Units
I_{CCPO}	Total V_{CC} supply current required during power-on	100	-	mA
T_{CCPO}	V_{CC} ramp time(2,3)	-	50	ms

Notes:
1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CC} ramps from 0 to 3.3V.
2. The ramp time is measured from GND to V_{CC} max on a fully loaded board.
3. V_{CC} must not dip in the negative direction during power on.

Spartan-XL Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade -5 Min	-5 Max	-4 Min	-4 Max	Units
Clocks						
T_{CH}	Clock High time	2.0	-	2.3	-	ns
T_{CL}	Clock Low time	2.0	-	2.3	-	ns
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	1.0	-	1.1	ns
T_{IHO}	F/G inputs via H to X/Y outputs	-	1.7	-	2.0	ns
T_{ITO}	F/G inputs via transparent latch to Q outputs	-	1.5	-	1.8	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.5	-	1.8	ns
Sequential Delays						
T_{CKO}	Clock K to Flip-Flop or latch outputs Q	-	1.2	-	1.4	ns
Setup Time before Clock K						
T_{ICK}	F/G inputs	0.6	-	0.7	-	ns
T_{IHCK}	F/G inputs via H	1.3	-	1.6	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	2.5	-	2.8	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	2.3	-	2.7	ns
Global Set/Reset						
T_{MRW}	Minimum GSR Pulse Width	10.5	-	11.5	-	ns
T_{MRQ}	Delay from GSR input to any Q	See page 60 for T_{RRI} values per device.				
F_{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	250	-	217	MHz

Spartan-XL Family Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Family Setup and Hold

Symbol	Description	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Input Setup/Hold Times Using Global Clock and IFF					
T_{SUF}/T_{HF}	No Delay	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
T_{SU}/T_H	Full Delay	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Capacitive Load Factor

Figure 35 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 35 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

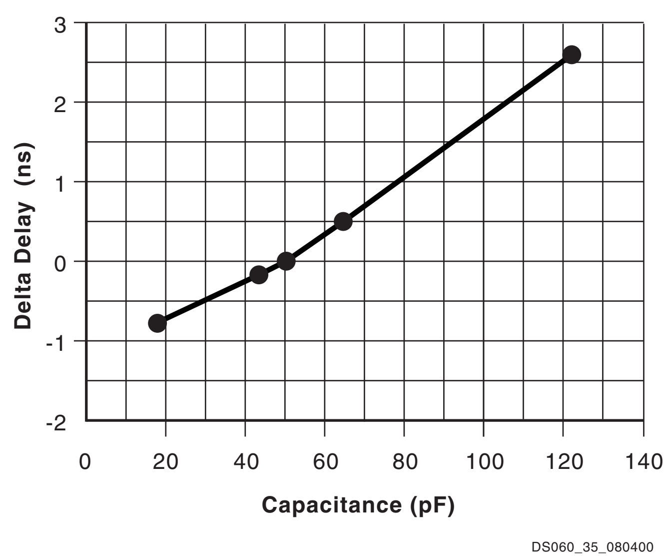

Figure 35: **Delay Factor at Various Capacitive Loads**

Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade -5 Min	-5 Max	-4 Min	-4 Max	Units
Setup Times							
T_{ECIK}	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T_{PICK}	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T_{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T_{PID}	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T_{Delay}	$T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T_{RRI}	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144(2,4)	TQ144	PQ208	Bndry Scan
PROGRAM	P52	M13	P74	P106	-
I/O (D7(2))	P53	L12	P75	P107	367 (3)
I/O, PGCK3(1), GCK5(2)	P54	L13	P76	P108	370 (3)
I/O	-	K10	P77	P109	373 (3)
I/O	-	K11	P78	P110	376 (3)
I/O (D6(2))	P55	K12	P79	P112	379 (3)
I/O	P56	K13	P80	P113	382 (3)
I/O	-	-	-	P114	385 (3)
I/O	-	-	-	P115	388 (3)
I/O	-	-	-	P116	391 (3)
I/O	-	-	-	P117	394 (3)
GND	-	J10	P81	P118	-
I/O	-	J11	P82	P119	397 (3)
I/O	-	J12	P83	P120	400 (3)
VCC(2)	-	-	-	P121	-
I/O (D5(2))	P57	J13	P84	P122	403 (3)
I/O	P58	H10	P85	P123	406 (3)
I/O	-	-	-	P124	409 (3)
I/O	-	-	-	P125	412 (3)
I/O	P59	H11	P86	P126	415 (3)
I/O	P60	H12	P87	P127	418 (3)
I/O (D4(2))	P61	H13	P88	P128	421 (3)
I/O	P62	G12	P89	P129	424 (3)
VCC	P63	G13	P90	P130	-
GND	P64	G11	P91	P131	-
I/O (D3(2))	P65	G10	P92	P132	427 (3)
I/O	P66	F13	P93	P133	430 (3)
I/O	P67	F12	P94	P134	433 (3)
I/O	-	F11	P95	P135	436 (3)
I/O	-	-	-	P136	439 (3)
I/O	-	-	-	P137	442 (3)
I/O (D2(2))	P68	F10	P96	P138	445 (3)
I/O	P69	E13	P97	P139	448 (3)
VCC(2)	-	-	-	P140	-
I/O	-	E12	P98	P141	451 (3)
I/O	-	E11	P99	P142	454 (3)
GND	-	E10	P100	P143	-
I/O	-	-	-	P145	457 (3)
I/O	-	-	-	P146	460 (3)
I/O	-	-	-	P147	463 (3)
I/O	-	-	-	P148	466 (3)
I/O (D1(2))	P70	D13	P101	P149	469 (3)
I/O	P71	D12	P102	P150	472 (3)
I/O	-	D11	P103	P151	475 (3)

XCS20 and XCS20XL Device Pinouts

XCS20/XL Pad Name	VQ100	CS144(2,4)	TQ144	PQ208	Bndry Scan
I/O	-	C13	P104	P152	478 (3)
I/O (D0(2), DIN)	P72	C12	P105	P153	481 (3)
I/O, SGCK4(1), GCK6(2) (DOUT)	P73	C11	P106	P154	484 (3)
CCLK	P74	B13	P107	P155	-
VCC	P75	B12	P108	P156	-
O, TDO	P76	A13	P109	P157	0
GND	P77	A12	P110	P158	-
I/O	P78	B11	P111	P159	2
I/O, PGCK4(1), GCK7(2)	P79	A11	P112	P160	5
I/O	-	D10	P113	P161	8
I/O	-	C10	P114	P162	11
I/O (CS1(2))	P80	B10	P115	P163	14
I/O	P81	A10	P116	P164	17
I/O	-	D9	P117	P166	20
I/O	-	-	-	P167	23
I/O	-	-	-	P168	26
I/O	-	-	-	P169	29
GND	-	C9	P118	P170	-
I/O	-	B9	P119	P171	32
I/O	-	A9	P120	P172	35
VCC(2)	-	-	-	P173	-
I/O	P82	D8	P121	P174	38
I/O	P83	C8	P122	P175	41
I/O	-	-	-	P176	44
I/O	-	-	-	P177	47
I/O	P84	B8	P123	P178	50
I/O	P85	A8	P124	P179	53
I/O	P86	B7	P125	P180	56
I/O	P87	A7	P126	P181	59
GND	P88	C7	P127	P182	-

2/8/00