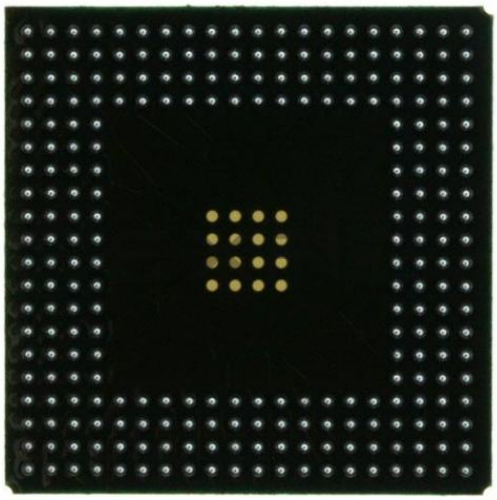


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	205
Number of Gates	40000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40xl-5bg256c

Spartan and Spartan-XL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In addition to the conventional benefit of high volume programmable logic solutions, Spartan series FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan/XL families leverage the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA process developments.

Logic Functional Description

The Spartan series uses a standard FPGA structure as shown in Figure 1, page 2. The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in Figure 2. There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the **Advanced Features Description**, page 13.

Function Generators

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box "A" of Figure 2). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.

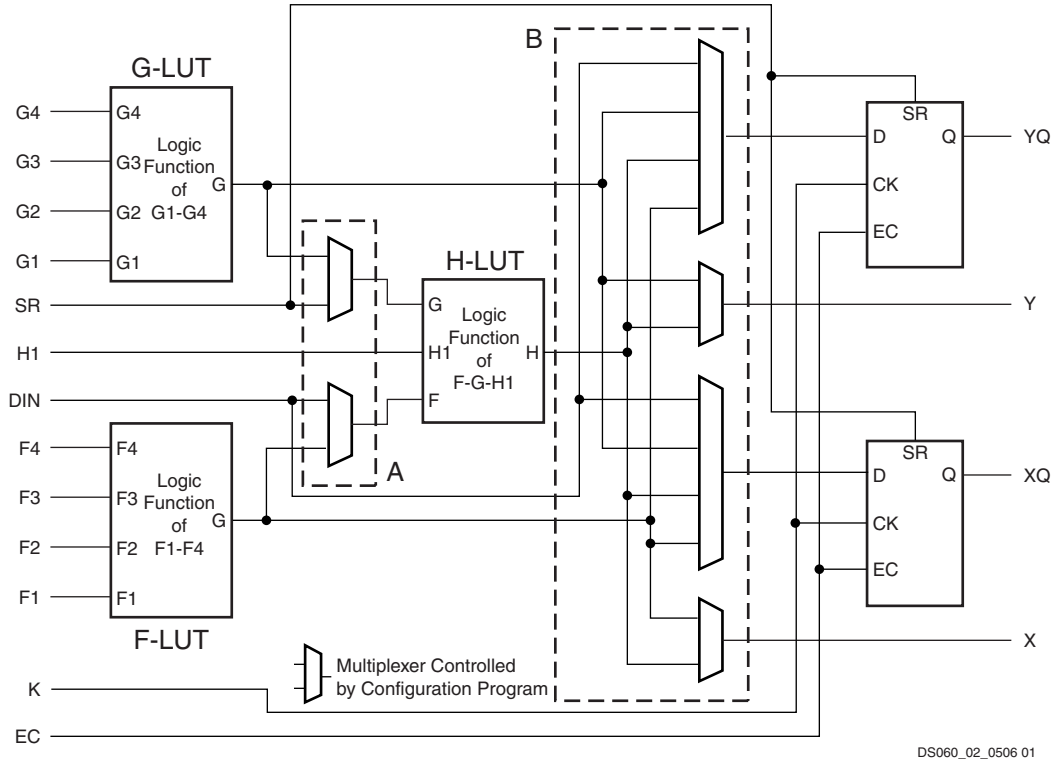


Figure 2: **Spartan/XL Simplified CLB Logic Diagram (some features not shown)**

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables

  Note: When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.
- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in **Global Signals: GSR and GTS**, page 20.

Latches (Spartan-XL Family Only)

The Spartan-XL family CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 2.

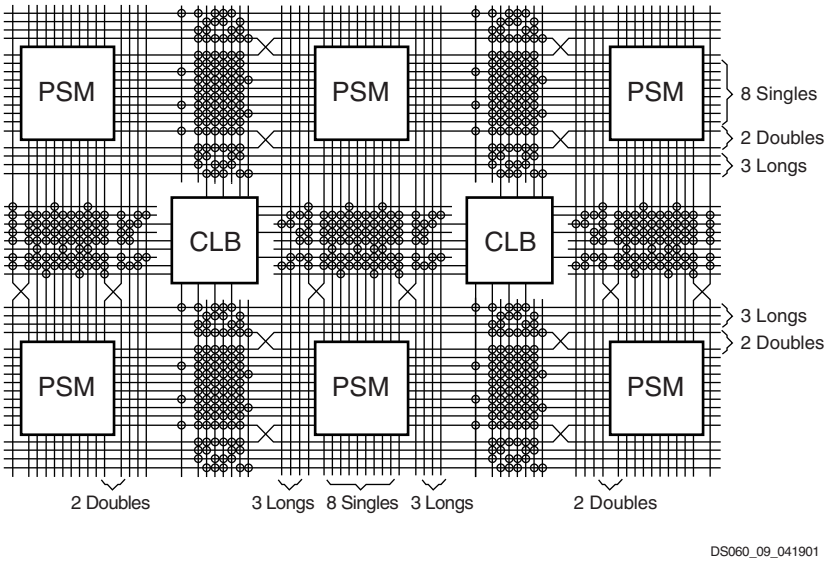


Figure 8: **Spartan/XL CLB Routing Channels and Interface Block Diagram**

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.

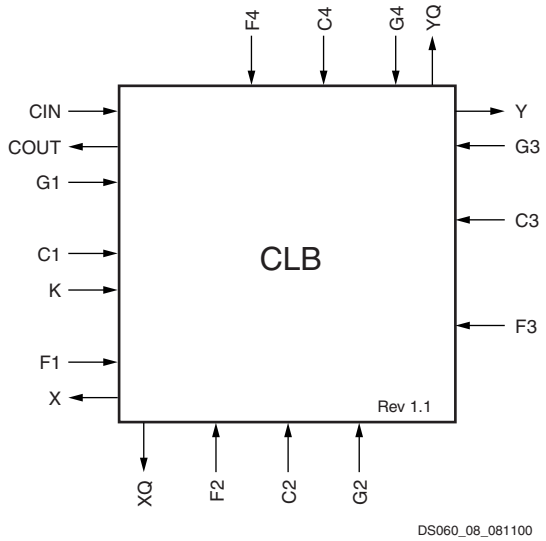


Figure 9: **CLB Interconnect Signals**

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs. Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. $\overline{\text{PROGRAM}}$, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.

Table 12: **Boundary Scan Instructions**

Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	IDCODE (Spartan-XL only)	IDCODE Register	-
1	1	1	BYPASS	Bypass Register	-

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-state. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 21. The device-specific pinout tables for the Spartan/XL devices include the boundary scan locations for each IOB pin.

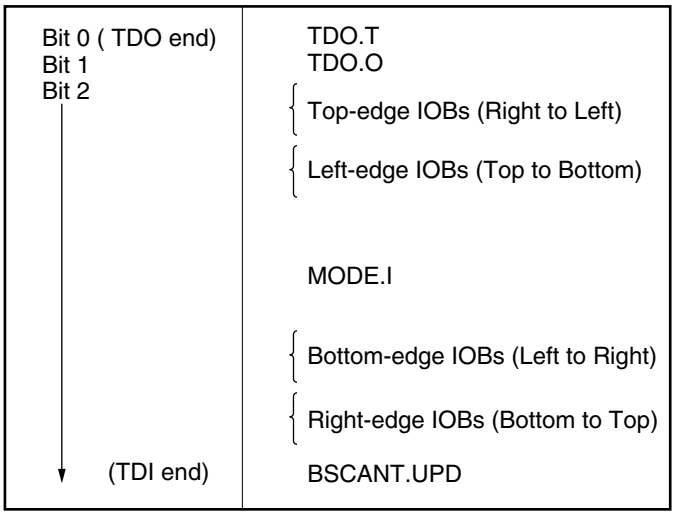


Figure 21: **Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Spartan/XL devices are available on the Xilinx website in the File Download area. Note that the 5V Spartan devices and 3V Spartan-XL devices have different BSDL files.

Including Boundary Scan in a Design

If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 22.

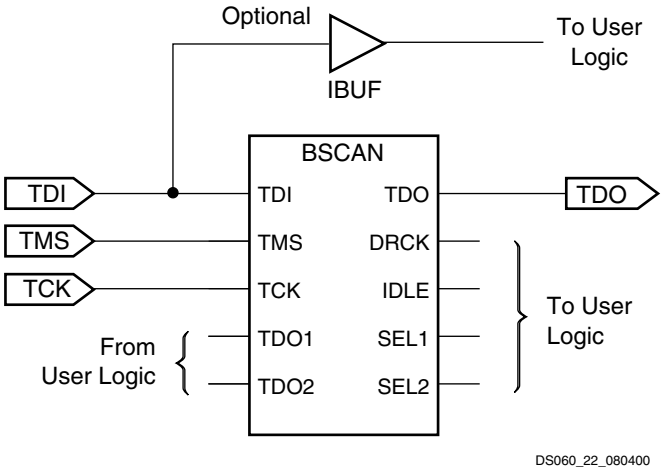


Figure 22: **Boundary Scan Example**

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.

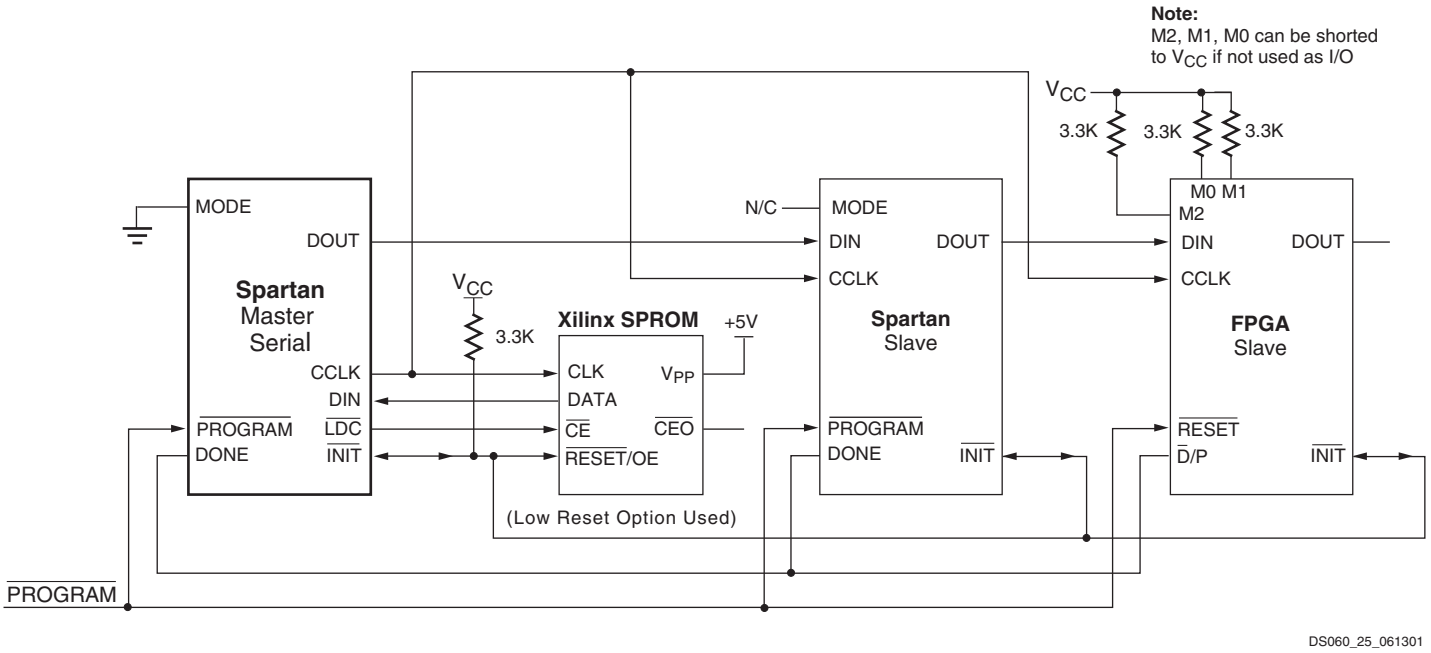


Figure 25: **Master/Slave Serial Mode Circuit Diagram**

Table 16: **Spartan/XL Data Stream Formats**

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0](1)
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	11111110b(2)
Data Frame	DATA[n–1:0]	DATA[n–1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes(3)	FFh	FFFFFFFFFFFFFFh

Legend:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Notes:
1. Not used by configuration logic.
2. 11111111b for XCS40XL only.
3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the $\overline{\text{INIT}}$ pin. In Master serial mode, CCLK continues to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling V_{CC}.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

Table 17: **Spartan/XL Program Data**

Device	XCS05		XCS10		XCS20		XCS30		XCS40	
Max System Gates	5,000		10,000		20,000		30,000		40,000	
CLBs (Row x Col.)	100 (10 x 10)		196 (14 x 14)		400 (20 x 20)		576 (24 x 24)		784 (28 x 28)	
IOBs	80		112		160		192		205(4)	
Part Number	XCS05	XCS05XL	XCS10	XCS10XL	XCS20	XCS20XL	XCS30	XCS30XL	XCS40	XCS40XL
Supply Voltage	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V
Bits per Frame	126	127	166	167	226	227	266	267	306	307
Frames	428	429	572	573	788	789	932	933	1,076	1,077
Program Data	53,936	54,491	94,960	95,699	178,096	179,111	247,920	249,119	329,264	330,647
PROM Size (bits)	53,984	54,544	95,008	95,752	178,144	179,160	247,968	249,168	329,312	330,696
Express Mode PROM Size (bits)	-	79,072	-	128,488	-	221,056	-	298,696	-	387,856

Notes:

1. Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits (+1 for Spartan-XL device)
   Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1 (+ 1 for Spartan-XL device)
   Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
   PROM Size = Program Data + 40 (header) + 8, rounded up to the nearest byte
2. The user can add more "1" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.
3. Express mode adds 57 (XCS05XL, XCS10XL), or 53 (XCS20XL, XCS30XL, XCS40XL) bits per frame, + additional start-up bits.
4. XCS40XL provided 224 max I/O in CS280 package discontinued by PDN2004-01.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 29. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Readback Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

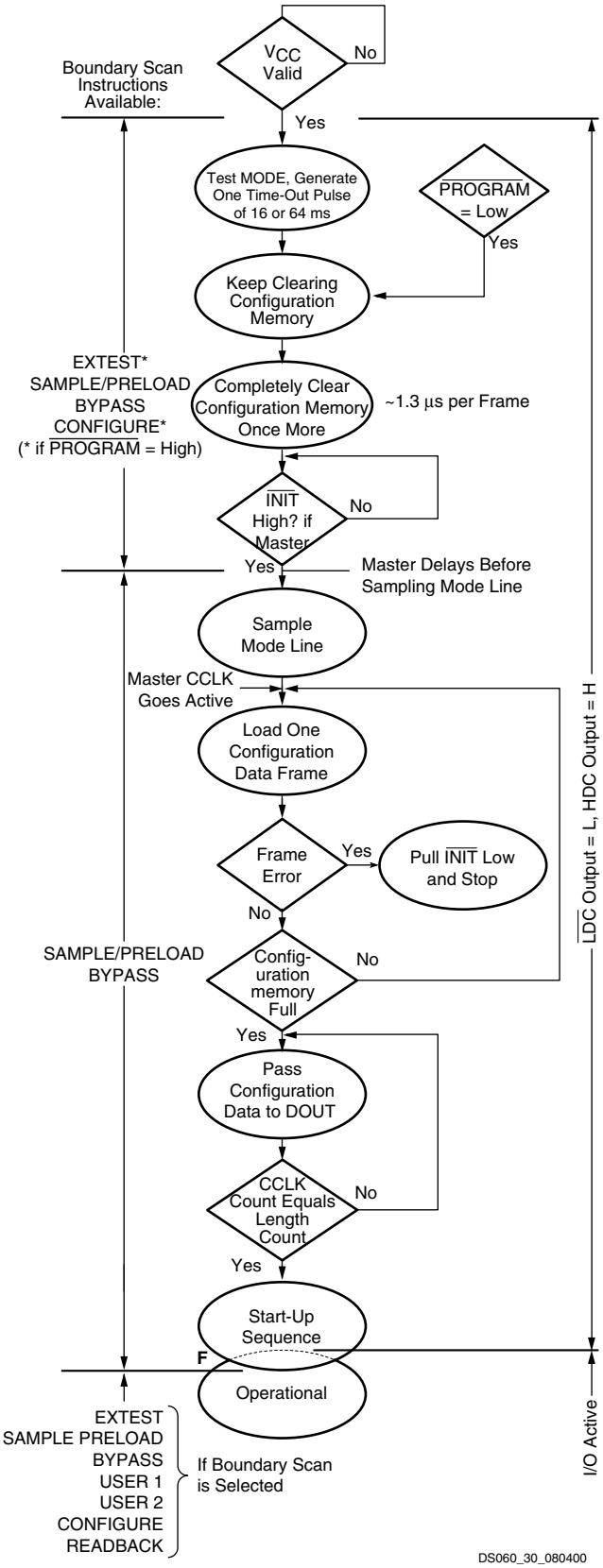


Figure 30: **Power-up Configuration Sequence**

Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count for serial modes. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Spartan-XL family Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{\text{INIT}}$ pin Low. After all configuration frames have been loaded into an FPGA using a serial mode, DOUT again follows the input data so that the remaining data is passed on to the next device. In Spartan-XL family Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See Figure 30.)

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the FPGA keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the $\overline{\text{INIT}}$ input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output. The Spartan/XL FPGA $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up.

Avoid holding $\overline{\text{PROGRAM}}$ Low for more than 500 µs. The 500 µs maximum limit is only a recommendation, not a requirement. The only effect of holding $\overline{\text{PROGRAM}}$ Low for more than 500 µs is an increase in current, measured at about 40 mA in the XCS40XL. This increased current cannot damage the device. This applies only during reconfiguration, not during power-up. The $\overline{\text{INIT}}$ pin can also be held Low to delay reconfiguration, and the same characteristics apply as for the $\overline{\text{PROGRAM}}$ pin.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration causes the FPGA

Spartan Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-4		-3		
		Min	Max	Min	Max	
Clocks						
T_{CH}	Clock High time	3.0	-	4.0	-	ns
T_{CL}	Clock Low time	3.0	-	4.0	-	ns
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	1.2	-	1.6	ns
T_{IHO}	F/G inputs via H to X/Y outputs	-	2.0	-	2.7	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.7	-	2.2	ns
CLB Fast Carry Logic						
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	1.7	-	2.1	ns
T_{ASCY}	Add/Subtract input (F3) to C_{OUT}	-	2.8	-	3.7	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	1.2	-	1.4	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	2.0	-	2.6	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.5	-	0.6	ns
Sequential Delays						
T_{CKO}	Clock K to Flip-Flop outputs Q	-	2.1	-	2.8	ns
Setup Time before Clock K						
T_{ICK}	F/G inputs	1.8	-	2.4	-	ns
T_{IHCK}	F/G inputs via H	2.9	-	3.9	-	ns
T_{HH1CK}	C inputs via H1 through H	2.3	-	3.3	-	ns
T_{DICK}	C inputs via DIN	1.3	-	2.0	-	ns
T_{ECCK}	C inputs via EC	2.0	-	2.6	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	2.5	-	4.0	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	3.0	-	4.0	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	3.0	-	4.0	ns
Global Set/Reset						
T_{MRW}	Minimum GSR pulse width	11.5	-	13.5	-	ns
T_{MRQ}	Delay from GSR input to any Q	See page 50 for T_{RRI} values per device.				
F_{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	166	-	125	MHz

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

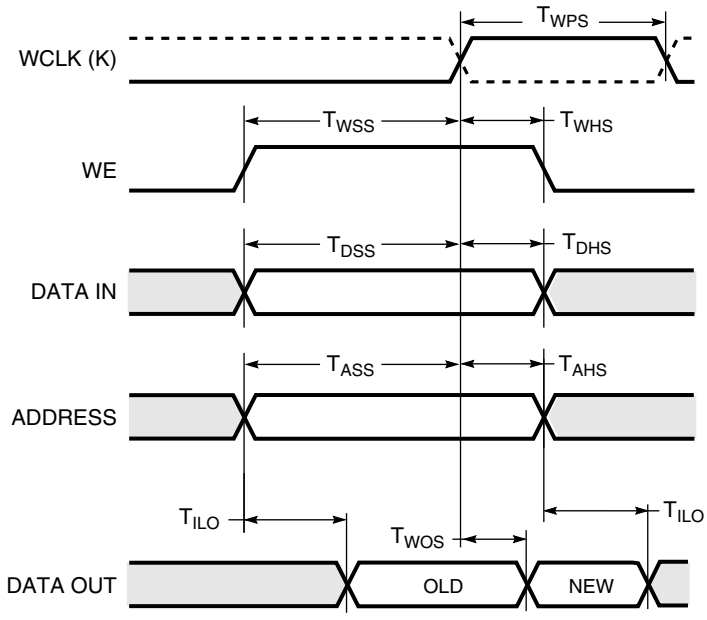
Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Dual Port RAM	Size[1]	-4		-3		Units
			Min	Max	Min	Max	
Write Operation							
T_{WCDS}	Address write cycle time (clock K period)	16x1	8.0	-	11.6	-	ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	4.0	-	5.8	-	ns
T_{ASDS}	Address setup time before clock K	16x1	1.5	-	2.1	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	0	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	1.5	-	1.6	-	ns
T_{DHDS}	DIN hold time after clock K	16x1	0	-	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.5	-	1.6	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	6.5	-	7.0	ns

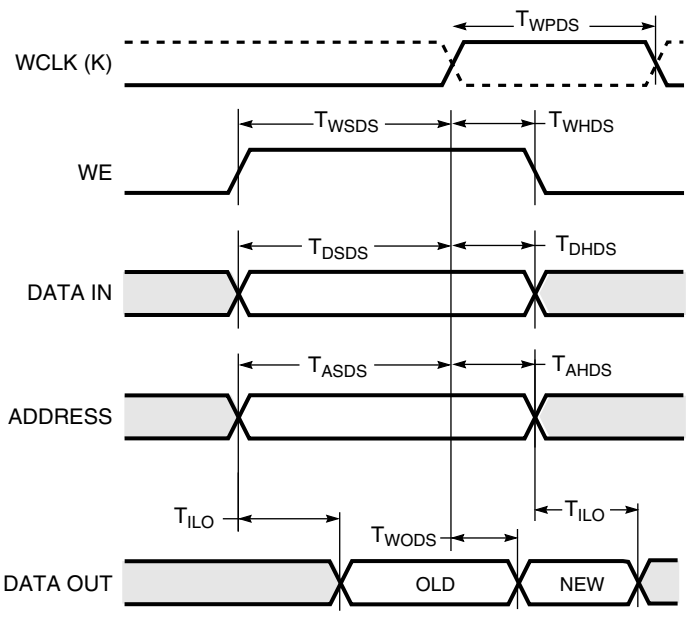
Notes:
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



DS060_34_011300

Spartan Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Spartan Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
Global Primary Clock to TTL Output using OFF					
T_{ICKOF}	Fast	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
T_{ICKO}	Slew-rate limited	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
T_{ICKSOF}	Fast	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
T_{ICKSO}	Slew-rate limited	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
T_{CMOSOF}	Fast	All devices	0.8	1.0	ns
T_{CMOSO}	Slew-rate limited	All devices	1.5	2.0	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column,and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 34.
3. OFF = Output Flip-Flop

Spartan-XL Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clocks						
T_{CH}	Clock High time	2.0	-	2.3	-	ns
T_{CL}	Clock Low time	2.0	-	2.3	-	ns
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	1.0	-	1.1	ns
T_{IHO}	F/G inputs via H to X/Y outputs	-	1.7	-	2.0	ns
T_{ITO}	F/G inputs via transparent latch to Q outputs	-	1.5	-	1.8	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.5	-	1.8	ns
Sequential Delays						
T_{CKO}	Clock K to Flip-Flop or latch outputs Q	-	1.2	-	1.4	ns
Setup Time before Clock K						
T_{ICK}	F/G inputs	0.6	-	0.7	-	ns
T_{IHCK}	F/G inputs via H	1.3	-	1.6	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	2.5	-	2.8	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	2.3	-	2.7	ns
Global Set/Reset						
T_{MRW}	Minimum GSR Pulse Width	10.5	-	11.5	-	ns
T_{MRQ}	Delay from GSR input to any Q	See page 60 for T_{RRI} values per device.				
F_{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	250	-	217	MHz

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

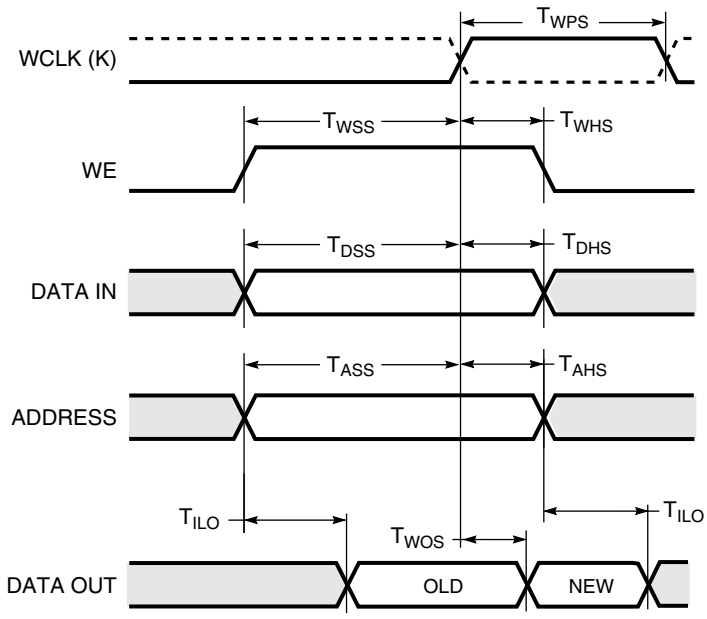
All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation(1)							
T_{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T_{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

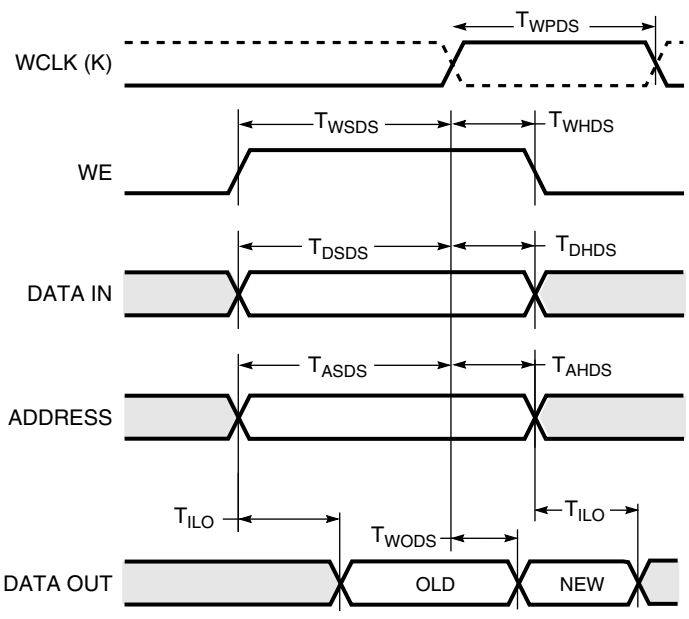
Notes:
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



DS060_34_011300

Spartan-XL Family IOB Input Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Setup Times							
T_{ECIK}	Clock Enable (EC) to Clock (IK)	All devices	0.0	-	0.0	-	ns
T_{PICK}	Pad to Clock (IK), no delay	All devices	1.0	-	1.2	-	ns
T_{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	All devices	0.7	-	0.8	-	ns
Hold Times							
	All Hold Times	All devices	0.0	-	0.0	-	ns
Propagation Delays							
T_{PID}	Pad to I1, I2	All devices	-	0.9	-	1.1	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	2.1	-	2.5	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.0	-	1.1	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.1	-	1.2	ns
Delay Adder for Input with Full Delay Option							
T_{Delay}	$T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	XCS05XL	4.0	-	4.7	-	ns
		XCS10XL	4.8	-	5.6	-	ns
		XCS20XL	5.0	-	5.9	-	ns
		XCS30XL	5.5	-	6.5	-	ns
		XCS40XL	6.5	-	7.6	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T_{RRI}	Delay from GSR input to any Q	XCS05XL	-	9.0	-	10.5	ns
		XCS10XL	-	9.5	-	11.0	ns
		XCS20XL	-	10.0	-	11.5	ns
		XCS30XL	-	11.0	-	12.5	ns
		XCS40XL	-	12.0	-	13.5	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Table 18: **Pin Descriptions *(Continued)***

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Spartan-XL family Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
VCC	P33	P25	N1	P37	-
Not Connect-ed[1] PWRDWN[2]	P34	P26	N2	P38	174 [1]
I/O, PGCK2[1] GCK3[2]	P35	P27	M3	P39	175[3]
I/O (HDC)	P36	P28	N3	P40	178 [3]
I/O	-	-	K4	P41	181 [3]
I/O	-	-	L4	P42	184 [3]
I/O	-	P29	M4	P43	187 [3]
I/O ($\overline{LDC}$)	P37	P30	N4	P44	190 [3]
GND	-	-	K5	P45	-
I/O	-	-	L5	P46	193 [3]
I/O	-	-	M5	P47	196 [3]
I/O	P38	P31	N5	P48	199 [3]
I/O	P39	P32	K6	P49	202 [3]
I/O	-	P33	L6	P50	205 [3]
I/O	-	P34	M6	P51	208 [3]
I/O	P40	P35	N6	P52	211 [3]
I/O ($\overline{INIT}$)	P41	P36	M7	P53	214 [3]
VCC	P42	P37	N7	P54	-
GND	P43	P38	L7	P55	-
I/O	P44	P39	K7	P56	217 [3]
I/O	P45	P40	N8	P57	220 [3]
I/O	-	P41	M8	P58	223 [3]
I/O	-	P42	L8	P59	226 [3]
I/O	P46	P43	K8	P60	229 [3]
I/O	P47	P44	N9	P61	232 [3]
I/O	-	-	M9	P62	235 [3]
I/O	-	-	L9	P63	238 [3]
GND	-	-	K9	P64	-
I/O	P48	P45	N10	P65	241 [3]
I/O	P49	P46	M10	P66	244 [3]
I/O	-	-	L10	P67	247 [3]
I/O	-	-	N11	P68	250 [3]
I/O	P50	P47	M11	P69	253 [3]
I/O, SGCK3[1] GCK4[2]	P51	P48	L11	P70	256 [3]
GND	P52	P49	N12	P71	-
DONE	P53	P50	M12	P72	-
VCC	P54	P51	N13	P73	-
$\overline{PROGRAM}$	P55	P52	M13	P74	-
I/O (D7[2])	P56	P53	L12	P75	259 [3]

XCS10 and XCS10XL Device Pinouts

XCS10/XL Pad Name	PC84[4]	VQ100	CS144[2,4]	TQ144	Bndry Scan
I/O, PGCK3[1] GCK5[2]	P57	P54	L13	P76	262 [3]
I/O	-	-	K10	P77	265 [3]
I/O	-	-	K11	P78	268 [3]
I/O (D6[2])	P58	P55	K12	P79	271 [3]
I/O	-	P56	K13	P80	274 [3]
GND	-	-	J10	P81	-
I/O	-	-	J11	P82	277 [3]
I/O	-	-	J12	P83	280 [3]
I/O (D5[2])	P59	P57	J13	P84	283 [3]
I/O	P60	P58	H10	P85	286 [3]
I/O	-	P59	H11	P86	289 [3]
I/O	-	P60	H12	P87	292 [3]
I/O (D4[2])	P61	P61	H13	P88	295 [3]
I/O	P62	P62	G12	P89	298 [3]
VCC	P63	P63	G13	P90	-
GND	P64	P64	G11	P91	-
I/O (D3[2])	P65	P65	G10	P92	301 [3]
I/O	P66	P66	F13	P93	304 [3]
I/O	-	P67	F12	P94	307 [3]
I/O	-	-	F11	P95	310 [3]
I/O (D2[2])	P67	P68	F10	P96	313 [3]
I/O	P68	P69	E13	P97	316 [3]
I/O	-	-	E12	P98	319 [3]
I/O	-	-	E11	P99	322 [3]
GND	-	-	E10	P100	-
I/O (D1[2])	P69	P70	D13	P101	325 [3]
I/O	P70	P71	D12	P102	328 [3]
I/O	-	-	D11	P103	331 [3]
I/O	-	-	C13	P104	334 [3]
I/O (D0[2], DIN)	P71	P72	C12	P105	337 [3]
I/O, SGCK4[1] GCK6[2] (DOUT)	P72	P73	C11	P106	340 [3]
CCLK	P73	P74	B13	P107	-
VCC	P74	P75	B12	P108	-
O, TDO	P75	P76	A13	P109	0
GND	P76	P77	A12	P110	-
I/O	P77	P78	B11	P111	2
I/O, PGCK4[1] GCK7[2]	P78	P79	A11	P112	5
I/O	-	-	D10	P113	8
I/O	-	-	C10	P114	11
I/O (CS1[2])	P79	P80	B10	P115	14

Additional XCS20/XL Package Pins

PQ208					
Not Connected Pins					
P12	P18 (1)	P33 (1)	P39	P65	P71 (1)
P86 (1)	P92	P111	P121(1)	P140(1)	P144
P165	P173(1)	P192(1)	P202	P203	-
9/16/98					

Notes:
1. 5V Spartan family only
2. 3V Spartan-XL family only
3. The “PWRDWN” on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).
4. CS144 package discontinued by PDN2004-01

XCS30 and XCS30XL Device Pinouts

XCS30/XL Pad Name	VQ100(5)	TQ144	PQ208	PQ240	BG256(5)	CS280(2,5)	Bndry Scan
VCC	P89	P128	P183	P212	VCC(4)	C10	-
I/O	P90	P129	P184	P213	C10	D10	74
I/O	P91	P130	P185	P214	D10	E10	77
I/O	P92	P131	P186	P215	A9	A9	80
I/O	P93	P132	P187	P216	B9	B9	83
I/O	-	-	P188	P217	C9	C9	86
I/O	-	-	P189	P218	D9	D9	89
I/O	P94	P133	P190	P220	A8	A8	92
I/O	P95	P134	P191	P221	B8	B8	95
VCC	-	-	P192	P222	VCC(4)	A7	-
I/O	-	-	-	P223	A6	B7	98
I/O	-	-	-	P224	C7	C7	101
I/O	-	P135	P193	P225	B6	D7	104
I/O	-	P136	P194	P226	A5	A6	107
GND	-	P137	P195	P227	GND(4)	GND(4)	-
I/O	-	-	P196	P228	C6	B6	110
I/O	-	-	P197	P229	B5	C6	113
I/O	-	-	P198	P230	A4	D6	116
I/O	-	-	P199	P231	C5	E6	119
I/O	P96	P138	P200	P232	B4	A5	122
I/O	P97	P139	P201	P233	A3	C5	125
I/O	-	-	P202	P234	D5	B4	128
I/O	-	-	P203	P235	C4	C4	131
I/O	-	P140	P204	P236	B3	A3	134
I/O	-	P141	P205	P237	B2	A2	137
I/O	P98	P142	P206	P238	A2	B3	140
I/O, SGCK1(1), GCK8(2)	P99	P143	P207	P239	C3	B2	143
VCC	P100	P144	P208	P240	VCC(4)	A1	-
GND	P1	P1	P1	P1	GND(4)	GND(4)	-
I/O, PGCK1(1), GCK1(2)	P2	P2	P2	P2	B1	C3	146
I/O	P3	P3	P3	P3	C2	C2	149
I/O	-	P4	P4	P4	D2	B1	152

XCS30 and XCS30XL Device Pinouts *(Continued)*

XCS30/XL Pad Name	VQ100[5]	TQ144	PQ208	PQ240	BG256[5]	CS280[2,5]	Bndry Scan
I/O	-	-	P124	P144	M20	L19	493 [3]
I/O	-	-	P125	P145	L19	L18	496 [3]
I/O	P59	P86	P126	P146	L18	L17	499 [3]
I/O	P60	P87	P127	P147	L20	L16	502 [3]
I/O (D4[2])	P61	P88	P128	P148	K20	K19	505 [3]
I/O	P62	P89	P129	P149	K19	K18	508 [3]
VCC	P63	P90	P130	P150	VCC[4]	K17	-
GND	P64	P91	P131	P151	GND[4]	GND[4]	-
I/O (D3[2])	P65	P92	P132	P152	K18	K16	511 [3]
I/O	P66	P93	P133	P153	K17	K15	514 [3]
I/O	P67	P94	P134	P154	J20	J19	517 [3]
I/O	-	P95	P135	P155	J19	J18	520 [3]
I/O	-	-	P136	P156	J18	J17	523 [3]
I/O	-	-	P137	P157	J17	J16	526 [3]
I/O (D2[2])	P68	P96	P138	P159	H19	H17	529 [3]
I/O	P69	P97	P139	P160	H18	H16	532 [3]
VCC	-	-	P140	P161	VCC[4]	G19	-
I/O	-	P98	P141	P162	G19	G18	535 [3]
I/O	-	P99	P142	P163	F20	G17	538 [3]
I/O	-	-	-	P164	G18	G16	541 [3]
I/O	-	-	-	P165	F19	F19	544 [3]
GND	-	P100	P143	P166	GND[4]	GND[4]	-
I/O	-	-	-	P167	F18	F18	547 [3]
I/O	-	-	P144	P168	E19	F17	550 [3]
I/O	-	-	P145	P169	D20	F16	553 [3]
I/O	-	-	P146	P170	E18	F15	556 [3]
I/O	-	-	P147	P171	D19	E19	559 [3]
I/O	-	-	P148	P172	C20	E17	562 [3]
I/O (D1[2])	P70	P101	P149	P173	E17	E16	565 [3]
I/O	P71	P102	P150	P174	D18	D19	568 [3]
I/O	-	P103	P151	P175	C19	C19	571 [3]
I/O	-	P104	P152	P176	B20	B19	574 [3]
I/O (D0[2], DIN)	P72	P105	P153	P177	C18	C18	577 [3]
I/O, SGCK4[1], GCK6[2] (DOUT)	P73	P106	P154	P178	B19	B18	580 [3]
CCLK	P74	P107	P155	P179	A20	A19	-
VCC	P75	P108	P156	P180	VCC[4]	C17	-
O, TDO	P76	P109	P157	P181	A19	B17	0
GND	P77	P110	P158	P182	GND[4]	GND[4]	-
I/O	P78	P111	P159	P183	B18	A18	2
I/O, PGCK4[1], GCK7[2]	P79	P112	P160	P184	B17	A17	5
I/O	-	P113	P161	P185	C17	D16	8
I/O	-	P114	P162	P186	D16	C16	11
I/O (CS1)[2]	P80	P115	P163	P187	A18	B16	14
I/O	P81	P116	P164	P188	A17	A16	17
I/O	-	-	P165	P189	C16	D15	20

Revision History

The following table shows the revision history for this document.

Date	Version	Description
11/20/98	1.3	Added Spartan-XL specs and Power Down.
01/06/99	1.4	All Spartan-XL -4 specs designated Preliminary with no changes.
03/02/00	1.5	Added CS package, updated Spartan-XL specs to Final.
09/19/01	1.6	Reformatted, updated power specs, clarified configuration information. Removed T_{SOL} soldering information from Absolute Maximum Ratings table. Changed Figure 26: Slave Serial Mode Characteristics: T_{CCH}, T_{CCL} from 45 to 40 ns. Changed Master Mode Configuration Switching Characteristics: T_{CCLK} min. from 80 to 100 ns. Added Total Dist. RAM Bits to Table 1; added **Start-Up**, page 36 characteristics.
06/27/02	1.7	Clarified Express Mode pseudo daisy chain. Added new Industrial options. Clarified XCS30XL CS280 V_{CC} pinout.
06/26/08	1.8	Noted that PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, are discontinued by **PDN2004-01**. Extended description of recommended maximum delay of reconfiguration in **Delaying Configuration After Power-Up**, page 35. Added reference to Pb-free package options and provided link to **Package Specifications**, page 81. Updated links.
03/01/13	2.0	The products listed in this data sheet are obsolete. See **XCN10016** and **XCN11010** for further information.