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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	224
Number of Gates	40000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	280-TFBGA, CSPBGA
Supplier Device Package	280-CSBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40xl-5cs280c

Table 4: Supported Sources for Spartan/XL Inputs

Source	Spartan Inputs		Spartan-XL Inputs
	5V, TTL	5V, CMOS	3.3V CMOS
Any device, $V_{CC} = 3.3V$, CMOS outputs	✓	Unreliable Data	✓
Spartan family, $V_{CC} = 5V$, TTL outputs	✓		✓
Any device, $V_{CC} = 5V$, TTL outputs ($V_{OH} \leq 3.7V$)	✓		✓
Any device, $V_{CC} = 5V$, CMOS outputs	✓	✓	✓ (default mode)

Table 5: I/O Standards Supported by Spartan-XL FPGAs

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}
LVC MOS 3V	OK	12/24 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}

Additional Fast Capture Input Latch (Spartan-XL Family Only)

The Spartan-XL family OB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active High input flip-flop. ILFLX is a transparent Low Fast Capture latch followed by a transparent High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 6.


Spartan-XL Family V_{CC} Clamping

Spartan-XL FPGAs have an optional clamping diode connected from each I/O to V_{CC} . When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. V_{CC} clamping is a global option affecting all I/O pins.


Spartan-XL devices are fully 5V TTL I/O compatible if V_{CC} clamping is not enabled. With V_{CC} clamping enabled, the Spartan-XL devices will begin to clamp input voltages to one diode voltage drop above V_{CC} . If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

Spartan-XL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 5.

Table 6: Output Flip-Flop Functionality

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
		1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
	Rising edge (clock not inverted).
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

Output Multiplexer/2-Input Function Generator (Spartan-XL Family Only)

The output path in the Spartan-XL family IOB contains an additional multiplexer not available in the Spartan family IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass gate, AND gate, OR gate, or XOR gate, with 0, 1, or 2 inverted inputs.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. The select input is the pin used for the output flip-flop clock, OK.

When the multiplexer is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe driven by a global buffer.

The user can specify that the IOB function generator be used by placing special library symbols beginning with the letter "O." For example, a 2-input AND gate in the IOB function generator is called OAND2. Use the symbol input pin labeled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in Figure 7.



Figure 7: AND and MUX Symbols in Spartan-XL IOB

Output Buffer

An active High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (O) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB (see Figure 6, page 7). An output can be configured as open-drain (open-collector) by tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground.

By default, a 5V Spartan device output buffer pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below V_{CC} . Alternatively, the outputs can be globally configured as CMOS drivers, with additional p-channel pull-up transistors pulling to V_{CC} . This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable.

All Spartan-XL device outputs are configured as CMOS drivers, therefore driving rail-to-rail. The Spartan-XL family outputs are individually programmable for 12 mA or 24 mA output drive.

Any 5V Spartan device with its outputs configured in TTL mode can drive the inputs of any typical 3.3V device. Supported destinations for Spartan/XL device outputs are shown in Table 7.

Three-State Register (Spartan-XL Family Only)

Spartan-XL devices incorporate an optional register controlling the three-state enable in the IOBs. The use of the three-state control register can significantly improve output enable and disable time.

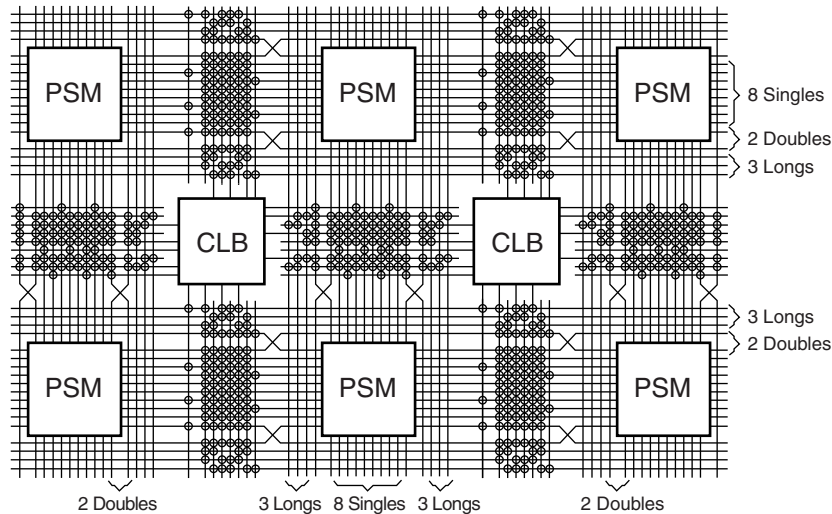
Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

Spartan/XL devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Pull-up and Pull-down Network

Programmable pull-up and pull-down resistors are used for tying unused pins to V_{CC} or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to V_{CC} . The configurable pull-down resistor is an n-channel transistor that pulls to Ground. The value of these resistors is typically 20 K Ω – 100 K Ω (See "Spartan Family DC Characteristics Over Operating Conditions" on page 43.).

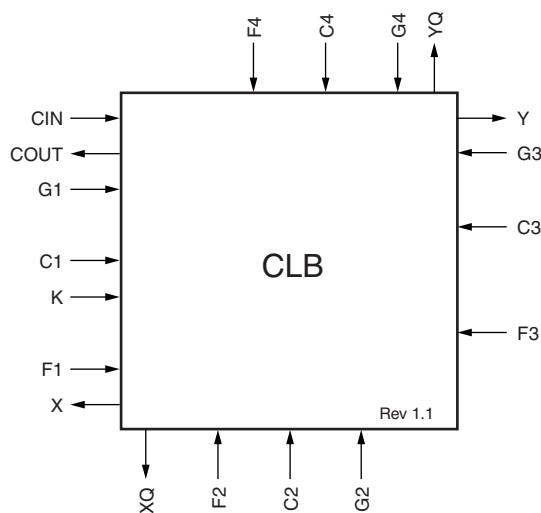


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Figure 8: Spartan/XL CLB Routing Channels and Interface Block Diagram

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.



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Figure 9: CLB Interconnect Signals

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs. Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

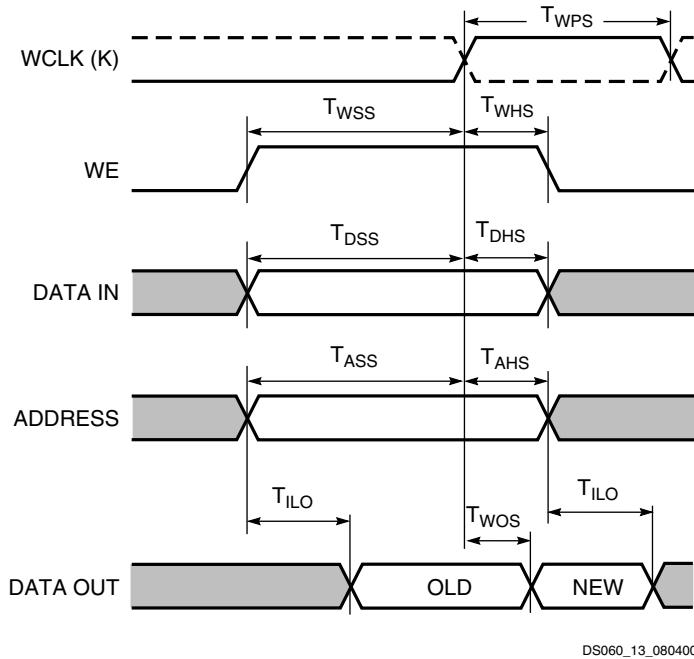


Figure 13: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be

inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO} , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS} , the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by $A[3:0]$ while the second provides only for read operations at the address specified independently by $DPRA[3:0]$. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the

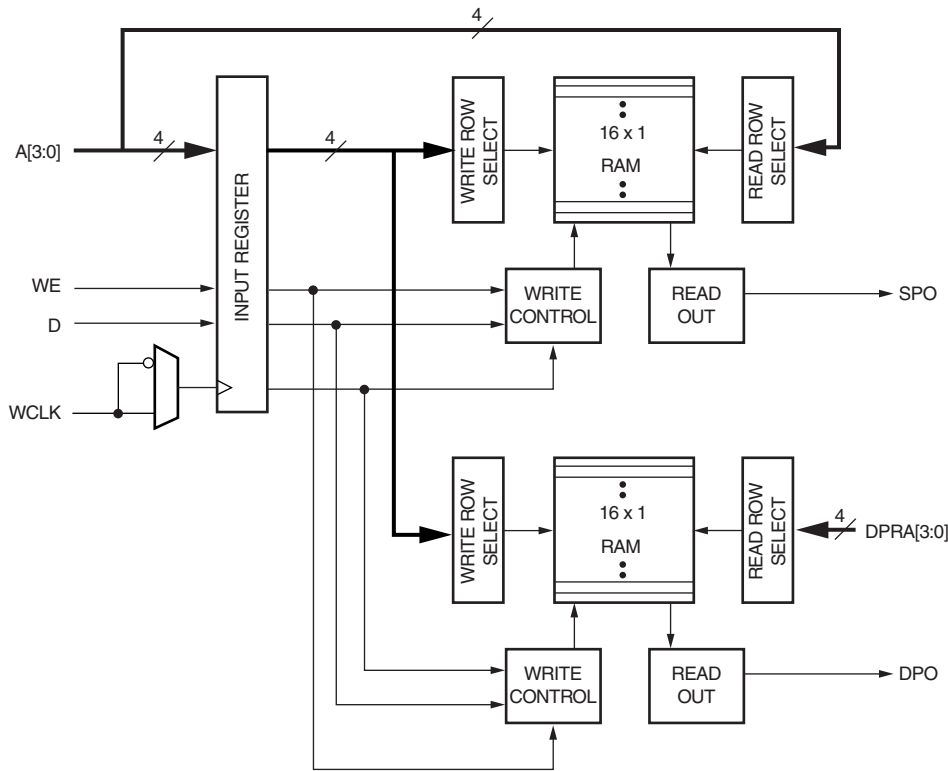


Figure 14: Logic Diagram for the Dual-Port RAM

Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to $+25\%$.

In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

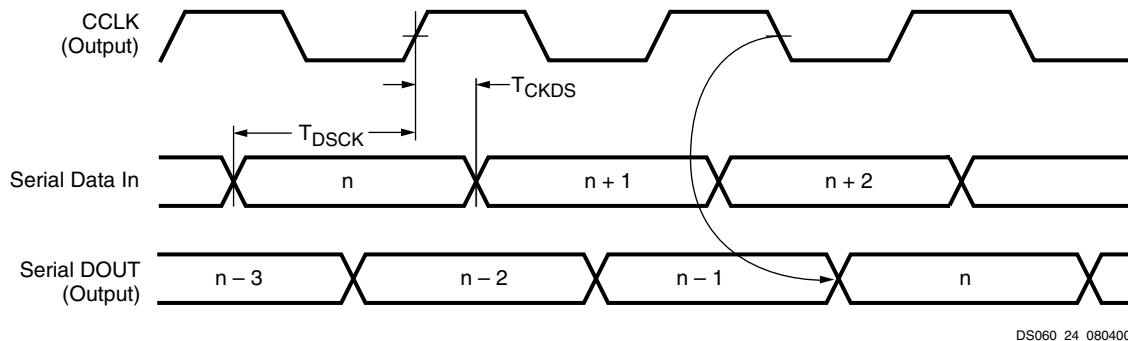
When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the

falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in [Figure 24](#).

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Earlier families such as the XC3000 series do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

[Figure 25](#) shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Symbol	Description	Min	Units
CCLK	T_{DSCK}	DIN setup	20	ns
	T_{CKDS}	DIN hold	0	ns

Notes:

1. At power-up, V_{CC} must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 24: Master Serial Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

[Figure 25](#) shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

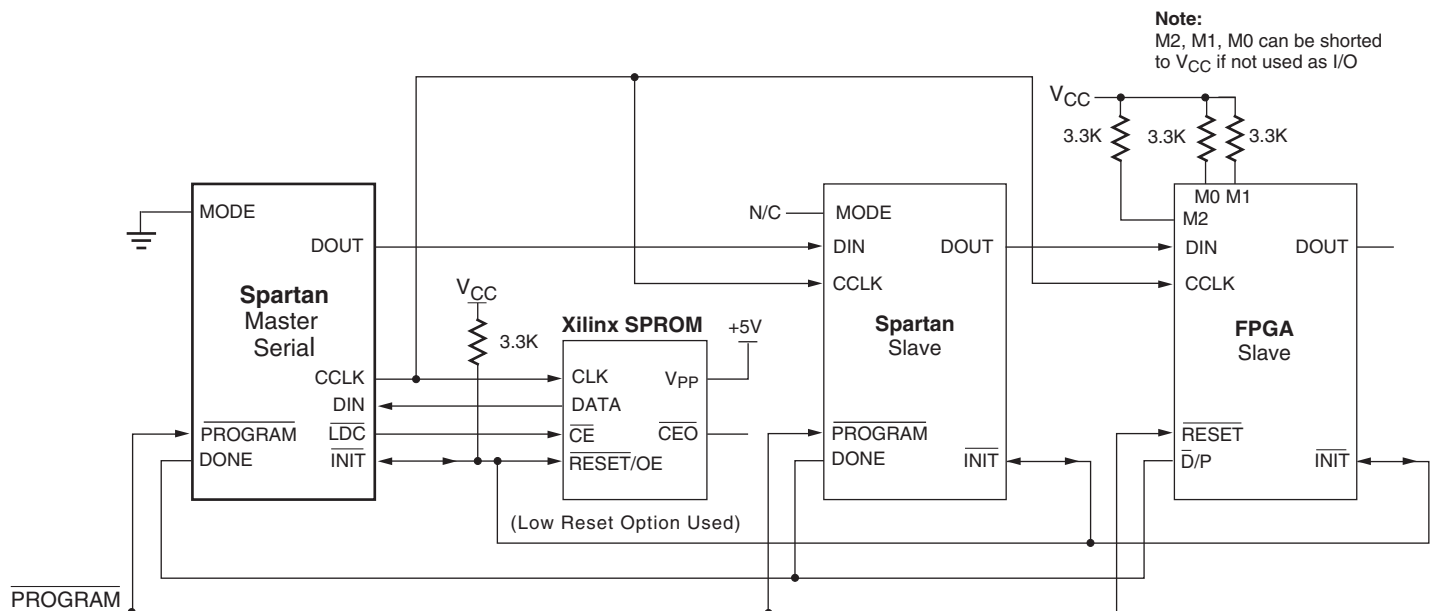
Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through

and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.

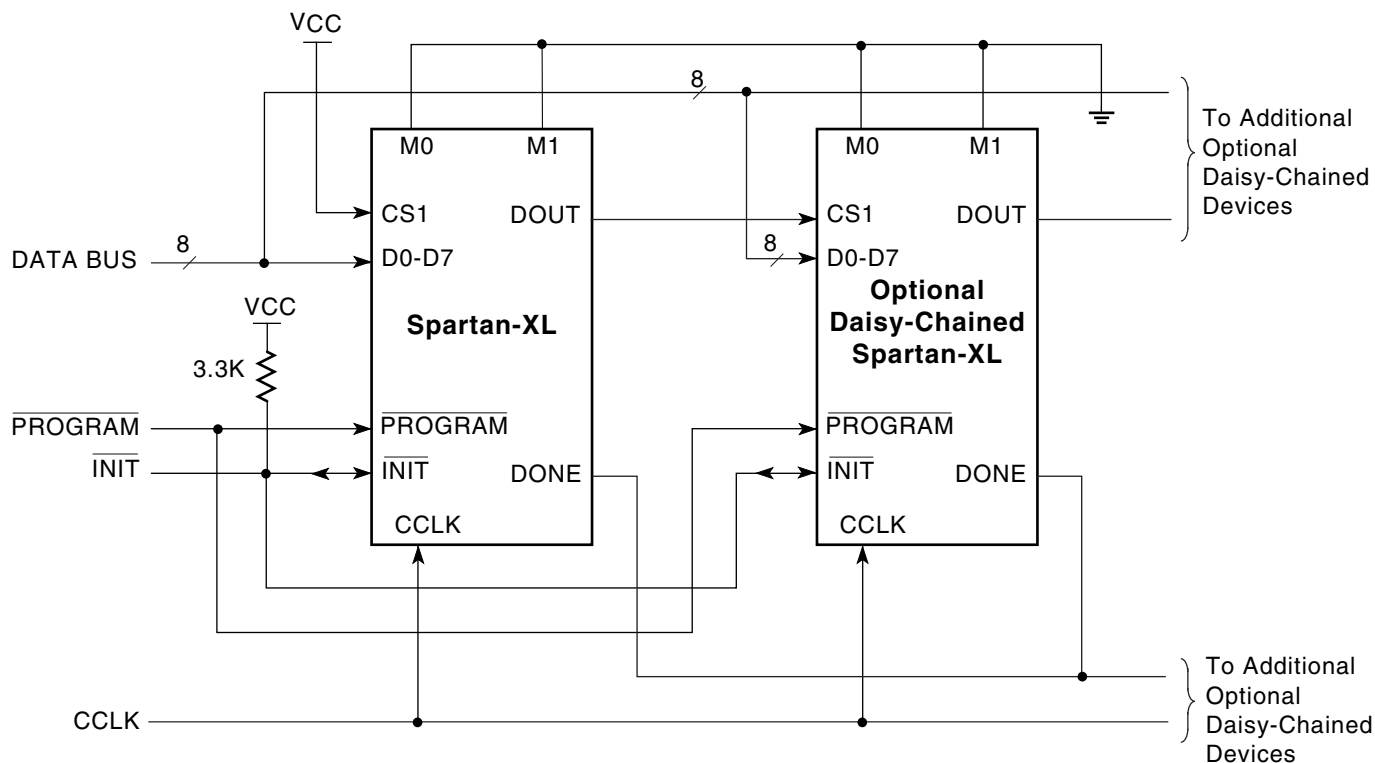


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Figure 25: Master/Slave Serial Mode Circuit Diagram

to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device

in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Only devices supporting Express mode can be used to form an Express mode daisy chain.



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Figure 27: Express Mode Circuit Diagram

Table 17: Spartan/XL Program Data

Device	XCS05		XCS10		XCS20		XCS30		XCS40	
Max System Gates	5,000		10,000		20,000		30,000		40,000	
CLBs (Row x Col.)	100 (10 x 10)		196 (14 x 14)		400 (20 x 20)		576 (24 x 24)		784 (28 x 28)	
I/Os	80		112		160		192		205 ⁽⁴⁾	
Part Number	XCS05	XCS05XL	XCS10	XCS10XL	XCS20	XCS20XL	XCS30	XCS30XL	XCS40	XCS40XL
Supply Voltage	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V
Bits per Frame	126	127	166	167	226	227	266	267	306	307
Frames	428	429	572	573	788	789	932	933	1,076	1,077
Program Data	53,936	54,491	94,960	95,699	178,096	179,111	247,920	249,119	329,264	330,647
PROM Size (bits)	53,984	54,544	95,008	95,752	178,144	179,160	247,968	249,168	329,312	330,696
Express Mode PROM Size (bits)	-	79,072	-	128,488	-	221,056	-	298,696	-	387,856

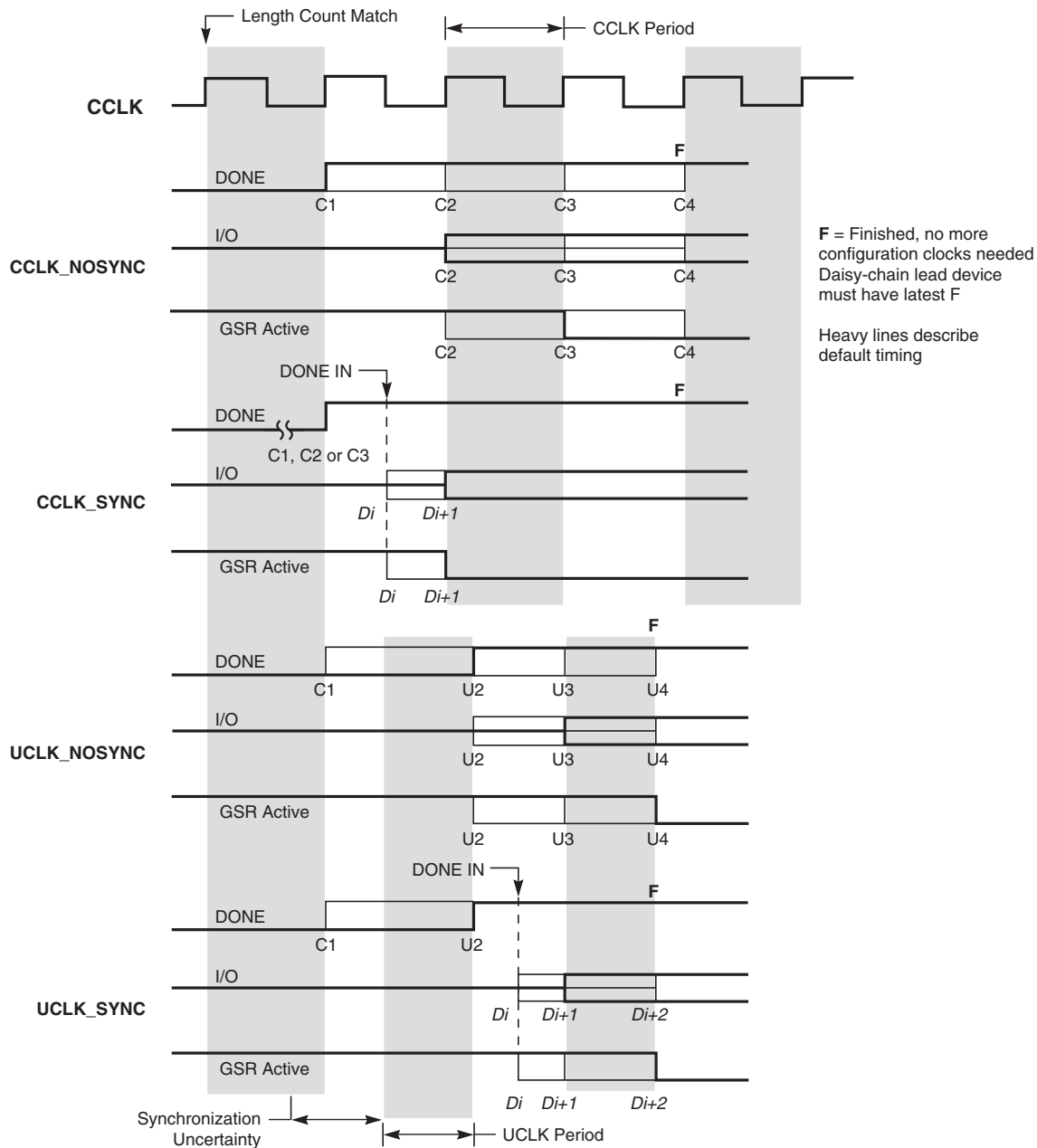
Notes:

- Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits (+1 for Spartan-XL device)
 Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1 (+ 1 for Spartan-XL device)
 Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
 PROM Size = Program Data + 40 (header) + 8, rounded up to the nearest byte
- The user can add more "1" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.
- Express mode adds 57 (XCS05XL, XCS10XL), or 53 (XCS20XL, XCS30XL, XCS40XL) bits per frame, + additional start-up bits.
- XCS40XL provided 224 max I/O in CS280 package discontinued by [PDN2004-01](#).

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in [Figure 29](#). The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback

data is independent of the current device state. CLB outputs should not be included (Readback Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.



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Figure 31: Start-up Timing

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the PROGRAM pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input.

- Wait for $\overline{\text{INIT}}$ to go High.
- Sequence the boundary scan Test Access Port to the SHIFT-DR state.
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after $\overline{\text{INIT}}$ goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "Boundary Scan in FPGA Devices." This application note applies to Spartan and Spartan-XL devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Although readback can be performed while the device is operating, for best results and to freeze a known capture state, it is recommended that the clock inputs be stopped until readback is complete.

Readback of Spartan-XL family Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL FPGA Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in [Figure 32](#).

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low)

of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

Readback Capture

When the Readback Capture option is selected, the data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.

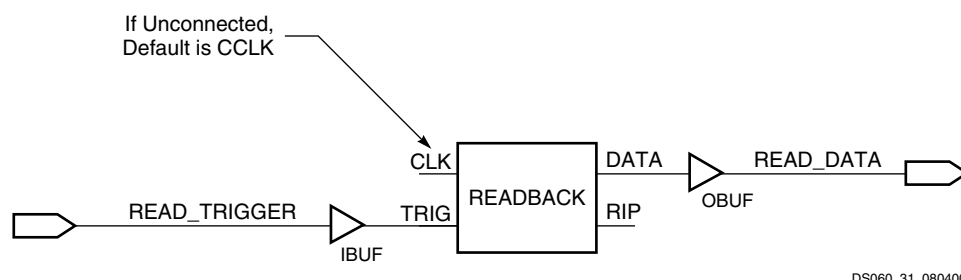


Figure 32: Readback Example

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be

met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in [Table 16](#) and [Table 17](#).

Spartan Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan Family Absolute Maximum Ratings⁽¹⁾

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		−0.5 to +7.0	V
V_{IN}	Input voltage relative to GND ^(2,3)		−0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output ^(2,3)		−0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		−65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- Maximum DC overshoot (above V_{CC}) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to −2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Spartan Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	4.75	5.25	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ ⁽¹⁾	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage ⁽²⁾	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage ⁽²⁾	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:

- At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings⁽¹⁾

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		−0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked ^(2, 3)	−0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	−0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked ^(2, 3)	−0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	−0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)		−65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to −2.0V or overshoot to +7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to −2.0V or overshoot to $V_{CC} + 2.0V$, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ ⁽¹⁾	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage ⁽²⁾		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage ⁽²⁾		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:

- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement threshold is ~50% of V_{CC} .

Spartan-XL Family CLB Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and expressed in nanoseconds unless otherwise noted.

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clocks						
T _{CH}	Clock High time	2.0	-	2.3	-	ns
T _{CL}	Clock Low time	2.0	-	2.3	-	ns
Combinatorial Delays						
T _{ILO}	F/G inputs to X/Y outputs	-	1.0	-	1.1	ns
T _{IHO}	F/G inputs via H to X/Y outputs	-	1.7	-	2.0	ns
T _{ITO}	F/G inputs via transparent latch to Q outputs	-	1.5	-	1.8	ns
T _{HH1O}	C inputs via H1 via H to X/Y outputs	-	1.5	-	1.8	ns
Sequential Delays						
T _{CKO}	Clock K to Flip-Flop or latch outputs Q	-	1.2	-	1.4	ns
Setup Time before Clock K						
T _{ICK}	F/G inputs	0.6	-	0.7	-	ns
T _{IHCK}	F/G inputs via H	1.3	-	1.6	-	ns
Hold Time after Clock K						
	All Hold times, all devices	0.0	-	0.0	-	ns
Set/Reset Direct						
T _{RPW}	Width (High)	2.5	-	2.8	-	ns
T _{RIO}	Delay from C inputs via S/R, going High to Q	-	2.3	-	2.7	ns
Global Set/Reset						
T _{MRW}	Minimum GSR Pulse Width	10.5	-	11.5	-	ns
T _{MRQ}	Delay from GSR input to any Q	See page 60 for T _{RR1} values per device.				
F _{TOG}	Toggle Frequency (MHz) (for export control purposes)	-	250	-	217	MHz

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE

in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

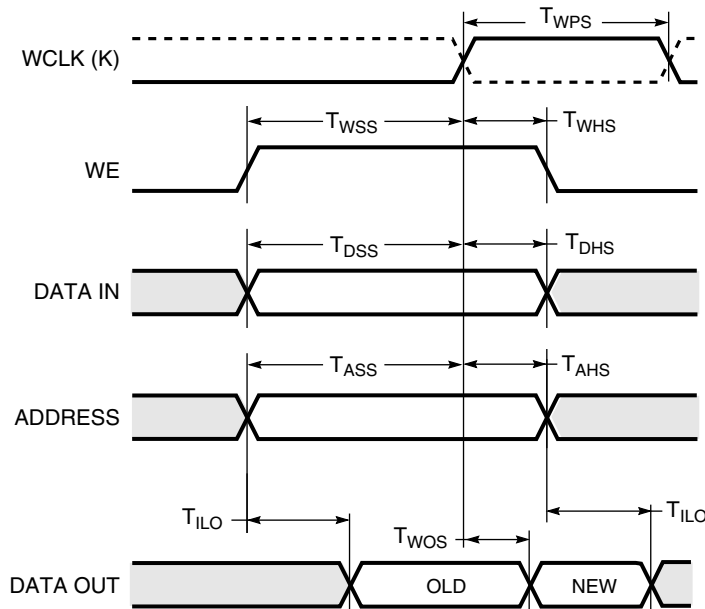
Symbol	Dual Port RAM	Size	-5		-4		Units
			Min	Max	Min	Max	
Write Operation ⁽¹⁾							
T _{WCDS}	Address write cycle time (clock K period)	16x1	7.7	-	8.4	-	ns
T _{WPDS}	Clock K pulse width (active edge)	16x1	3.1	-	3.6	-	ns
T _{ASDS}	Address setup time before clock K	16x1	1.3	-	1.5	-	ns
T _{DSDS}	DIN setup time before clock K	16x1	1.7	-	2.0	-	ns
T _{WSDS}	WE setup time before clock K	16x1	1.4	-	1.6	-	ns
	All hold times after clock K	16x1	0	-	0	-	ns
T _{WODS}	Data valid after clock K	16x1	-	5.2	-	6.1	ns

Notes:

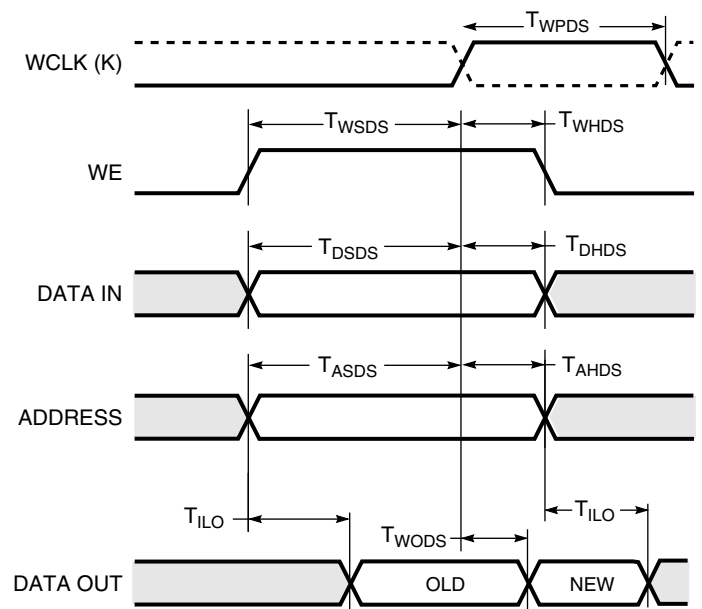
1. Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing

Spartan-XL Family CLB RAM Synchronous (Edge-Triggered) Write Timing

Single Port



Dual Port



DS060_34_011300

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
$\overline{\text{PWRDWN}}$	I	I	$\overline{\text{PWRDWN}}$ is an active Low input that forces the FPGA into the Power Down state and reduces power consumption. When $\overline{\text{PWRDWN}}$ is Low, the FPGA disables all I/O and initializes all flip-flops. All inputs are interpreted as Low independent of their actual level. VCC must be maintained, and the configuration data is maintained. $\overline{\text{PWRDWN}}$ halts configuration if asserted before or during configuration, and re-starts configuration when removed. When $\overline{\text{PWRDWN}}$ returns High, the FPGA becomes operational by first enabling the inputs and flip-flops and then enabling the outputs. $\overline{\text{PWRDWN}}$ has a default internal pull-up resistor.
User I/O Pins That Can Have Special Functions			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 k Ω to 10 k Ω external pull-up resistor is recommended. As an active Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 μs after INIT has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFPGP symbol is automatically placed on one of these pins.

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	P18	P28	P44	P52	V1	T1	272
I/O	P19	P29	P45	P53	T4	T2	275
I/O	-	P30	P46	P54	U3	T3	278
I/O	-	P31	P47	P55	V2	U1	281
I/O	P20	P32	P48	P56	W1	V1	284
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P21	P33	P49	P57	V3	U2	287
Not Connected ⁽¹⁾ , M1 ⁽²⁾	P22	P34	P50	P58	W2	V2	290
GND	P23	P35	P51	P59	GND ⁽⁴⁾	GND ⁽⁴⁾	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P24	P36	P52	P60	Y1	W1	293
VCC	P25	P37	P53	P61	VCC ⁽⁴⁾	U3	-
Not Connected ⁽¹⁾ , PWRDWN ⁽²⁾	P26	P38	P54	P62	W3	V3	294 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P27	P39	P55	P63	Y2	W2	295 ⁽³⁾
I/O (HDC)	P28	P40	P56	P64	W4	W3	298 ⁽³⁾
I/O	-	P41	P57	P65	V4	T4	301 ⁽³⁾
I/O	-	P42	P58	P66	U5	U4	304 ⁽³⁾
I/O	P29	P43	P59	P67	Y3	V4	307 ⁽³⁾
I/O (LDC)	P30	P44	P60	P68	Y4	W4	310 ⁽³⁾
I/O	-	-	P61	P69	V5	T5	313 ⁽³⁾
I/O	-	-	P62	P70	W5	W5	316 ⁽³⁾
I/O	-	-	P63	P71	Y5	R6	319 ⁽³⁾
I/O	-	-	P64	P72	V6	U6	322 ⁽³⁾
I/O	-	-	P65	P73	W6	V6	325 ⁽³⁾
I/O	-	-	-	P74	Y6	T6	328 ⁽³⁾
GND	-	P45	P66	P75	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P46	P67	P76	W7	W6	331 ⁽³⁾
I/O	-	P47	P68	P77	Y7	U7	334 ⁽³⁾
I/O	P31	P48	P69	P78	V8	V7	337 ⁽³⁾
I/O	P32	P49	P70	P79	W8	W7	340 ⁽³⁾
VCC	-	-	P71	P80	VCC ⁽⁴⁾	T7	-
I/O	-	-	P72	P81	Y8	W8	343 ⁽³⁾
I/O	-	-	P73	P82	U9	U8	346 ⁽³⁾
I/O	-	-	-	P84	Y9	W9	349 ⁽³⁾
I/O	-	-	-	P85	W10	V9	352 ⁽³⁾
I/O	P33	P50	P74	P86	V10	U9	355 ⁽³⁾
I/O	P34	P51	P75	P87	Y10	T9	358 ⁽³⁾
I/O	P35	P52	P76	P88	Y11	W10	361 ⁽³⁾
I/O (INIT)	P36	P53	P77	P89	W11	V10	364 ⁽³⁾
VCC	P37	P54	P78	P90	VCC ⁽⁴⁾	U10	-
GND	P38	P55	P79	P91	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P39	P56	P80	P92	V11	T10	367 ⁽³⁾
I/O	P40	P57	P81	P93	U11	R10	370 ⁽³⁾
I/O	P41	P58	P82	P94	Y12	W11	373 ⁽³⁾
I/O	P42	P59	P83	P95	W12	V11	376 ⁽³⁾
I/O	-	-	P84	P96	V12	U11	379 ⁽³⁾

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	P85	P97	U12	T11	382 ⁽³⁾
I/O	-	-	-	P99	V13	U12	385 ⁽³⁾
I/O	-	-	-	P100	Y14	T12	388 ⁽³⁾
VCC	-	-	P86	P101	VCC ⁽⁴⁾	W13	-
I/O	P43	P60	P87	P102	Y15	V13	391 ⁽³⁾
I/O	P44	P61	P88	P103	V14	U13	394 ⁽³⁾
I/O	-	P62	P89	P104	W15	T13	397 ⁽³⁾
I/O	-	P63	P90	P105	Y16	W14	400 ⁽³⁾
GND	-	P64	P91	P106	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P107	V15	V14	403 ⁽³⁾
I/O	-	-	P92	P108	W16	U14	406 ⁽³⁾
I/O	-	-	P93	P109	Y17	T14	409 ⁽³⁾
I/O	-	-	P94	P110	V16	R14	412 ⁽³⁾
I/O	-	-	P95	P111	W17	W15	415 ⁽³⁾
I/O	-	-	P96	P112	Y18	U15	418 ⁽³⁾
I/O	P45	P65	P97	P113	U16	V16	421 ⁽³⁾
I/O	P46	P66	P98	P114	V17	U16	424 ⁽³⁾
I/O	-	P67	P99	P115	W18	W17	427 ⁽³⁾
I/O	-	P68	P100	P116	Y19	W18	430 ⁽³⁾
I/O	P47	P69	P101	P117	V18	V17	433 ⁽³⁾
I/O, SGCK3 ⁽¹⁾ , GCK4 ⁽²⁾	P48	P70	P102	P118	W19	V18	436 ⁽³⁾
GND	P49	P71	P103	P119	GND ⁽⁴⁾	GND ⁽⁴⁾	-
DONE	P50	P72	P104	P120	Y20	W19	-
VCC	P51	P73	P105	P121	VCC ⁽⁴⁾	U17	-
PROGRAM	P52	P74	P106	P122	V19	U18	-
I/O (D7 ⁽²⁾)	P53	P75	P107	P123	U19	V19	439 ⁽³⁾
I/O, PGCK3 ⁽¹⁾ , GCK5 ⁽²⁾	P54	P76	P108	P124	U18	U19	442 ⁽³⁾
I/O	-	P77	P109	P125	T17	T16	445 ⁽³⁾
I/O	-	P78	P110	P126	V20	T17	448 ⁽³⁾
I/O	-	-	-	P127	U20	T18	451 ⁽³⁾
I/O	-	-	P111	P128	T18	T19	454 ⁽³⁾
I/O (D6 ⁽²⁾)	P55	P79	P112	P129	T19	R16	457 ⁽³⁾
I/O	P56	P80	P113	P130	T20	R19	460 ⁽³⁾
I/O	-	-	P114	P131	R18	P15	463 ⁽³⁾
I/O	-	-	P115	P132	R19	P17	466 ⁽³⁾
I/O	-	-	P116	P133	R20	P18	469 ⁽³⁾
I/O	-	-	P117	P134	P18	P16	472 ⁽³⁾
GND	-	P81	P118	P135	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P136	P20	P19	475 ⁽³⁾
I/O	-	-	-	P137	N18	N17	478 ⁽³⁾
I/O	-	P82	P119	P138	N19	N18	481 ⁽³⁾
I/O	-	P83	P120	P139	N20	N19	484 ⁽³⁾
VCC	-	-	P121	P140	VCC ⁽⁴⁾	N16	-
I/O (D5 ⁽²⁾)	P57	P84	P122	P141	M17	M19	487 ⁽³⁾
I/O	P58	P85	P123	P142	M18	M17	490 ⁽³⁾

Table 20: User I/O Chart for Spartan/XL FPGAs

Device	Max I/O	Package Type							
		PC84 ⁽¹⁾	VQ100 ⁽¹⁾	CS144 ⁽¹⁾	TQ144	PQ208	PQ240	BG256 ⁽¹⁾	CS280 ⁽¹⁾
XCS05	80	61 ⁽¹⁾	77	-	-	-	-	-	-
XCS10	112	61 ⁽¹⁾	77	-	112	-	-	-	-
XCS20	160	-	77	-	113	160	-	-	-
XCS30	192	-	77 ⁽¹⁾	-	113	169	192	192 ⁽¹⁾	-
XCS40	224	-	-	-	-	169	192	205	-
XCS05XL	80	61 ⁽¹⁾	77 ⁽²⁾	-	-	-	-	-	-
XCS10XL	112	61 ⁽¹⁾	77 ⁽²⁾	112 ⁽¹⁾	112 ⁽²⁾	-	-	-	-
XCS20XL	160	-	77 ⁽²⁾	113 ⁽¹⁾	113 ⁽²⁾	160 ⁽²⁾	-	-	-
XCS30XL	192	-	77 ⁽²⁾	-	113 ⁽²⁾	169 ⁽²⁾	192 ⁽²⁾	192 ⁽²⁾	192 ⁽¹⁾
XCS40XL	224	-	-	-	-	169 ⁽²⁾	192 ⁽²⁾	205 ⁽²⁾	224 ⁽¹⁾

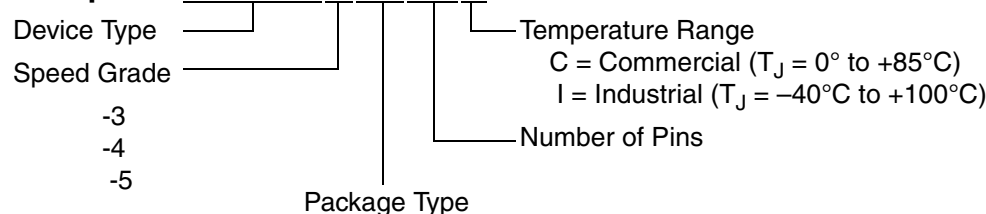
6/25/08

Notes:

1. PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, discontinued by [PDN2004-01](#)
2. These Spartan-XL devices are available in Pb-free package options. The Pb-free packages insert a "G" in the package code. Contact Xilinx for availability.

Ordering Information

Example: XCS20XL-4 PQ208C



BG = Ball Grid Array

BGG = Ball Grid Array (Pb-free)

PC = Plastic Lead Chip Carrier

PQ = Plastic Quad Flat Pack

PQG = Plastic Quad Flat Pack (Pb-free)

VQ = Very Thin Quad Flat Pack

VQG = Very Thin Quad Flat Pack (Pb-free)

TQ = Thin Quad Flat Pack

TQG = Thin Quad Flat Pack (Pb-free)

CS = Chip Scale

Revision History

The following table shows the revision history for this document.

Date	Version	Description
11/20/98	1.3	Added Spartan-XL specs and Power Down.
01/06/99	1.4	All Spartan-XL -4 specs designated Preliminary with no changes.
03/02/00	1.5	Added CS package, updated Spartan-XL specs to Final.
09/19/01	1.6	Reformatted, updated power specs, clarified configuration information. Removed T_{SOL} soldering information from Absolute Maximum Ratings table. Changed Figure 26 : Slave Serial Mode Characteristics: T_{CCH} , T_{CCL} from 45 to 40 ns. Changed Master Mode Configuration Switching Characteristics: T_{CCLK} min. from 80 to 100 ns. Added Total Dist. RAM Bits to Table 1 ; added Start-Up, page 36 characteristics.
06/27/02	1.7	Clarified Express Mode pseudo daisy chain. Added new Industrial options. Clarified XCS30XL CS280 V_{CC} pinout.
06/26/08	1.8	Noted that PC84, CS144, and CS280 packages, and VQ100 and BG256 packages for XCS30 only, are discontinued by PDN2004-01 . Extended description of recommended maximum delay of reconfiguration in Delaying Configuration After Power-Up, page 35 . Added reference to Pb-free package options and provided link to Package Specifications, page 81 . Updated links.
03/01/13	2.0	The products listed in this data sheet are obsolete. See XCN10016 and XCN11010 for further information.