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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	784
Number of Logic Elements/Cells	1862
Total RAM Bits	25088
Number of I/O	169
Number of Gates	40000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcs40xl-5pq208c

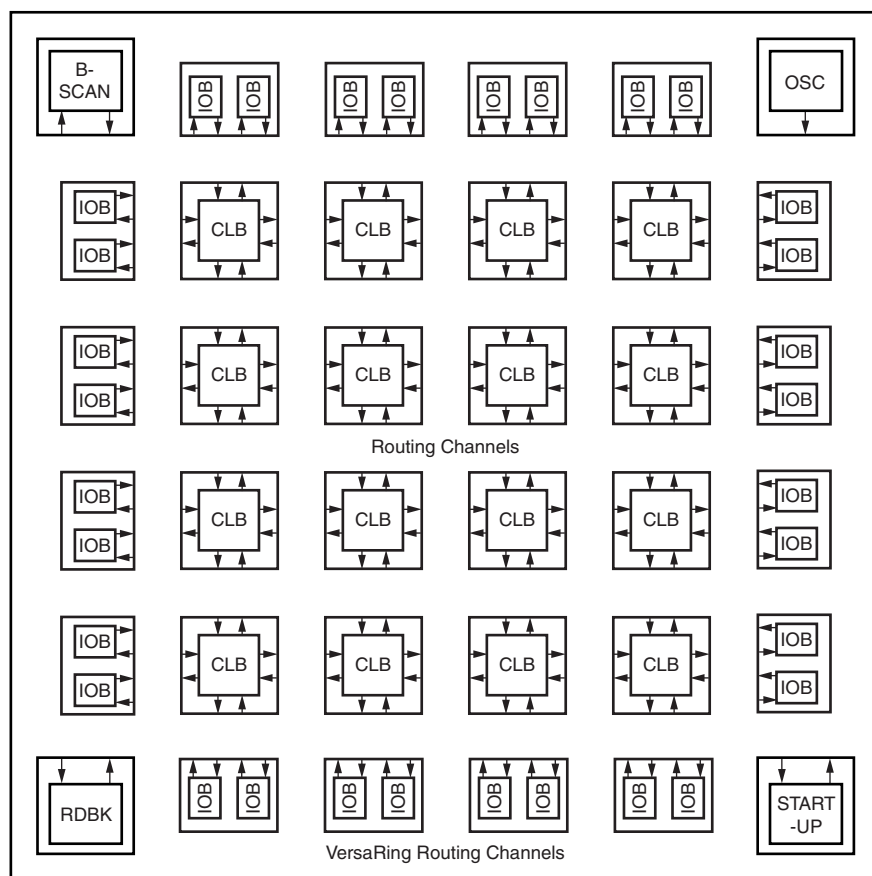
General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in **Figure 1**. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these

memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).


Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.




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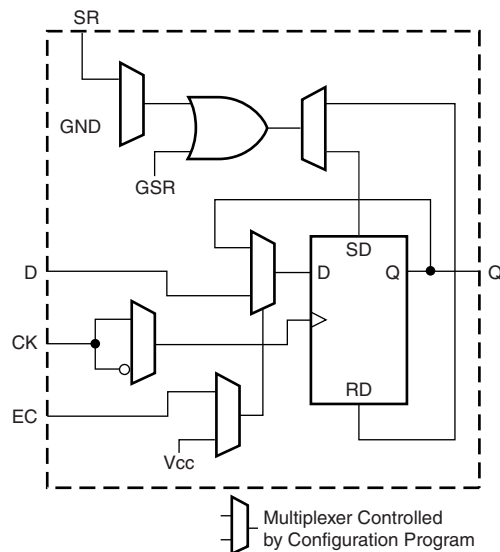
Figure 1: Basic FPGA Block Diagram

Table 2: CLB Storage Element Functionality

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
		1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (Spartan-XL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

- X Don't care
-  Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0* Input is Low or unconnected (default value)
- 1* Input is High or unconnected (default value)



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Figure 3: CLB Flip-Flop Functional Block Diagram

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

CLB Signal Flow Control

In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2, page 4) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinational CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinational output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1-C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

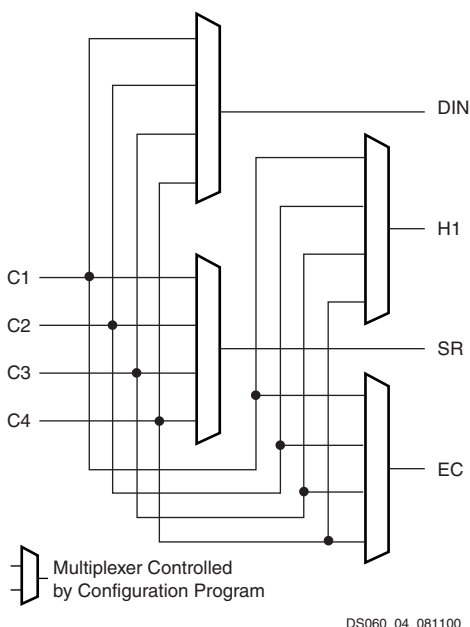


Figure 4: CLB Control Signal Interface

The four internal control signals are:

- EC: Enable Clock
- SR: Asynchronous Set/Reset or H function generator Input 0
- DIN: Direct In or H function generator Input 2
- H1: H function generator Input 1.

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 6 shows a simplified functional block diagram of the Spartan/XL FPGA IOB.

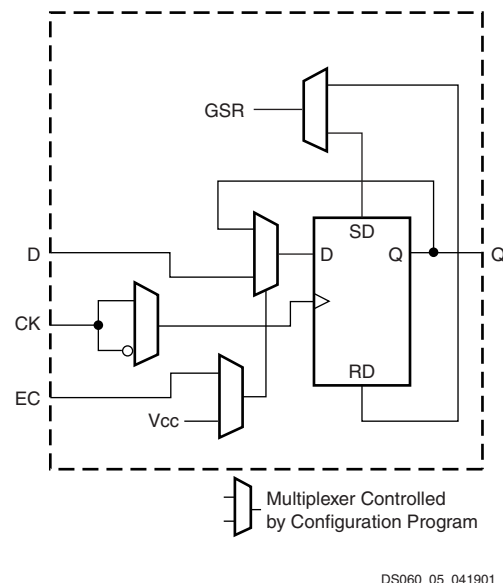


Figure 5: IOB Flip-Flop/Latch Functional Block Diagram

IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 6) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 3, and a simplified block diagram of the register can be seen in Figure 5.

Table 3: Input Register Functionality

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop		1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

- X Don't care.
- Rising edge (clock not inverted).
- SR Set or Reset value. Reset is default.
- 0* Input is Low or unconnected (default value)
- 1* Input is High or unconnected (default value)

Output Multiplexer/2-Input Function Generator (Spartan-XL Family Only)

The output path in the Spartan-XL family IOB contains an additional multiplexer not available in the Spartan family IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass gate, AND gate, OR gate, or XOR gate, with 0, 1, or 2 inverted inputs.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. The select input is the pin used for the output flip-flop clock, OK.

When the multiplexer is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe driven by a global buffer.

The user can specify that the IOB function generator be used by placing special library symbols beginning with the letter "O." For example, a 2-input AND gate in the IOB function generator is called OAND2. Use the symbol input pin labeled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in Figure 7.



Figure 7: AND and MUX Symbols in Spartan-XL IOB

Output Buffer

An active High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (O) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB (see Figure 6, page 7). An output can be configured as open-drain (open-collector) by tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground.

By default, a 5V Spartan device output buffer pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below V_{CC} . Alternatively, the outputs can be globally configured as CMOS drivers, with additional p-channel pull-up transistors pulling to V_{CC} . This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable.

All Spartan-XL device outputs are configured as CMOS drivers, therefore driving rail-to-rail. The Spartan-XL family outputs are individually programmable for 12 mA or 24 mA output drive.

Any 5V Spartan device with its outputs configured in TTL mode can drive the inputs of any typical 3.3V device. Supported destinations for Spartan/XL device outputs are shown in Table 7.

Three-State Register (Spartan-XL Family Only)

Spartan-XL devices incorporate an optional register controlling the three-state enable in the IOBs. The use of the three-state control register can significantly improve output enable and disable time.

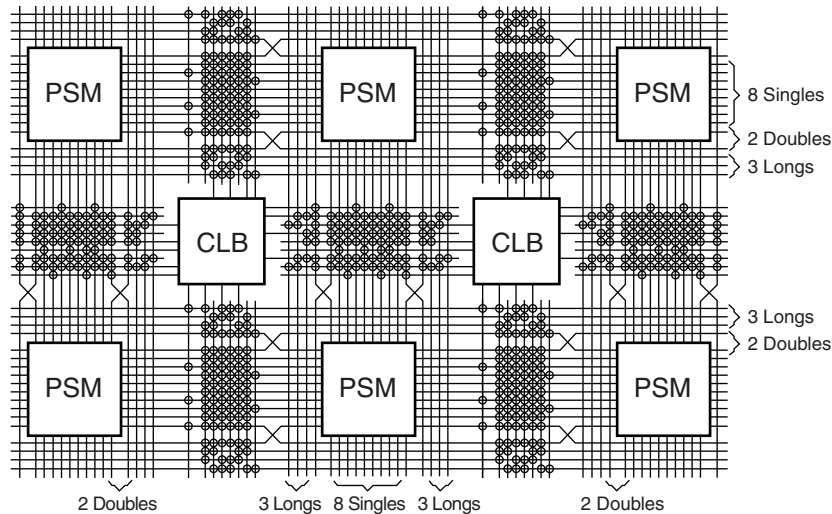
Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

Spartan/XL devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Pull-up and Pull-down Network

Programmable pull-up and pull-down resistors are used for tying unused pins to V_{CC} or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to V_{CC} . The configurable pull-down resistor is an n-channel transistor that pulls to Ground. The value of these resistors is typically 20 K Ω – 100 K Ω (See "Spartan Family DC Characteristics Over Operating Conditions" on page 43.).

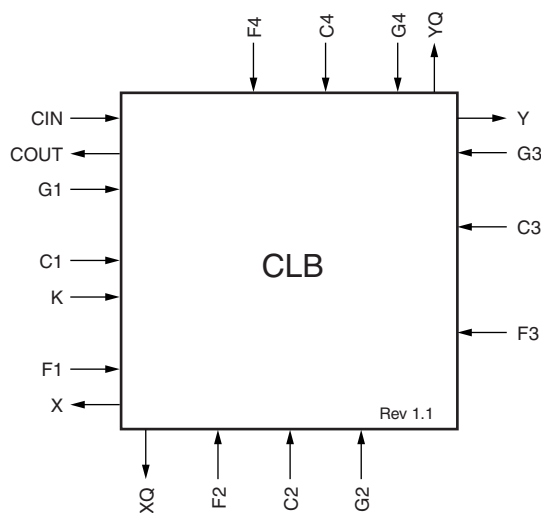


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Figure 8: Spartan/XL CLB Routing Channels and Interface Block Diagram

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.



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Figure 9: CLB Interconnect Signals

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs. Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

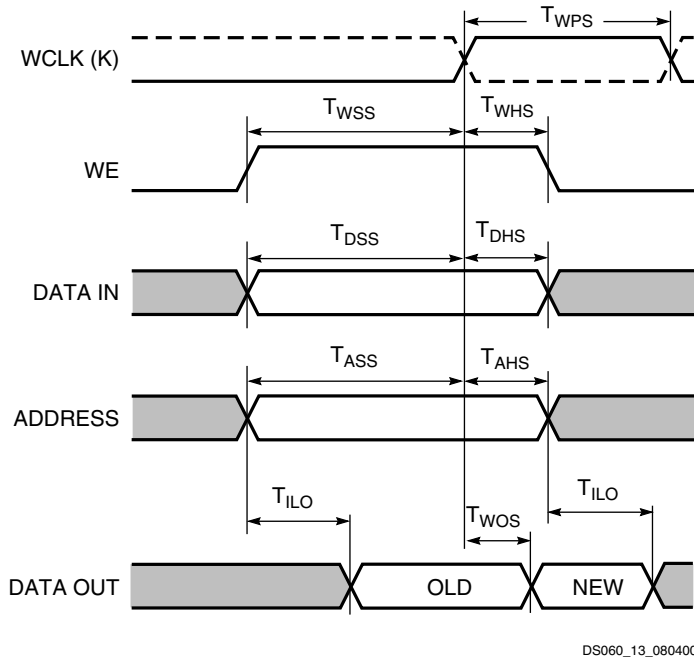


Figure 13: Data Write and Access Timing for RAM

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be

inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO} , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS} , the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by $A[3:0]$ while the second provides only for read operations at the address specified independently by $DPRA[3:0]$. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14. The dual-port RAM signals and the

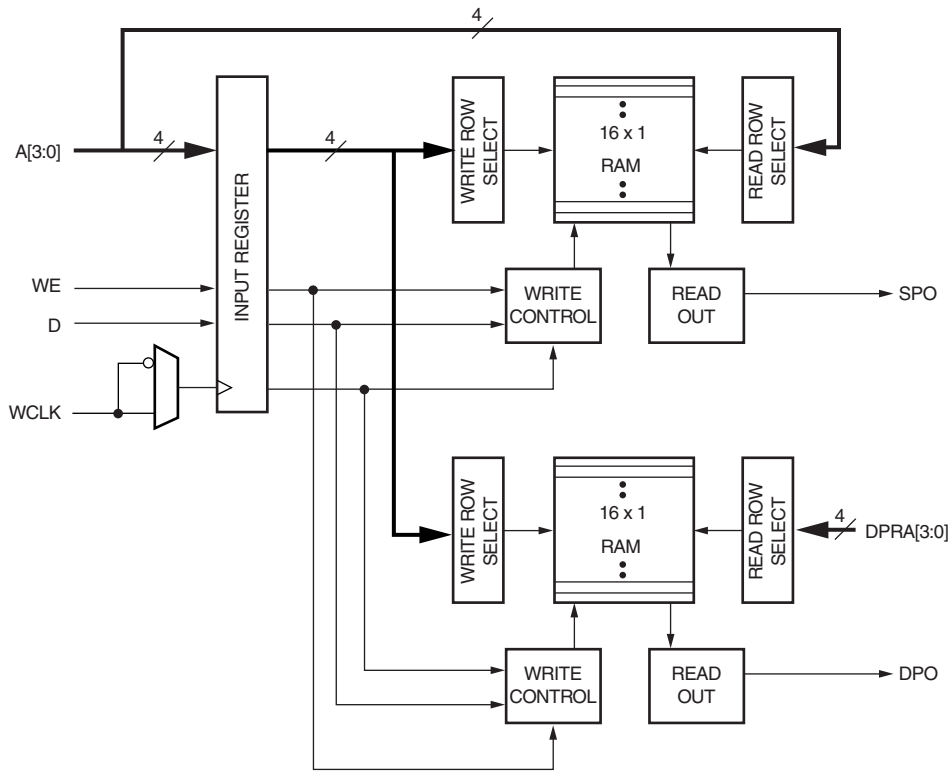


Figure 14: Logic Diagram for the Dual-Port RAM

CLB signals from which they are originally derived are shown in Table 10.

Table 10: Dual-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F[4:1]
DPRA[3:0]	Read Address for Dual-Port	G[4:1]
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F _{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G _{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on Using RAM Inside CLBs

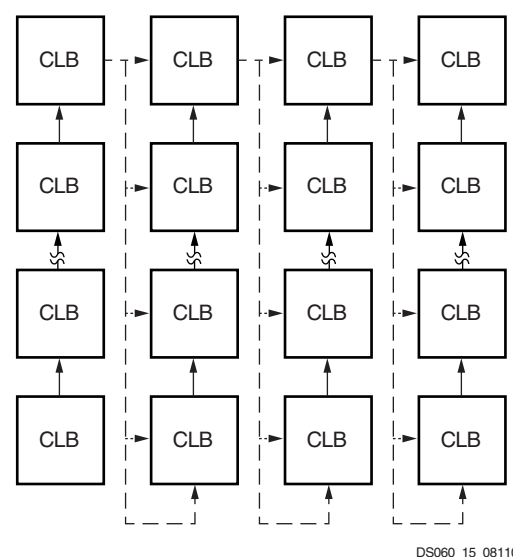
Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "Xilinx Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

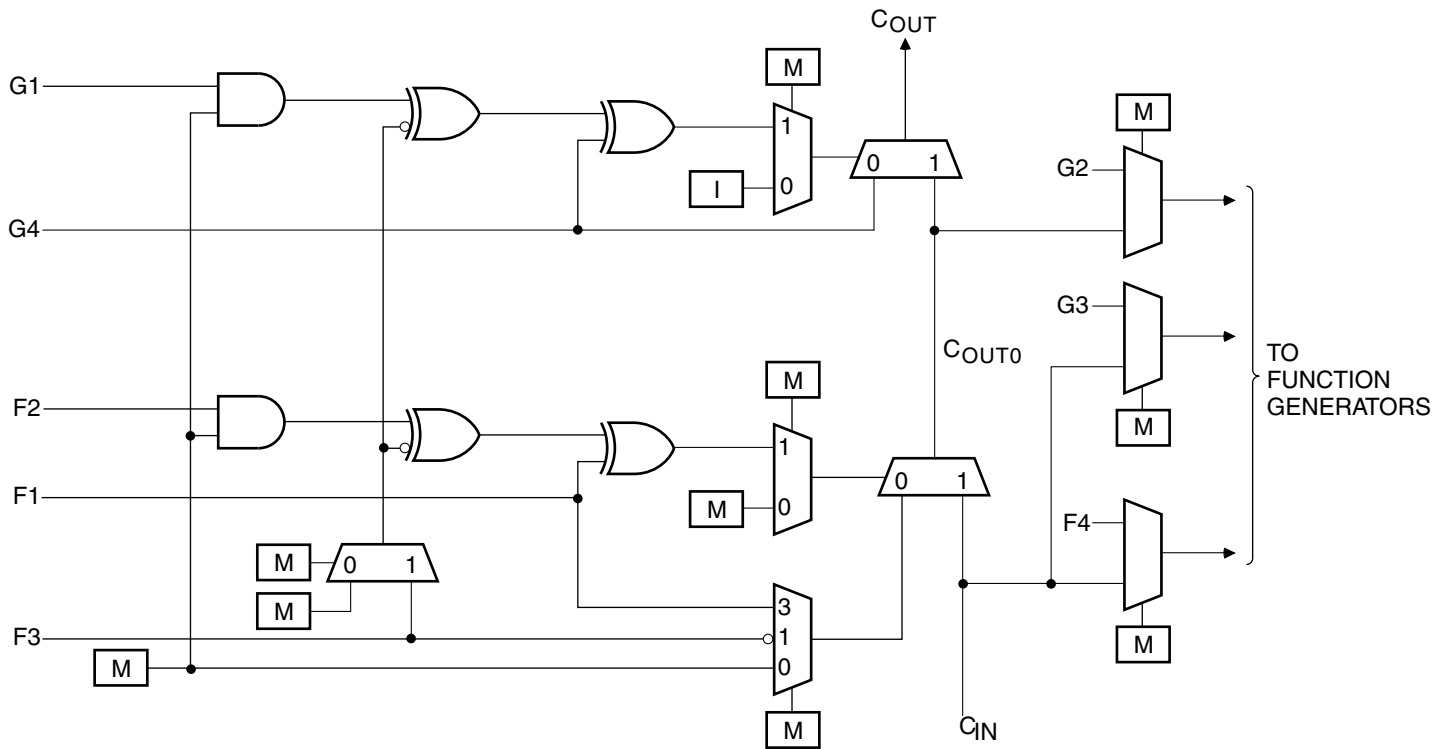
Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in micro-processor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan



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Figure 15: Available Spartan/XL Carry Propagation Paths



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Figure 17: Detail of Spartan/XL Dedicated Carry Logic

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 11.

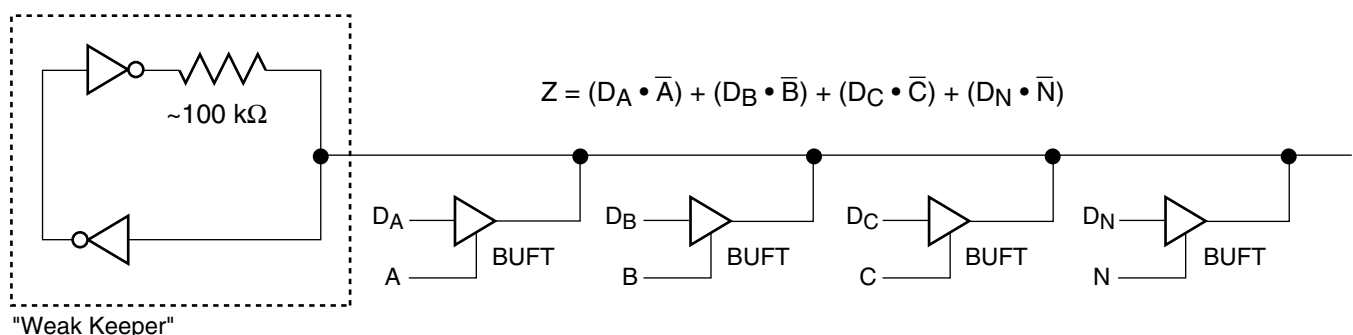
Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 11.

Table 11: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN



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Figure 18: 3-state Buffers Implement a Multiplexer

Figure 20 is a diagram of the Spartan/XL FPGA boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See **Configuration Through the Boundary Scan Pins**, page 37.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL FPGA boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 12.

Even if the boundary scan symbol is used in a design, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state.
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "Boundary Scan in FPGA Devices."

Boundary Scan Enhancements (Spartan-XL Family Only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

IDCODE: The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

c = the company code (49h for Xilinx)

a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)

f = the family code (02h for Spartan-XL family)

v = the die version number

Table 13: IDCODEs Assigned to Spartan-XL FPGAs

FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

Configuration State: The configuration state is available to JTAG controllers.

Configuration Disable: The JTAG port can be prevented from configuring the FPGA.

TCK Startup: TCK can now be used to clock the start-up block in addition to other user clocks.

CCLK Holdoff: Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

Reissue Configure: The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

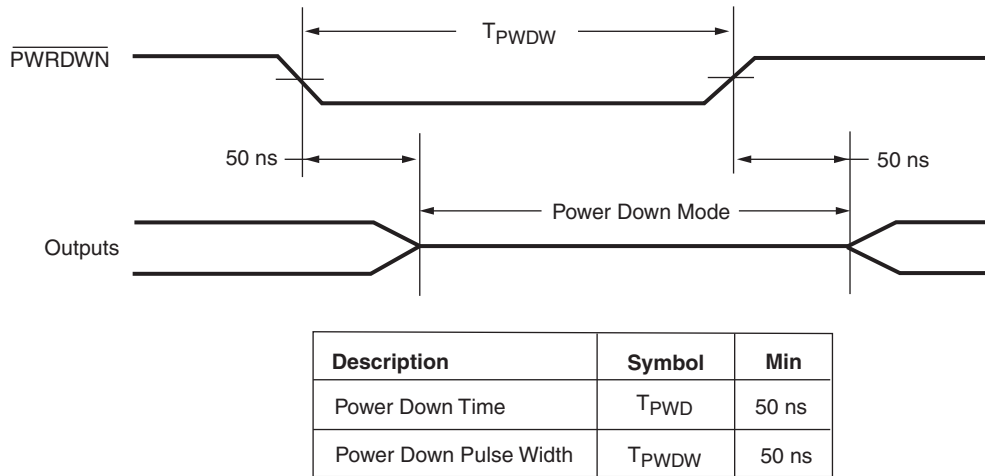
Bypass FF: Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

Power-Down (Spartan-XL Family Only)

All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low power-down pin (PWRDWN) to reduce supply current to 100 μ A typical. The PWRDWN pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The PWRDWN pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

V_{CC} must continue to be supplied during Power-down, and configuration data is maintained. When the PWRDWN pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The PROGRAM pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

PWRDWN has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before PWRDWN to affect the order of events. When the PWRDWN signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of PWRDWN before using the device.



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Figure 23: **PWRDWN** Pulse Timing

Power-down retains the configuration, but loses all data stored in the device flip-flops. All inputs are interpreted as Low, but the internal combinatorial logic is fully functional. Make sure that the combination of all inputs Low and all flip-flops set or reset in your design will not generate internal oscillations, or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line.

During configuration, the **PWRDWN** pin must be High. If the Power Down state is entered before or during configuration, the device will restart configuration once the **PWRDWN** signal is removed. Note that the configuration pins are affected by Power Down and may not reflect their normal function. If there is an external pull-up resistor on the **DONE** pin, it will be High during Power Down even if the device is not yet configured. Similarly, if **PWRDWN** is asserted before configuration is completed, the **INIT** pin will not indicate status information.

Note that the **PWRDWN** pin is not part of the Boundary Scan chain. Therefore, the Spartan-XL family has a separate set of BSDL files than the 5V Spartan family. Boundary scan logic is not usable during Power Down.

Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan/XL devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell

that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Configuration Mode Control

5V Spartan devices have two configuration modes.

- **MODE** = 1 sets Slave Serial mode
- **MODE** = 0 sets Master Serial mode

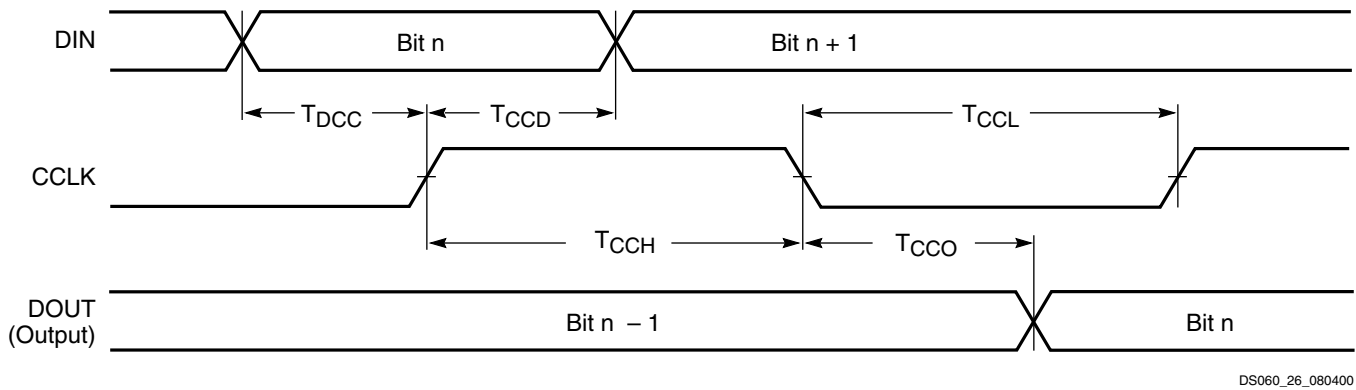
3V Spartan-XL devices have three configuration modes.

- **M1/M0** = 11 sets Slave Serial mode
- **M1/M0** = 10 sets Master Serial mode
- **M1/M0** = 0X sets Express mode

In addition to these modes, the device can be configured through the Boundary Scan logic (See "Configuration Through the Boundary Scan Pins" on page 37.).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pins are unused. The Mode pins have a weak pull-up resistor turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the **MODE/M0** pin should be connected directly to GND, or through a pull-down resistor of 1 K Ω or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during con-



Symbol		Description	Min	Max	Units
T_{DCC}	CCLK	DIN setup	20	-	ns
T_{CCD}		DIN hold	0	-	ns
T_{CCO}		DIN to DOUT	-	30	ns
T_{CCH}		High time	40	-	ns
T_{CCL}		Low time	40	-	ns
F_{CC}		Frequency	-	12.5	MHz

Notes:

1. Configuration must be delayed until the \overline{INIT} pins of all daisy-chained FPGAs are High.

Figure 26: Slave Serial Mode Programming Switching Characteristics

Express Mode (Spartan-XL Family Only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 16, page 32.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

Pseudo Daisy Chain

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices

are in Express mode. Concatenated bitstreams are used to configure the chain of Express mode devices so that each device receives a separate header. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the next header and configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized

Table 16: Spartan/XL Data Stream Formats

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT[23:0]	COUNT[23:0] ⁽¹⁾
Fill Bits	1111b	-
Field Check Code	-	11010010b
Start Field	0b	11111110b ⁽²⁾
Data Frame	DATA[n-1:0]	DATA[n-1:0]
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	-	FFD2FFFFFFh
Postamble	01111111b	-
Start-Up Bytes ⁽³⁾	FFh	FFFFFFFFFFFFFFh

Legend:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Notes:

1. Not used by configuration logic.
2. 11111111b for XCS40XL only.
3. Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL family Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the $\overline{\text{INIT}}$ pin. In Master serial mode, CCLK continues to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the PROGRAM pin Low or cycling VCC.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 16. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

Spartan Family Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more pre-

cise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Spartan Family Output Flip-Flop, Clock-to-Out

Symbol	Description	Device	Speed Grade		Units
			-4	-3	
			Max	Max	
Global Primary Clock to TTL Output using OFF					
T _{ICKOF}	Fast	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
T _{ICKO}	Slew-rate limited	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
T _{ICKSOF}	Fast	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
T _{ICKSO}	Slew-rate limited	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
T _{CMOSOF}	Fast	All devices	0.8	1.0	ns
T _{CMOSO}	Slew-rate limited	All devices	1.5	2.0	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see [Figure 34](#).
3. OFF = Output Flip-Flop

Spartan-XL Family Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Family Absolute Maximum Ratings⁽¹⁾

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		−0.5 to 4.0	V
V_{IN}	Input voltage relative to GND	5V Tolerant I/O Checked ^(2, 3)	−0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	−0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	5V Tolerant I/O Checked ^(2, 3)	−0.5 to 5.5	V
		Not 5V Tolerant I/Os ^(4, 5)	−0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)		−65 to +150	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA and undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to −2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
- Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to −2.0V or overshoot to $V_{CC} + 2.0V$, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Spartan-XL Family Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ ⁽¹⁾	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage ⁽²⁾		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage ⁽²⁾		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:

- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement threshold is ~50% of V_{CC} .

Spartan-XL Family DC Characteristics Over Operating Conditions

Symbol	Description		Min	Typ.	Max	Units
V _{OH}	High-level output voltage @ I _{OH} = −4.0 mA, V _{CC} min (LVTTL)		2.4	-	-	V
	High-level output voltage @ I _{OH} = −500 μA, (LVCMOS)		90% V _{CC}	-	-	V
V _{OL}	Low-level output voltage @ I _{OL} = 12.0 mA, V _{CC} min (LVTTL) ⁽¹⁾		-	-	0.4	V
	Low-level output voltage @ I _{OL} = 24.0 mA, V _{CC} min (LVTTL) ⁽²⁾		-	-	0.4	V
	Low-level output voltage @ I _{OL} = 1500 μA, (LVCMOS)		-	-	10% V _{CC}	V
V _{DR}	Data retention supply voltage (below which configuration data may be lost)		2.5	-	-	V
I _{CCO}	Quiescent FPGA supply current ^(3,4)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I _{CCPD}	Power Down FPGA supply current ^(3,5)	Commercial	-	0.1	2.5	mA
		Industrial	-	0.1	5	mA
I _L	Input or output leakage current		−10	-	10	μA
C _{IN}	Input capacitance (sample tested)		-	-	10	pF
I _{RPU}	Pad pull-up (when selected) @ V _{IN} = 0V (sample tested)		0.02	-	0.25	mA
I _{RPD}	Pad pull-down (when selected) @ V _{IN} = 3.3V (sample tested)		0.02	-	-	mA

Notes:

1. With up to 64 pins simultaneously sinking 12 mA (default mode).
2. With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
3. With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
4. With no output current loads, no active input resistors, and all package pins at V_{CC} or GND.
5. With \overline{PWRDWN} active.

Supply Current Requirements During Power-On

Spartan-XL FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CC} lines for a successful power on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description	Min	Max	Units
I_{CCPO}	Total V_{CC} supply current required during power-on	100	-	mA
T_{CCPO}	V_{CC} ramp time ^(2,3)	-	50	ms

Notes:

1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CC} ramps from 0 to 3.3V.
2. The ramp time is measured from GND to V_{CC} max on a fully loaded board.
3. V_{CC} must not dip in the negative direction during power on.

Spartan-XL Family IOB Output Switching Characteristic Guidelines

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to

the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Propagation Delays							
T _{OKPOF}	Clock (OK) to Pad, fast	All devices	-	3.2	-	3.7	ns
T _{OPF}	Output (O) to Pad, fast	All devices	-	2.5	-	2.9	ns
T _{TSHZ}	3-state to Pad High-Z (slew-rate independent)	All devices	-	2.8	-	3.3	ns
T _{TSONF}	3-state to Pad active and valid, fast	All devices	-	2.6	-	3.0	ns
T _{OFFPF}	Output (O) to Pad via Output MUX, fast	All devices	-	3.7	-	4.4	ns
T _{OKFPF}	Select (OK) to Pad via Output MUX, fast	All devices	-	3.3	-	3.9	ns
T _{SLOW}	For Output SLOW option add	All devices	-	1.5	-	1.7	ns
Setup and Hold Times							
T _{OOK}	Output (O) to clock (OK) setup time	All devices	0.5	-	0.5	-	ns
T _{OKO}	Output (O) to clock (OK) hold time	All devices	0.0	-	0.0	-	ns
T _{ECOK}	Clock Enable (EC) to clock (OK) setup time	All devices	0.0	-	0.0	-	ns
T _{OKEC}	Clock Enable (EC) to clock (OK) hold time	All devices	0.1	-	0.2	-	ns
Global Set/Reset							
T _{MRW}	Minimum GSR pulse width	All devices	10.5	-	11.5	-	ns
T _{RPO}	Delay from GSR input to any Pad	XCS05XL	-	11.9	-	14.0	ns
		XCS10XL	-	12.4	-	14.5	ns
		XCS20XL	-	12.9	-	15.0	ns
		XCS30XL	-	13.9	-	16.0	ns
		XCS40XL	-	14.9	-	17.0	ns

Notes:

- Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
- Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See **Global Signals: GSR and GTS**, page 20 for more information.

Device pins for Spartan/XL devices are described in **Table 18**.

Some Spartan-XL devices are available in Pb-free package options. The Pb-free package options have the same pin-outs as the standard package options.

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
V _{CC}	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 – 0.1 μ F capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See Violating the Maximum High and Low Time Specification for the Readback Clock , page 39 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an open-drain output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.

XCS30 and XCS30XL Device Pinouts (Continued)

XCS30/XL Pad Name	VQ100 ⁽⁵⁾	TQ144	PQ208	PQ240	BG256 ⁽⁵⁾	CS280 ^(2,5)	Bndry Scan
I/O	-	-	P124	P144	M20	L19	493 ⁽³⁾
I/O	-	-	P125	P145	L19	L18	496 ⁽³⁾
I/O	P59	P86	P126	P146	L18	L17	499 ⁽³⁾
I/O	P60	P87	P127	P147	L20	L16	502 ⁽³⁾
I/O (D4 ⁽²⁾)	P61	P88	P128	P148	K20	K19	505 ⁽³⁾
I/O	P62	P89	P129	P149	K19	K18	508 ⁽³⁾
VCC	P63	P90	P130	P150	VCC ⁽⁴⁾	K17	-
GND	P64	P91	P131	P151	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O (D3 ⁽²⁾)	P65	P92	P132	P152	K18	K16	511 ⁽³⁾
I/O	P66	P93	P133	P153	K17	K15	514 ⁽³⁾
I/O	P67	P94	P134	P154	J20	J19	517 ⁽³⁾
I/O	-	P95	P135	P155	J19	J18	520 ⁽³⁾
I/O	-	-	P136	P156	J18	J17	523 ⁽³⁾
I/O	-	-	P137	P157	J17	J16	526 ⁽³⁾
I/O (D2 ⁽²⁾)	P68	P96	P138	P159	H19	H17	529 ⁽³⁾
I/O	P69	P97	P139	P160	H18	H16	532 ⁽³⁾
VCC	-	-	P140	P161	VCC ⁽⁴⁾	G19	-
I/O	-	P98	P141	P162	G19	G18	535 ⁽³⁾
I/O	-	P99	P142	P163	F20	G17	538 ⁽³⁾
I/O	-	-	-	P164	G18	G16	541 ⁽³⁾
I/O	-	-	-	P165	F19	F19	544 ⁽³⁾
GND	-	P100	P143	P166	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	-	-	P167	F18	F18	547 ⁽³⁾
I/O	-	-	P144	P168	E19	F17	550 ⁽³⁾
I/O	-	-	P145	P169	D20	F16	553 ⁽³⁾
I/O	-	-	P146	P170	E18	F15	556 ⁽³⁾
I/O	-	-	P147	P171	D19	E19	559 ⁽³⁾
I/O	-	-	P148	P172	C20	E17	562 ⁽³⁾
I/O (D1 ⁽²⁾)	P70	P101	P149	P173	E17	E16	565 ⁽³⁾
I/O	P71	P102	P150	P174	D18	D19	568 ⁽³⁾
I/O	-	P103	P151	P175	C19	C19	571 ⁽³⁾
I/O	-	P104	P152	P176	B20	B19	574 ⁽³⁾
I/O (D0 ⁽²⁾ , DIN)	P72	P105	P153	P177	C18	C18	577 ⁽³⁾
I/O, SGCK4 ⁽¹⁾ , GCK6 ⁽²⁾ (DOUT)	P73	P106	P154	P178	B19	B18	580 ⁽³⁾
CCLK	P74	P107	P155	P179	A20	A19	-
VCC	P75	P108	P156	P180	VCC ⁽⁴⁾	C17	-
O, TDO	P76	P109	P157	P181	A19	B17	0
GND	P77	P110	P158	P182	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P78	P111	P159	P183	B18	A18	2
I/O, PGCK4 ⁽¹⁾ , GCK7 ⁽²⁾	P79	P112	P160	P184	B17	A17	5
I/O	-	P113	P161	P185	C17	D16	8
I/O	-	P114	P162	P186	D16	C16	11
I/O (CS1 ⁽²⁾)	P80	P115	P163	P187	A18	B16	14
I/O	P81	P116	P164	P188	A17	A16	17
I/O	-	-	P165	P189	C16	D15	20

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
GND	P25	P29	GND ⁽⁴⁾	GND ⁽⁴⁾	-
VCC	P26	P30	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P27	P31	L2	K3	254
I/O	P28	P32	L3	K4	257
I/O	P29	P33	L4	K5	260
I/O	P30	P34	M1	L1	263
I/O	P31	P35	M2	L2	266
I/O	P32	P36	M3	L3	269
I/O	-	-	M4	L4	272
I/O	-	-	-	M1	275
I/O	-	P38	N1	M2	278
I/O	-	P39	N2	M3	281
VCC	P33	P40	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P34	P41	P1	N1	284
I/O	P35	P42	P2	N2	287
I/O	P36	P43	R1	N3	290
I/O	P37	P44	P3	N4	293
GND	P38	P45	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	-	P46	T1	P1	296
I/O	P39	P47	R3	P2	299
I/O	P40	P48	T2	P3	302
I/O	P41	P49	U1	P4	305
I/O	P42	P50	T3	P5	308
I/O	P43	P51	U2	R1	311
I/O	-	-	-	R2	314
I/O	-	-	-	R4	317
I/O	P44	P52	V1	T1	320
I/O	P45	P53	T4	T2	323
I/O	P46	P54	U3	T3	326
I/O	P47	P55	V2	U1	329
I/O	P48	P56	W1	V1	332
I/O, SGCK2 ⁽¹⁾ , GCK2 ⁽²⁾	P49	P57	V3	U2	335
Not Connected ⁽¹⁾ M1 ⁽²⁾	P50	P58	W2	V2	338
GND	P51	P59	GND ⁽⁴⁾	GND ⁽⁴⁾	-
MODE ⁽¹⁾ , M0 ⁽²⁾	P52	P60	Y1	W1	341
VCC	P53	P61	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
Not Connected ⁽¹⁾ PWRDWN ⁽²⁾	P54	P62	W3	V3	342 ⁽¹⁾
I/O, PGCK2 ⁽¹⁾ , GCK3 ⁽²⁾	P55	P63	Y2	W2	343 ⁽³⁾

XCS40 and XCS40XL Device Pinouts

XCS40/XL Pad Name	PQ208	PQ240	BG256	CS280 ^(2,5)	Bndry Scan
I/O (HDC)	P56	P64	W4	W3	346 ⁽³⁾
I/O	P57	P65	V4	T4	349 ⁽³⁾
I/O	P58	P66	U5	U4	352 ⁽³⁾
I/O	P59	P67	Y3	V4	355 ⁽³⁾
I/O (LDC)	P60	P68	Y4	W4	358 ⁽³⁾
I/O	-	-	-	R5	361 ⁽³⁾
I/O	-	-	-	U5	364 ⁽³⁾
I/O	P61	P69	V5	T5	367 ⁽³⁾
I/O	P62	P70	W5	W5	370 ⁽³⁾
I/O	P63	P71	Y5	R6	373 ⁽³⁾
I/O	P64	P72	V6	U6	376 ⁽³⁾
I/O	P65	P73	W6	V6	379 ⁽³⁾
I/O	-	P74	Y6	T6	382 ⁽³⁾
GND	P66	P75	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P67	P76	W7	W6	385 ⁽³⁾
I/O	P68	P77	Y7	U7	388 ⁽³⁾
I/O	P69	P78	V8	V7	391 ⁽³⁾
I/O	P70	P79	W8	W7	394 ⁽³⁾
VCC	P71	P80	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P72	P81	Y8	W8	397 ⁽³⁾
I/O	P73	P82	U9	U8	400 ⁽³⁾
I/O	-	-	V9	V8	403 ⁽³⁾
I/O	-	-	W9	T8	406 ⁽³⁾
I/O	-	P84	Y9	W9	409 ⁽³⁾
I/O	-	P85	W10	V9	412 ⁽³⁾
I/O	P74	P86	V10	U9	415 ⁽³⁾
I/O	P75	P87	Y10	T9	418 ⁽³⁾
I/O	P76	P88	Y11	W10	421 ⁽³⁾
I/O (INIT)	P77	P89	W11	V10	424 ⁽³⁾
VCC	P78	P90	VCC ⁽⁴⁾	VCC ⁽⁴⁾	VCC ⁽⁴⁾
GND	P79	P91	GND ⁽⁴⁾	GND ⁽⁴⁾	-
I/O	P80	P92	V11	T10	427 ⁽³⁾
I/O	P81	P93	U11	R10	430 ⁽³⁾
I/O	P82	P94	Y12	W11	433 ⁽³⁾
I/O	P83	P95	W12	V11	436 ⁽³⁾
I/O	P84	P96	V12	U11	439 ⁽³⁾
I/O	P85	P97	U12	T11	442 ⁽³⁾
I/O	-	-	Y13	W12	445 ⁽³⁾
I/O	-	-	W13	V12	448 ⁽³⁾
I/O	-	P99	V13	U12	451 ⁽³⁾
I/O	-	P100	Y14	T12	454 ⁽³⁾
VCC	P86	P101	VCC ⁽⁴⁾	VCC ⁽⁴⁾	-
I/O	P87	P102	Y15	V13	457 ⁽³⁾
I/O	P88	P103	V14	U13	460 ⁽³⁾
I/O	P89	P104	W15	T13	463 ⁽³⁾