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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1452 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 175 |
| Number of Gates | 24000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 125°C (TJ) |
| Package / Case | 208-BFCQFP with Tie Bar |
| Supplier Device Package | 208-CQFP (75x75) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/5962-9956903qyc |

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# SX Family FPGAs

## General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or “sea-of-modules”), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX’s flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

## SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

### Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

### Logic Module Design

The SX family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

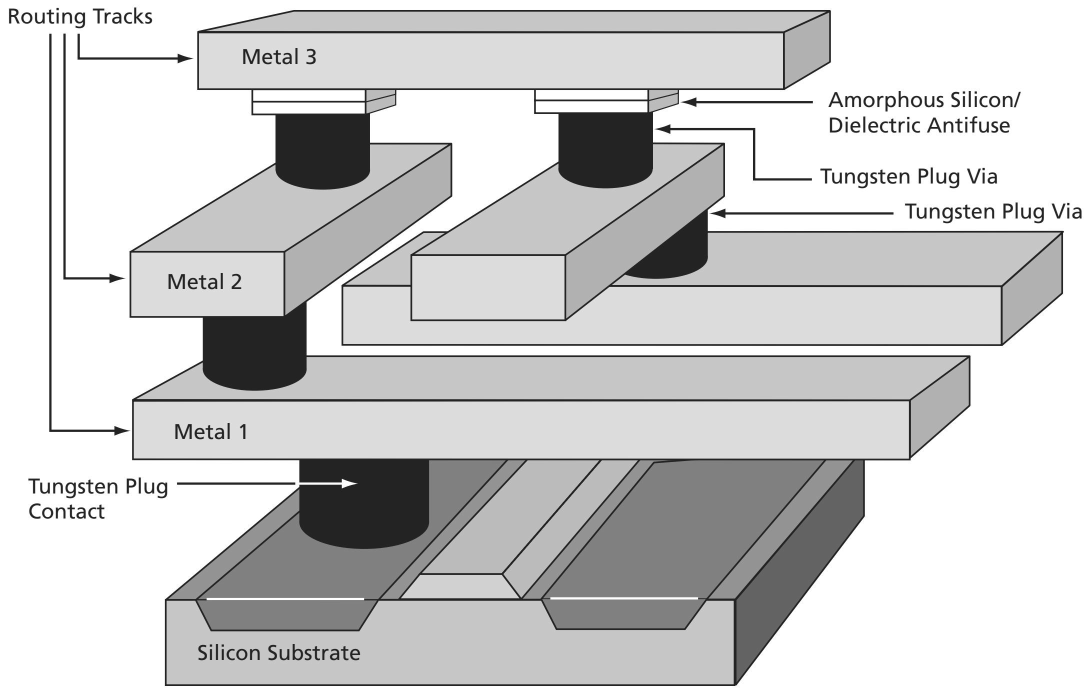



*Figure 1-1* • **SX Family Interconnect Elements**

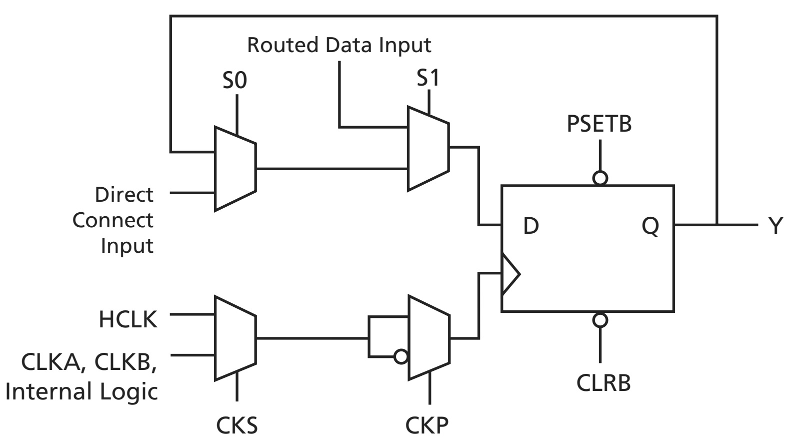



*Figure 1-2* • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

## Other Architectural Features

### Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35 μ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with a capacitance of 1.0 fF for low signal impedance.

### Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

### I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

### Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

*Table 1-1* • **Supply Voltages**

| Device | $V_{CCA}$ | $V_{CCI}$ | $V_{CCR}$ | Maximum Input Tolerance | Maximum Output Drive |
|---|---|---|---|---|---|
| A54SX08<br>A54SX16<br>A54SX32 | 3.3 V | 3.3 V | 5.0 V | 5.0 V | 3.3 V |
| A54SX16-P* | 3.3 V | 3.3 V | 3.3 V | 3.3 V | 3.3 V |
| | 3.3 V | 3.3 V | 5.0 V | 5.0 V | 3.3 V |
| | 3.3 V | 5.0 V | 5.0 V | 5.0 V | 5.0 V |

***Note:*** **A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.*

## Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 1-2. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

*Table 1-2* • **Boundary Scan Pin Functionality**

| Program Fuse Blown (Dedicated Test Mode) | Program Fuse Not Blown (Flexible Mode) |
|---|---|
| TCK, TDI, TDO are dedicated BST pins. | TCK, TDI, TDO are flexible and may be used as I/Os. |
| No need for pull-up resistor for TMS | Use a pull-up resistor of 10 kΩ on TMS. |

## Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-7). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the Table 1-5 on page 1-8 for detailed specifications.

*Figure 1-7* • **Device Selection Wizard**

## Development Tool Support

The SX family of FPGAs is fully supported by both the Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the Libero IDE flow diagram (located on the Actel website) for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators, and the simulation results can be cross-probed with Silicon Explorer II, Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys®, and Cadence® Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

## Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-8 on page 1-7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

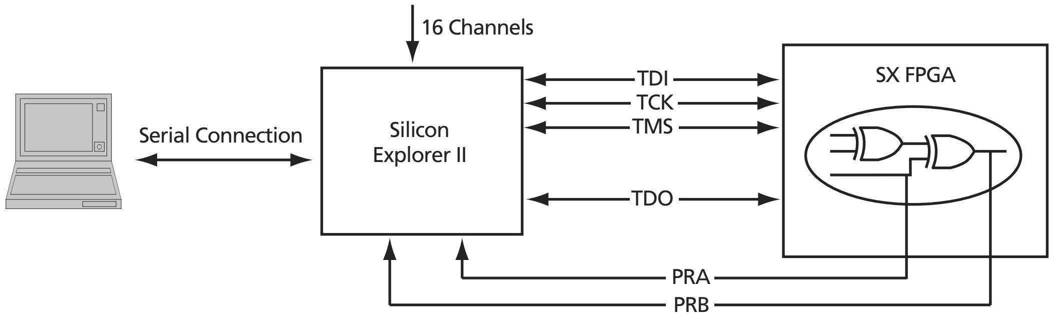



*Figure 1-8* • **Probe Setup**

# Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

# 3.3 V / 5 V Operating Conditions

*Table 1-3* • **Absolute Maximum Ratings**[1]

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CCR}$[2] | DC Supply Voltage[3] | –0.3 to + 6.0 | V |
| $V_{CCA}$[2] | DC Supply Voltage | –0.3 to + 4.0 | V |
| $V_{CCI}$[2] | DC Supply Voltage (A54SX08, A54SX16, A54SX32) | –0.3 to + 4.0 | V |
| $V_{CCI}$[2] | DC Supply Voltage (A54SX16P) | –0.3 to + 6.0 | V |
| $V_I$ | Input Voltage | –0.5 to + 5.5 | V |
| $V_O$ | Output Voltage | –0.5 to + 3.6 | V |
| $I_{IO}$ | I/O Source Sink Current[3] | –30 to + 5.0 | mA |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

***Notes:***

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *$V_{CCR}$ in the A54SX16P must be greater than or equal to $V_{CCI}$ during power-up and power-down sequences and during normal operation.*
3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC}$ + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward-bias and can draw excessive current.*

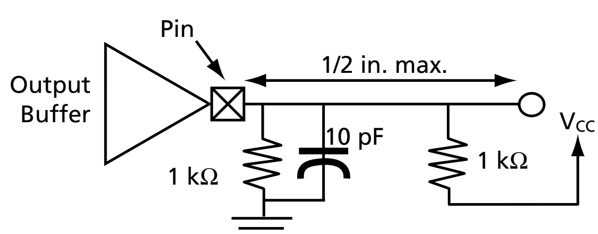
# A54SX16P AC Specifications (3.3 V PCI Operation)

*Table 1-9* • **A54SX16P AC Specifications (3.3 V PCI Operation)**

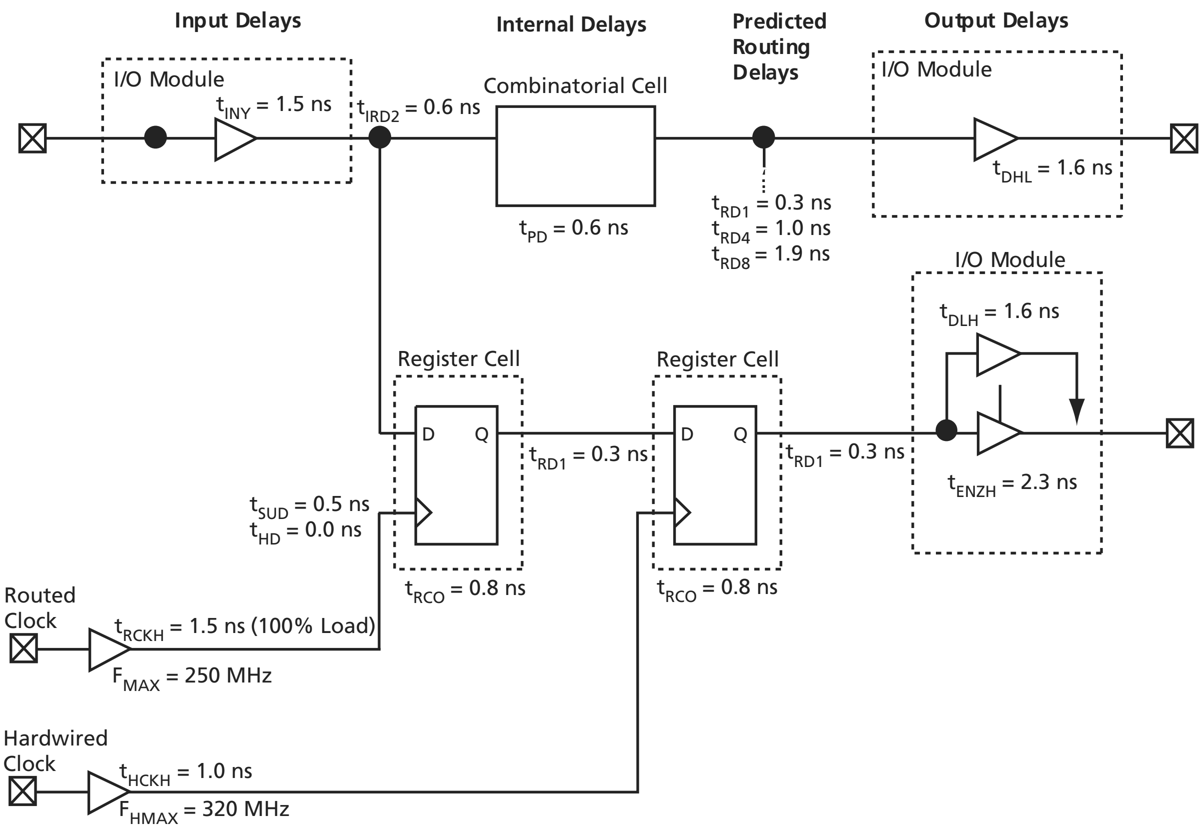
| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \le 0.3V_{CC}$ [1] | | | mA |
| | | $0.3V_{CC} \le V_{OUT} < 0.9V_{CC}$ [1] | $-12V_{CC}$ | | mA |
| | | $0.7V_{CC} < V_{OUT} < V_{CC}$ [1, 2] | $-17.1 + (V_{CC} - V_{OUT})$ | EQ 1-3 on page 1-14 | |
| | (Test Point) | $V_{OUT} = 0.7V_{CC}$ [2] | | $-32V_{CC}$ | mA |
| $I_{OL(AC)}$ | Switching Current High | $V_{CC} > V_{OUT} \ge 0.6V_{CC}$ [1] | | | mA |
| | | $0.6V_{CC} > V_{OUT} > 0.1V_{CC}$ [1] | $16V_{CC}$ | | mA |
| | | $0.18V_{CC} > V_{OUT} > 0$ [1, 2] | $26.7V_{OUT}$ | EQ 1-4 on page 1-14 | mA |
| | (Test Point) | $V_{OUT} = 0.18V_{CC}$ [2] | | $38V_{CC}$ | |
| $I_{CL}$ | Low Clamp Current | $-3 < V_{IN} \le -1$ | $-25 + (V_{IN} + 1)/0.015$ | | mA |
| $I_{CH}$ | High Clamp Current | $-3 < V_{IN} \le -1$ | $25 + (V_{IN} - V_{OUT} - 1)/0.015$ | | mA |
| $slew_R$ | Output Rise Slew Rate[3] | $0.2V_{CC}$ to $0.6V_{CC}$ load | 1 | 4 | V/ns |
| $slew_F$ | Output Fall Slew Rate[3] | $0.6V_{CC}$ to $0.2V_{CC}$ load | 1 | 4 | V/ns |

***Notes:***

1. *Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*



# SX Timing Model




***Note:*** *Values shown for A54SX08-3, worst-case commercial conditions.*

*Figure 1-12* • **SX Timing Model**

### Hardwired Clock

External Setup $= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH}$

$= 1.5 + 0.3 + 0.5 - 1.0 = 1.3$ ns

*EQ 1-15*

Clock-to-Out (Pin-to-Pin)

$= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

$= 1.0 + 0.8 + 0.3 + 1.6 = 3.7$ ns

*EQ 1-16*

### Routed Clock

External Setup $= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$

$= 1.5 + 0.3 + 0.5 - 1.5 = 0.8$ ns

*EQ 1-17*

Clock-to-Out (Pin-to-Pin)

$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

$= 1.52 + 0.8 + 0.3 + 1.6 = 4.2$ ns

*EQ 1-18*

*Table 1-17 •* **A54SX08 Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$,$V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| | | '–3' Speed | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | | | | | |
| $t_{HCKH}$ | Input LOW to HIGH (pad to R-Cell input) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | ns |
| $t_{HCKL}$ | Input HIGH to LOW (pad to R-Cell input) | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| $t_{HPWH}$ | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.1 | | 0.2 | | 0.2 | | 0.2 | ns |
| $t_{HP}$ | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input LOW to HIGH (light load) (pad to R-Cell input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (light load) (pad to R-Cell Input) | | 1.4 | | 1.6 | | 1.8 | | 2.1 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 1.5 | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 1.5 | | 1.8 | | 2.0 | | 2.3 | ns |
| $t_{RPWH}$ | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RPWL}$ | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (light load) | | 0.1 | | 0.2 | | 0.2 | | 0.2 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% load) | | 0.3 | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% load) | | 0.3 | | 0.3 | | 0.4 | | 0.4 | ns |
| **TTL Output Module Timing1** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.8 | | 3.2 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

*Table 1-19* • **A54SX16P Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCR}$ = 4.75 V, $V_{CCA}$,$V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| | | '–3' Speed | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | | | | | |
| $t_{HCKH}$ | Input LOW to HIGH (pad to R-Cell input) | | 1.2 | | 1.4 | | 1.5 | | 1.8 | ns |
| $t_{HCKL}$ | Input HIGH to LOW (pad to R-Cell input) | | 1.2 | | 1.4 | | 1.6 | | 1.9 | ns |
| $t_{HPWH}$ | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.2 | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{HP}$ | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input LOW to HIGH (light load) (pad to R-Cell input) | | 1.6 | | 1.8 | | 2.1 | | 2.5 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (Light Load) (pad to R-Cell input) | | 1.8 | | 2.0 | | 2.3 | | 2.7 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 1.8 | | 2.1 | | 2.5 | | 2.8 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 2.0 | | 2.2 | | 2.5 | | 3.0 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 2.0 | | 2.2 | | 2.5 | | 3.0 | ns |
| $t_{RPWH}$ | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RPWL}$ | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (light load) | | 0.5 | | 0.5 | | 0.5 | | 0.7 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% load) | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% load) | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| **TTL Output Module Timing** | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 2.4 | | 2.8 | | 3.1 | | 3.7 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 2.3 | | 2.9 | | 3.2 | | 3.8 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 3.0 | | 3.4 | | 3.9 | | 4.6 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 3.3 | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 2.3 | | 2.7 | | 3.0 | | 3.5 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 10 pF loading.*

| 208-Pin PQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 73 | NC | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | NC | I/O | I/O |
| 76 | PRB, I/O | PRB, I/O | PRB, I/O |
| 77 | GND | GND | GND |
| 78 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 79 | GND | GND | GND |
| 80 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 81 | I/O | I/O | I/O |
| 82 | HCLK | HCLK | HCLK |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | NC | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | NC | I/O | I/O |
| 89 | I/O | I/O | I/O |
| 90 | I/O | I/O | I/O |
| 91 | NC | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | NC | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | NC | I/O | I/O |
| 98 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 99 | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O |
| 103 | TDO, I/O | TDO, I/O | TDO, I/O |
| 104 | I/O | I/O | I/O |
| 105 | GND | GND | GND |
| 106 | NC | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | NC | I/O | I/O |

| 208-Pin PQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 109 | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | NC | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | NC | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | NC | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | NC | I/O | I/O |
| 126 | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | GND | GND | GND |
| 130 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 131 | GND | GND | GND |
| 132 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | NC | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | NC | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O |
| 141 | NC | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | NC | I/O | I/O |
| 144 | I/O | I/O | I/O |

***Note:*** ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | TMS | TMS | TMS |
| 10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 11 | GND | GND | GND |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 20 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 21 | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | GND | GND | GND |
| 29 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 30 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | GND | GND | GND |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 37 | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | PRB, I/O | PRB, I/O | PRB, I/O |
| 55 | I/O | I/O | I/O |
| 56 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 57 | GND | GND | GND |
| 58 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 59 | I/O | I/O | I/O |
| 60 | HCLK | HCLK | HCLK |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 69 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O |
| 71 | TDO, I/O | TDO, I/O | TDO, I/O |
| 72 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 73 | GND | GND | GND |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 80 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 81 | GND | GND | GND |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 90 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 99 | GND | GND | GND |
| 100 | I/O | I/O | I/O |
| 101 | GND | GND | GND |
| 102 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 109 | GND | GND | GND |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | CLKA | CLKA | CLKA |
| 126 | CLKB | CLKB | CLKB |
| 127 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 128 | GND | GND | GND |
| 129 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 130 | I/O | I/O | I/O |
| 131 | PRA, I/O | PRA, I/O | PRA, I/O |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | TCK, I/O | TCK, I/O | TCK, I/O |

# 176-Pin TQFP

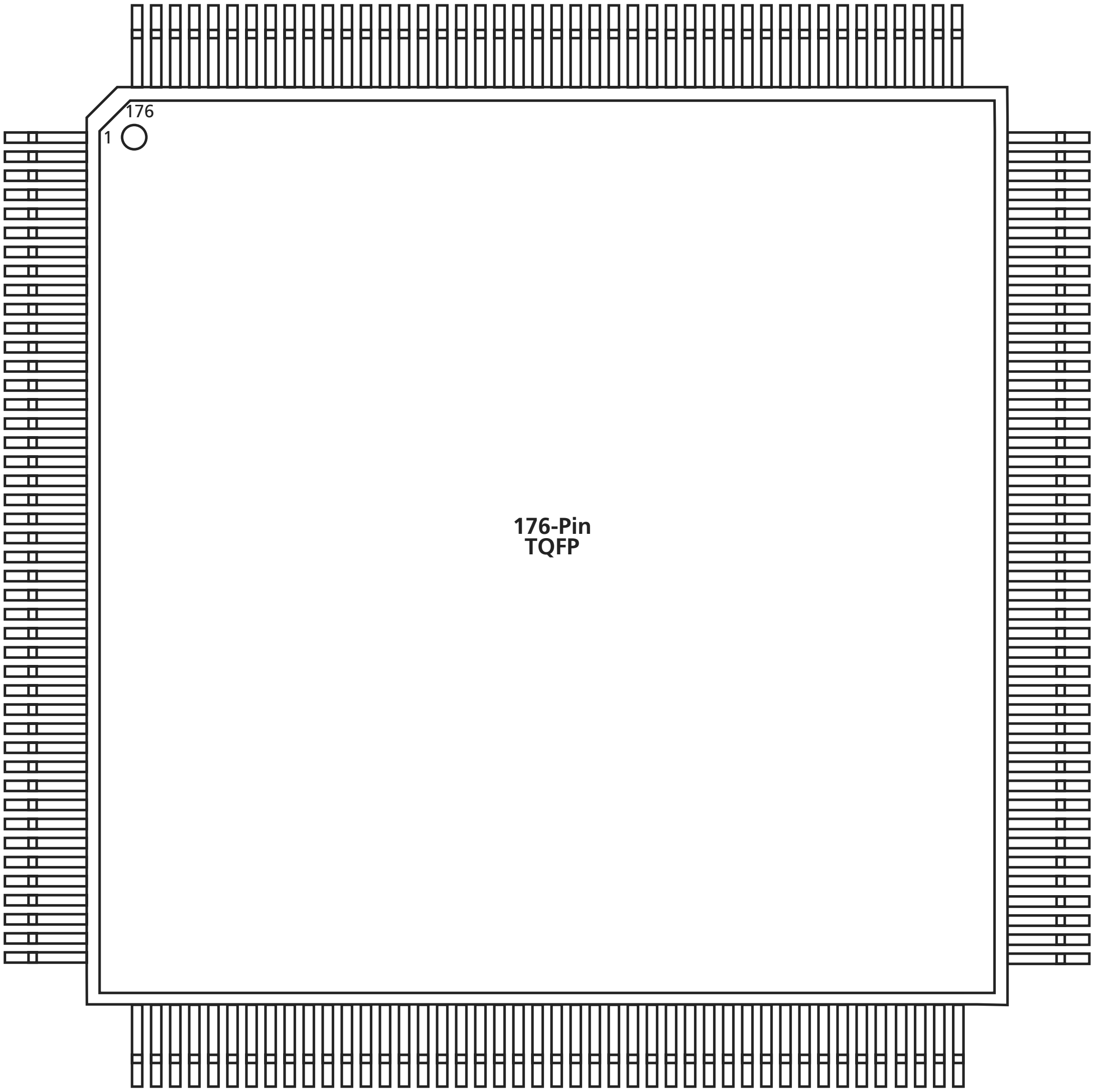



*Figure 2-4* • **176-Pin TQFP (Top View)**

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 313-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| A1 | GND |
| A3 | NC |
| A5 | I/O |
| A7 | I/O |
| A9 | I/O |
| A11 | I/O |
| A13 | $V_{CCR}$ |
| A15 | I/O |
| A17 | I/O |
| A19 | I/O |
| A21 | I/O |
| A23 | NC |
| A25 | GND |
| AA1 | I/O |
| AA3 | I/O |
| AA5 | NC |
| AA7 | I/O |
| AA9 | NC |
| AA11 | I/O |
| AA13 | I/O |
| AA15 | I/O |
| AA17 | I/O |
| AA19 | I/O |
| AA21 | I/O |
| AA23 | NC |
| AA25 | I/O |
| AB2 | NC |
| AB4 | NC |
| AB6 | I/O |
| AB8 | I/O |
| AB10 | I/O |
| AB12 | I/O |
| AB14 | I/O |
| AB16 | I/O |
| AB18 | $V_{CCI}$ |
| AB20 | NC |
| AB22 | I/O |
| AB24 | I/O |
| AC1 | I/O |
| AC3 | I/O |

| 313-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| AC5 | I/O |
| AC7 | I/O |
| AC9 | I/O |
| AC11 | I/O |
| AC13 | $V_{CCR}$ |
| AC15 | I/O |
| AC17 | I/O |
| AC19 | I/O |
| AC21 | I/O |
| AC23 | I/O |
| AC25 | NC |
| AD2 | GND |
| AD4 | I/O |
| AD6 | $V_{CCI}$ |
| AD8 | I/O |
| AD10 | I/O |
| AD12 | PRB, I/O |
| AD14 | I/O |
| AD16 | I/O |
| AD18 | I/O |
| AD20 | I/O |
| AD22 | NC |
| AD24 | I/O |
| AE1 | NC |
| AE3 | I/O |
| AE5 | I/O |
| AE7 | I/O |
| AE9 | I/O |
| AE11 | I/O |
| AE13 | $V_{CCA}$ |
| AE15 | I/O |
| AE17 | I/O |
| AE19 | I/O |
| AE21 | I/O |
| AE23 | TDO, I/O |
| AE25 | GND |
| B2 | TCK, I/O |
| B4 | I/O |
| B6 | I/O |
| B8 | I/O |

| 313-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| B10 | I/O |
| B12 | I/O |
| B14 | I/O |
| B16 | I/O |
| B18 | I/O |
| B20 | I/O |
| B22 | I/O |
| B24 | I/O |
| C1 | TDI, I/O |
| C3 | I/O |
| C5 | NC |
| C7 | I/O |
| C9 | I/O |
| C11 | I/O |
| C13 | $V_{CCI}$ |
| C15 | I/O |
| C17 | I/O |
| C19 | $V_{CCI}$ |
| C21 | I/O |
| C23 | I/O |
| C25 | NC |
| D2 | I/O |
| D4 | NC |
| D6 | I/O |
| D8 | I/O |
| D10 | I/O |
| D12 | I/O |
| D14 | I/O |
| D16 | I/O |
| D18 | I/O |
| D20 | I/O |
| D22 | I/O |
| D24 | NC |
| E1 | I/O |
| E3 | NC |
| E5 | I/O |
| E7 | I/O |
| E9 | I/O |
| E11 | I/O |
| E13 | $V_{CCA}$ |

| 313-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| E15 | I/O |
| E17 | I/O |
| E19 | I/O |
| E21 | I/O |
| E23 | I/O |
| E25 | I/O |
| F2 | I/O |
| F4 | I/O |
| F6 | NC |
| F8 | I/O |
| F10 | NC |
| F12 | I/O |
| F14 | I/O |
| F16 | NC |
| F18 | I/O |
| F20 | I/O |
| F22 | I/O |
| F24 | I/O |
| G1 | I/O |
| G3 | TMS |
| G5 | I/O |
| G7 | I/O |
| G9 | $V_{CCI}$ |
| G11 | I/O |
| G13 | CLKB |
| G15 | I/O |
| G17 | I/O |
| G19 | I/O |
| G21 | I/O |
| G23 | I/O |
| G25 | I/O |
| H2 | I/O |
| H4 | I/O |
| H6 | I/O |
| H8 | I/O |
| H10 | I/O |
| H12 | PRA, I/O |
| H14 | I/O |
| H16 | I/O |
| H18 | NC |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| D3 | I/O |
| D4 | TCK, I/O |
| D5 | I/O |
| D6 | I/O |
| D7 | I/O |
| D8 | I/O |
| D9 | I/O |
| D10 | I/O |
| D11 | $V_{CCA}$ |
| D12 | $V_{CCR}$ |
| D13 | I/O |
| D14 | I/O |
| D15 | I/O |
| D16 | I/O |
| D17 | I/O |
| D18 | I/O |
| D19 | I/O |
| D20 | I/O |
| D21 | I/O |
| D22 | I/O |
| D23 | I/O |
| E1 | $V_{CCI}$ |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E20 | I/O |
| E21 | I/O |
| E22 | I/O |
| E23 | I/O |
| F1 | I/O |
| F2 | TMS |
| F3 | I/O |
| F4 | I/O |
| F20 | I/O |
| F21 | I/O |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| F22 | I/O |
| F23 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | I/O |
| G4 | I/O |
| G20 | I/O |
| G21 | I/O |
| G22 | I/O |
| G23 | GND |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H20 | $V_{CCA}$ |
| H21 | I/O |
| H22 | I/O |
| H23 | I/O |
| J1 | NC |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J20 | I/O |
| J21 | I/O |
| J22 | I/O |
| J23 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | GND |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| K20 | I/O |
| K21 | I/O |
| K22 | I/O |
| K23 | I/O |
| L1 | I/O |
| L2 | I/O |
| L3 | I/O |
| L4 | $V_{CCR}$ |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | GND |
| L20 | $V_{CCR}$ |
| L21 | I/O |
| L22 | I/O |
| L23 | NC |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | $V_{CCA}$ |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M20 | $V_{CCA}$ |
| M21 | I/O |
| M22 | I/O |
| M23 | $V_{CCI}$ |
| N1 | I/O |
| N2 | I/O |
| N3 | I/O |
| N4 | I/O |
| N10 | GND |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N20 | NC |
| N21 | I/O |
| N22 | I/O |
| N23 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | I/O |
| P10 | GND |
| P11 | GND |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P20 | I/O |
| P21 | I/O |
| P22 | I/O |
| P23 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | I/O |
| R20 | I/O |
| R21 | I/O |
| R22 | I/O |
| R23 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T20 | I/O |
| T21 | I/O |

# 144-Pin FBGA

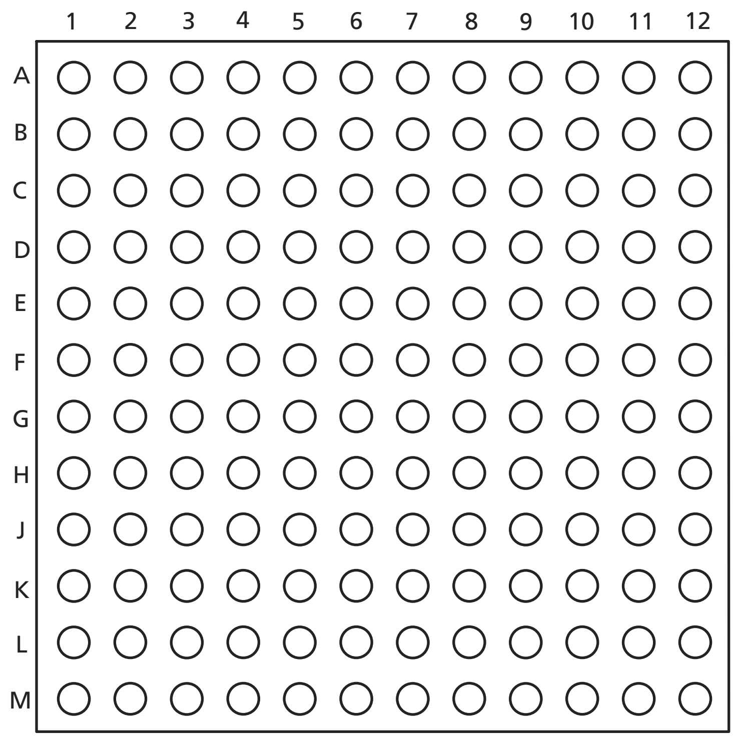



*Figure 2-8* • **144-Pin FBGA (Top View)**

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v3.2) | Page |
|---|---|---|
| v3.1 (June 2003) | The "Ordering Information" was updated to include RoHS information. | 1-ii |
| | The Product Plan was removed since all products have been released. | N/A |
| | Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed. | 1-6 |
| | The "Dedicated Test Mode" section is new. | 1-6 |
| | The "Programming" section is new. | 1-7 |
| | A note was added to the "Power-Up Sequencing" table. | 1-15 |
| | A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A54SX08, A54SX16, A54SX32. | 1-15 |
| | U11 and U13 were added to the "313-Pin PBGA" table. | 2-17 |
| v3.0.1 | Storage temperature in Table 1-3 was updated. | 1-7 |
| | Table 1-1 was updated. | 1-5 |

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Unmarked (production)

This datasheet version contains information that is considered to be final.

### Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

## International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

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