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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 768 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 111 |
| Number of Gates | 12000 |
| Voltage - Supply | 3V ~ 3.6V, 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-FPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a54sx08-1fg144i |

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

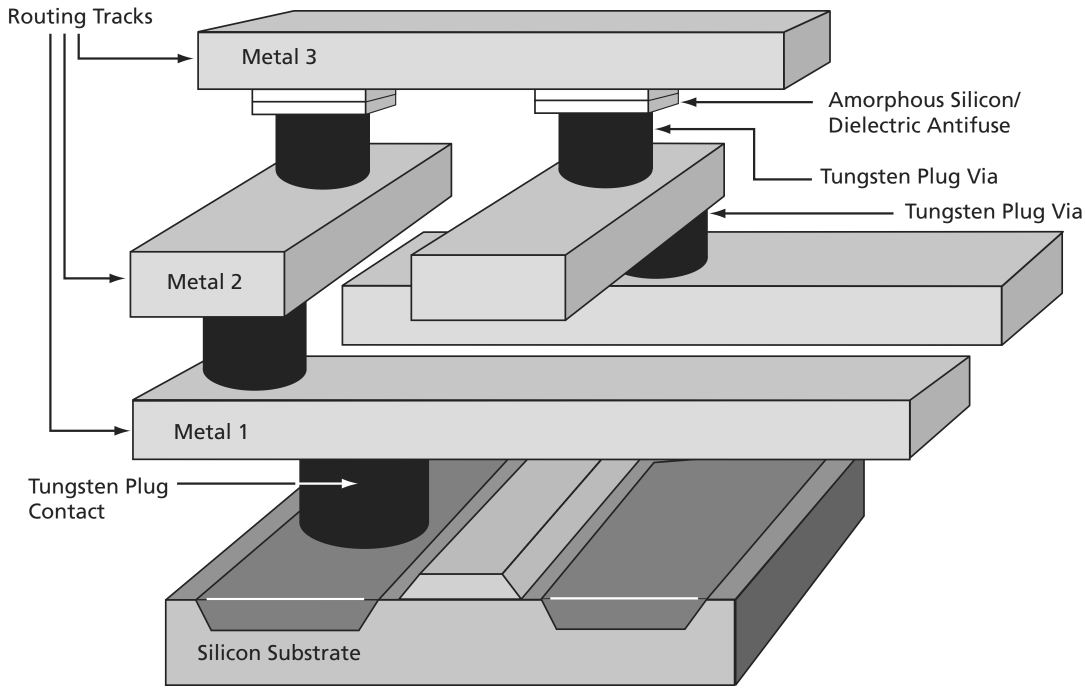



*Figure 1-1* • **SX Family Interconnect Elements**

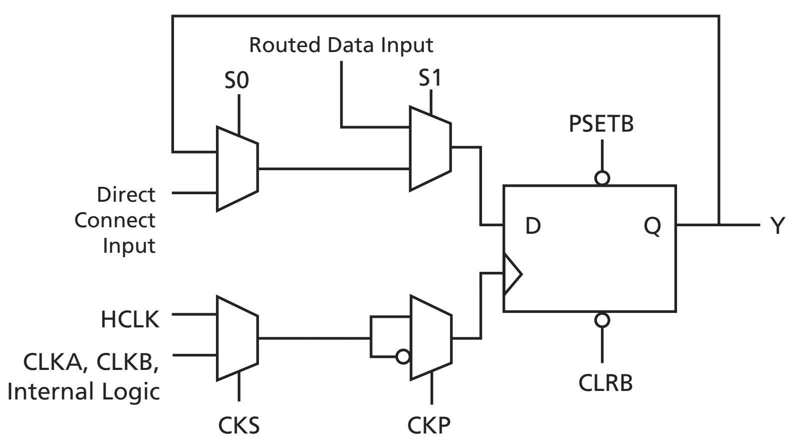



*Figure 1-2* • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

## Chip Architecture

The SX family chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

## Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *clusters*. There are two types of *clusters*: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 1-4). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

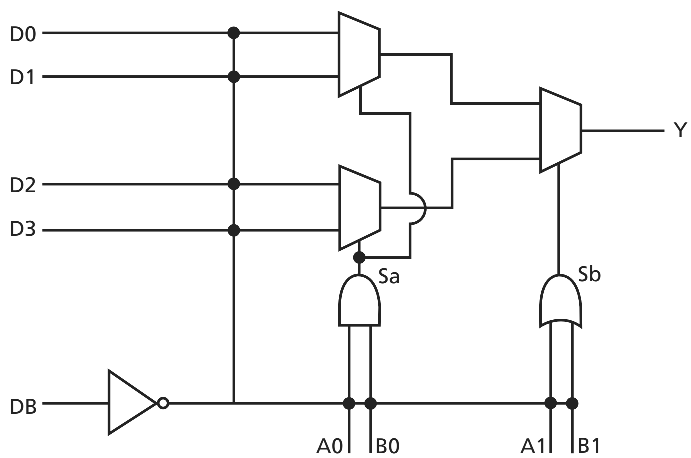



*Figure 1-3* • **C-Cell**

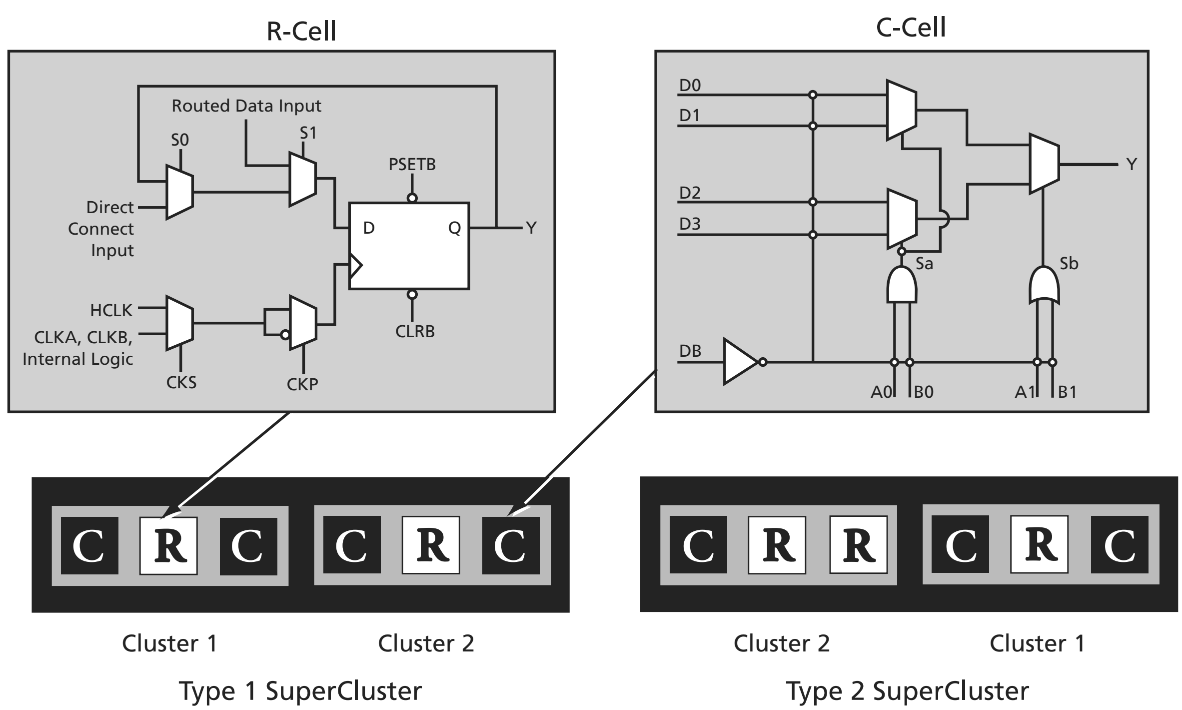



*Figure 1-4* • **Cluster Organization**

## Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

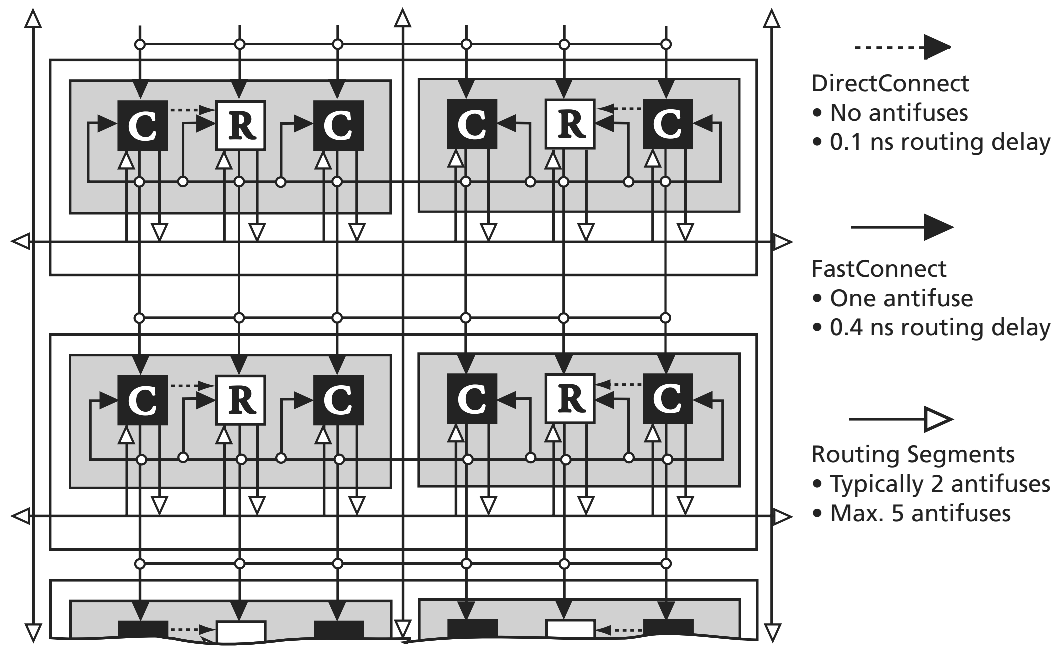



*Figure 1-5* • **DirectConnect and FastConnect for Type 1 SuperClusters**

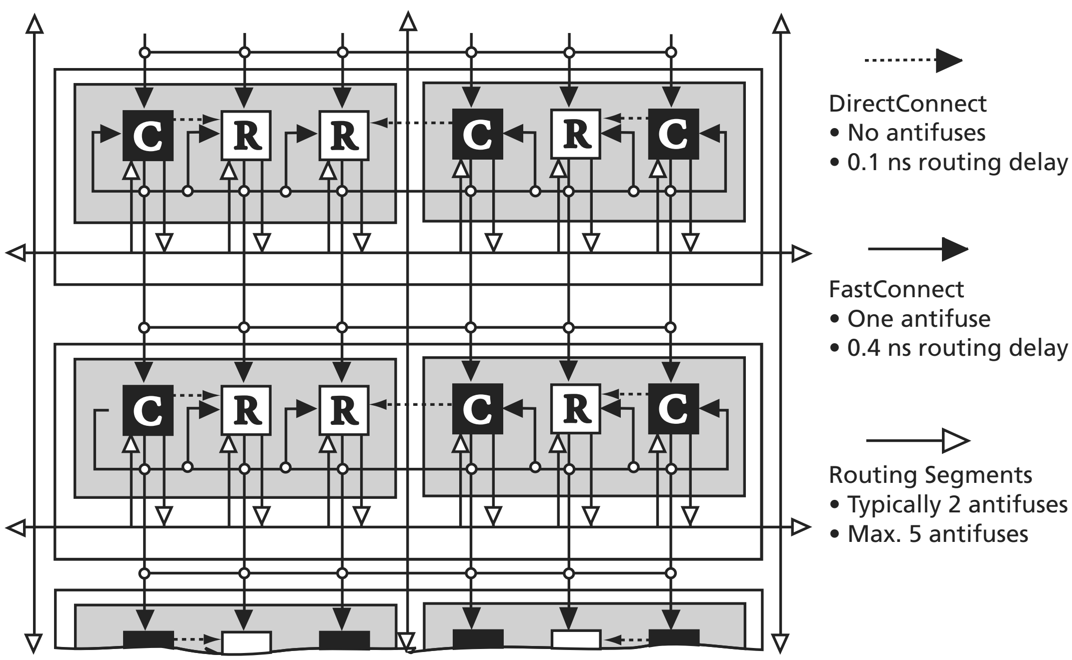



*Figure 1-6* • **DirectConnect and FastConnect for Type 2 SuperClusters**

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

## Other Architectural Features

### Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35 μ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with a capacitance of 1.0 fF for low signal impedance.

### Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

### I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

### Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

*Table 1-1* • **Supply Voltages**

| Device | $V_{CCA}$ | $V_{CCI}$ | $V_{CCR}$ | Maximum Input Tolerance | Maximum Output Drive |
|---|---|---|---|---|---|
| A54SX08<br>A54SX16<br>A54SX32 | 3.3 V | 3.3 V | 5.0 V | 5.0 V | 3.3 V |
| A54SX16-P* | 3.3 V | 3.3 V | 3.3 V | 3.3 V | 3.3 V |
| | 3.3 V | 3.3 V | 5.0 V | 5.0 V | 3.3 V |
| | 3.3 V | 5.0 V | 5.0 V | 5.0 V | 5.0 V |

***Note:*** **A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.*

## Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 1-2. In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

*Table 1-2* • **Boundary Scan Pin Functionality**

| **Program Fuse Blown (Dedicated Test Mode)** | **Program Fuse Not Blown (Flexible Mode)** |
|---|---|
| TCK, TDI, TDO are dedicated BST pins. | TCK, TDI, TDO are flexible and may be used as I/Os. |
| No need for pull-up resistor for TMS | Use a pull-up resistor of 10 kΩ on TMS. |

## Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-7). JTAG pins comply with LVTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the Table 1-5 on page 1-8 for detailed specifications.

*Figure 1-7* • **Device Selection Wizard**

## Development Tool Support

The SX family of FPGAs is fully supported by both the Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the Libero IDE flow diagram (located on the Actel website) for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators, and the simulation results can be cross-probed with Silicon Explorer II, Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys®, and Cadence® Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

## Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-8 on page 1-7 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

## Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

# Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

## Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC}$$

*EQ 1-5*

## DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

*Table 1-12* • **Standby Power**

| $I_{CC}$ | $V_{CC}$ | Power |
|---|---|---|
| 4 mA | 3.6 V | 14.4 mW |

The DC power dissipation is defined in EQ 1-6.

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + xV_{OL} \times I_{OL} + y(V_{CCI} - V_{OH}) \times V_{OH}$$

*EQ 1-6*

## AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

*EQ 1-7*

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5 \times (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5 \times (q2 \times CEQCR \times f_{q2}) + (r2 \times f_{q2}))RCLKB + (0.5 \times (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

*EQ 1-8*

### Definition of Terms Used in Formula

| | | |
|---|---|---|
| $m$ | = | Number of logic modules switching at $f_m$ |
| $n$ | = | Number of input buffers switching at $f_n$ |
| $p$ | = | Number of output buffers switching at $f_p$ |
| $q_1$ | = | Number of clock loads on the first routed array clock |
| $q_2$ | = | Number of clock loads on the second routed array clock |
| $x$ | = | Number of I/Os at logic low |
| $y$ | = | Number of I/Os at logic high |
| $r_1$ | = | Fixed capacitance due to first routed array clock |
| $r_2$ | = | Fixed capacitance due to second routed array clock |
| $s_1$ | = | Number of clock loads on the dedicated array clock |
| $C_{EQM}$ | = | Equivalent capacitance of logic modules in pF |
| $C_{EQI}$ | = | Equivalent capacitance of input buffers in pF |
| $C_{EQO}$ | = | Equivalent capacitance of output buffers in pF |
| $C_{EQCR}$ | = | Equivalent capacitance of routed array clock in pF |
| $C_{EQHV}$ | = | Variable capacitance of dedicated array clock |
| $C_{EQHF}$ | = | Fixed capacitance of dedicated array clock |
| $C_L$ | = | Output lead capacitance in pF |
| $f_m$ | = | Average logic module switching rate in MHz |
| $f_n$ | = | Average input buffer switching rate in MHz |
| $f_p$ | = | Average output buffer switching rate in MHz |
| $f_{q1}$ | = | Average first routed array clock rate in MHz |
| $f_{q2}$ | = | Average second routed array clock rate in MHz |
| $f_{s1}$ | = | Average dedicated array clock rate in MHz |

Table 1-13 shows capacitance values for various devices.

*Table 1-13* • **Capacitance Values for Devices**

| | A54SX08 | A54SX16 | A54SX16P | A54SX32 |
|---|---|---|---|---|
| $C_{EQM}$ (pF) | 4.0 | 4.0 | 4.0 | 4.0 |
| $C_{EQI}$ (pF) | 3.4 | 3.4 | 3.4 | 3.4 |
| $C_{EQO}$ (pF) | 4.7 | 4.7 | 4.7 | 4.7 |
| $C_{EQCR}$ (pF) | 1.6 | 1.6 | 1.6 | 1.6 |
| $C_{EQHV}$ | 0.615 | 0.615 | 0.615 | 0.615 |
| $C_{EQHF}$ | 60 | 96 | 96 | 140 |
| $r_1$ (pF) | 87 | 138 | 138 | 171 |
| $r_2$ (pF) | 87 | 138 | 138 | 171 |

## Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

## Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A54SX16P device. A pattern of 0101… was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101… caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

*Table 1-14* • **Power Consumption Guidelines**

| Description | Power Consumption Guideline |
|---|---|
| Logic Modules (m) | 20% of modules |
| Inputs Switching (n) | # inputs/4 |
| Outputs Switching (p) | # outputs/4 |
| First Routed Array Clock Loads ($q_1$) | 20% of register cells |
| Second Routed Array Clock Loads ($q_2$) | 20% of register cells |
| Load Capacitance ($C_L$) | 35 pF |
| Average Logic Module Switching Rate ($f_m$) | f/10 |
| Average Input Switching Rate ($f_n$) | f/5 |
| Average Output Switching Rate ($f_p$) | f/10 |
| Average First Routed Array Clock Rate ($f_{q1}$) | f/2 |
| Average Second Routed Array Clock Rate ($f_{q2}$) | f/2 |
| Average Dedicated Array Clock Rate ($f_{s1}$) | f |
| Dedicated Clock Array Clock Loads ($s_1$) | 20% of regular modules |

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{Total} = P_{AC} \text{ (dynamic power)} + P_{DC} \text{ (static power)}$$

*EQ 1-9*

## AC Power Dissipation

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

*EQ 1-10*

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5\ (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5\ (q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2}))_{RCLKB} + (0.5\ (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

*EQ 1-11*

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

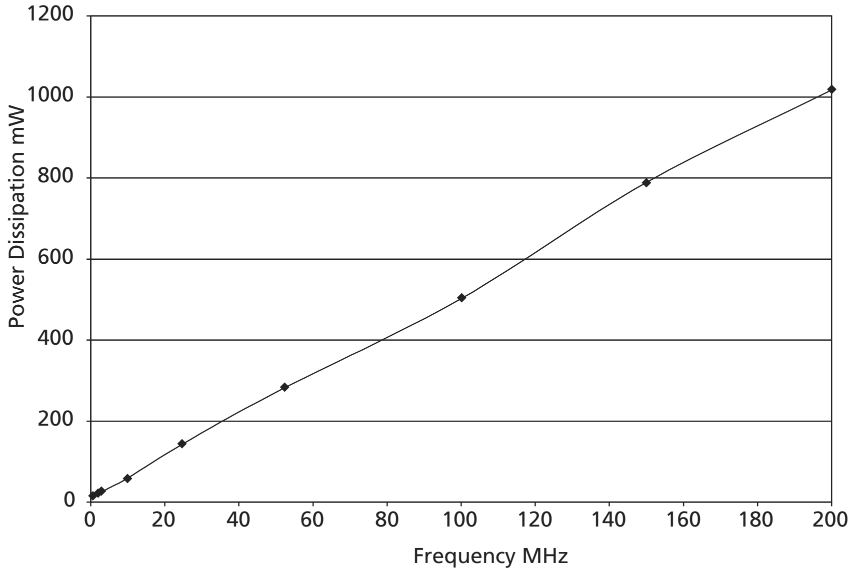



*Figure 1-11* • **Power Dissipation**

## Junction Temperature ($T_J$)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

*EQ 1-13*

Where:

$T_a$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} \times P$

P = Power calculated from Estimating Power Consumption section

$\theta_{ja}$ = Junction to ambient of package. $\theta_{ja}$ numbers are located in the "Package Thermal Characteristics" section.

## Package Thermal Characteristics

The device junction to case thermal characteristic is $\theta_{jc}$, and the junction to ambient air characteristic is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown with two different air flow rates.

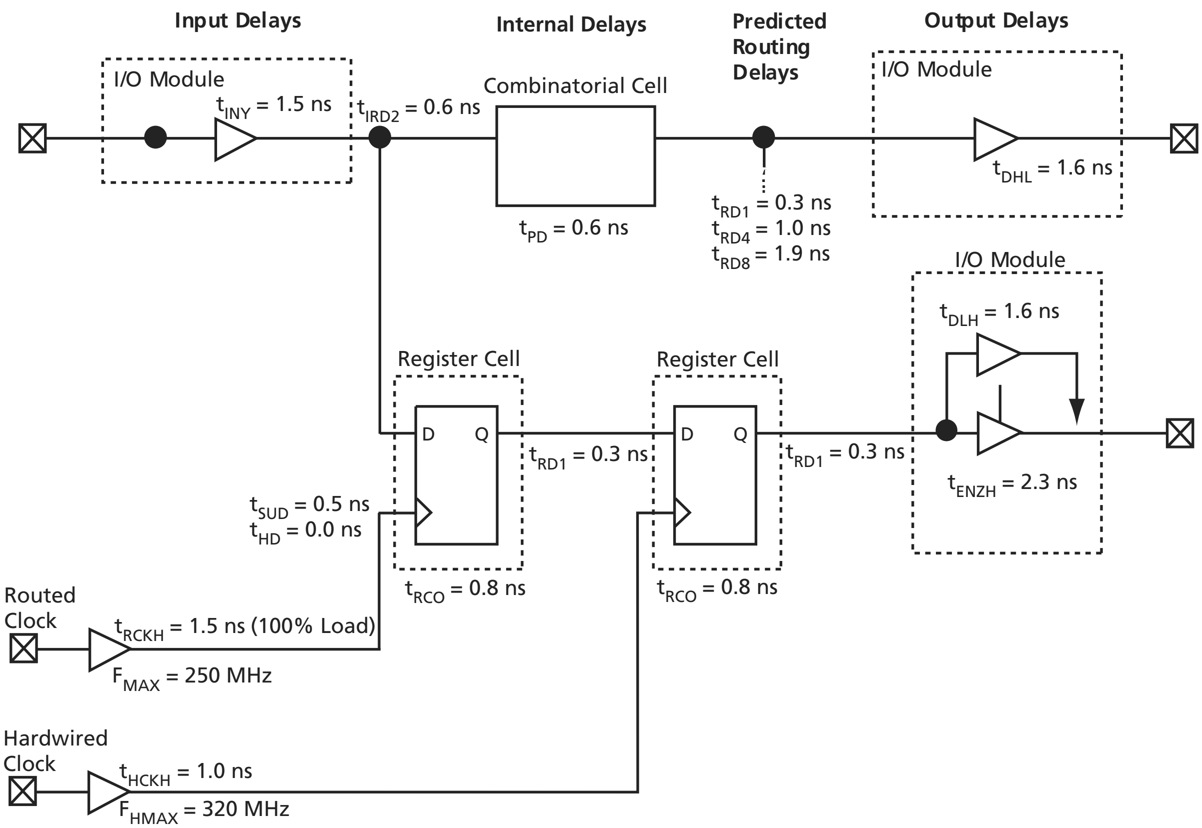
The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\ \text{(°C/W)}} = \frac{150°C - 70°C}{28°C/W} = 2.86\ W$$

*EQ 1-14*

# SX Timing Model




***Note:*** *Values shown for A54SX08-3, worst-case commercial conditions.*

*Figure 1-12* • **SX Timing Model**

### Hardwired Clock

External Setup $= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH}$

$= 1.5 + 0.3 + 0.5 - 1.0 = 1.3$ ns

*EQ 1-15*

Clock-to-Out (Pin-to-Pin)

$= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

$= 1.0 + 0.8 + 0.3 + 1.6 = 3.7$ ns

*EQ 1-16*

### Routed Clock

External Setup $= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$

$= 1.5 + 0.3 + 0.5 - 1.5 = 0.8$ ns

*EQ 1-17*

Clock-to-Out (Pin-to-Pin)

$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

$= 1.52 + 0.8 + 0.3 + 1.6 = 4.2$ ns

*EQ 1-18*

## Register Cell Timing Characteristics

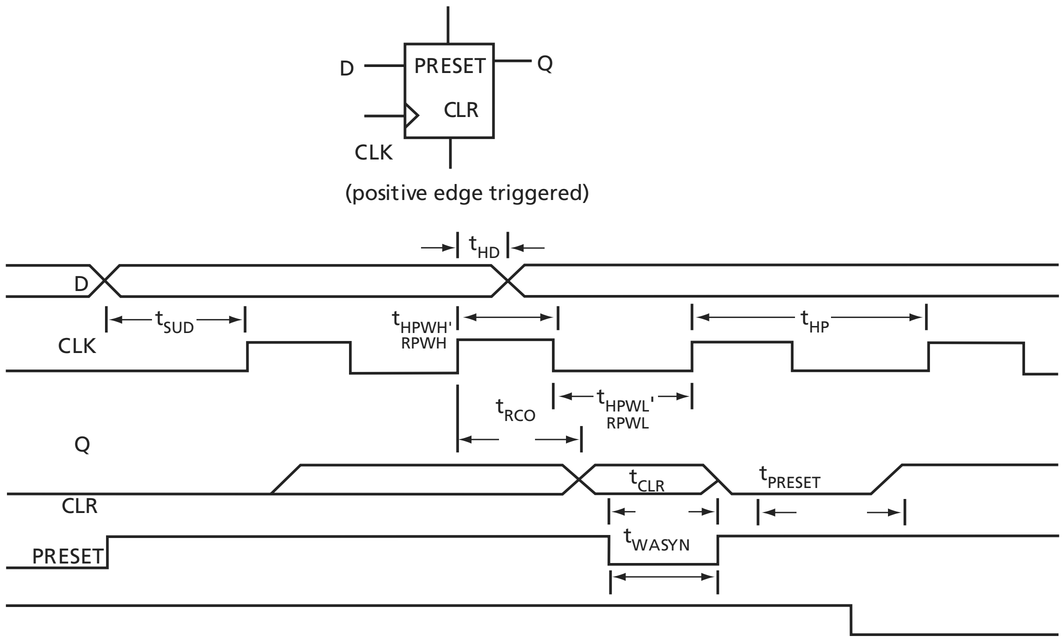



*Figure 1-17* • **Flip-Flops**

# Timing Characteristics

Timing characteristics for SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

## Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

## Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO = 24) routing delays in the datasheet specifications section.

## Timing Derating

SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

*Table 1-20* • **A54SX32 Timing Characteristics (Continued)**
**(Worst-Case Commercial Conditions, $V_{CCR}$= 4.75 V, $V_{CCA}$,$V_{CCI}$ = 3.0 V, $T_J$ = 70°C)**

| | | '–3' Speed | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | | | | | |
| $t_{HCKH}$ | Input LOW to HIGH (pad to R-Cell input) | | 1.9 | | 2.1 | | 2.4 | | 2.8 | ns |
| $t_{HCKL}$ | Input HIGH to LOW (pad to R-Cell input) | | 1.9 | | 2.1 | | 2.4 | | 2.8 | ns |
| $t_{HPWH}$ | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{HP}$ | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | |
| $t_{RCKH}$ | Input LOW to HIGH (light load) (pad to R-Cell input) | | 2.4 | | 2.7 | | 3.0 | | 3.5 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (light load) (pad to R-Cell input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 2.7 | | 3.0 | | 3.5 | | 4.1 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 2.7 | | 3.1 | | 3.6 | | 4.2 | ns |
| $t_{RCKH}$ | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 2.7 | | 3.1 | | 3.5 | | 4.1 | ns |
| $t_{RCKL}$ | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 2.8 | | 3.2 | | 3.6 | | 4.3 | ns |
| $t_{RPWH}$ | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RPWL}$ | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (light load) | | 0.85 | | 0.98 | | 1.1 | | 1.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% load) | | 1.23 | | 1.4 | | 1.6 | | 1.9 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% load) | | 1.30 | | 1.5 | | 1.7 | | 2.0 | ns |
| **TTL Output Module Timing**[3] | | | | | | | | | | |
| $t_{DLH}$ | Data-to-Pad LOW to HIGH | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{DHL}$ | Data-to-Pad HIGH to LOW | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.8 | | 3.2 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 1.3 | | 1.5 | | 1.7 | | 2.0 | ns |

***Note:***

1. *For dual-module macros, use $t_{PD}$ + $t_{RD1}$ + $t_{PDn}$, $t_{RCO}$ + $t_{RD1}$ + $t_{PDn}$, or $t_{PD1}$ + $t_{RD1}$ + $t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except $t_{ENZL}$ and $t_{ENZH}$. For $t_{ENZL}$ and $t_{ENZH}$ the loading is 5 pF.*

## Pin Description

**CLKA/B** **Clock A and B**

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

**GND** **Ground**

LOW supply voltage.

**HCLK** **Dedicated (hardwired) Array Clock**

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

**I/O** **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

**NC** **No Connection**

This pin is not connected to circuitry within the device.

**PRA, I/O** **Probe A**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**PRB, I/O** **Probe B**

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**TCK** **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDI** **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDO** **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-6). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TMS** **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-6). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

**$V_{CCI}$** **Supply Voltage**

Supply voltage for I/Os. See Table 1-1 on page 1-5.

**$V_{CCA}$** **Supply Voltage**

Supply voltage for Array. See Table 1-1 on page 1-5.

**$V_{CCR}$** **Supply Voltage**

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-5.

| 84-Pin PLCC | |
|---|---|
| Pin Number | A54SX08 Function |
| 1 | $V_{CCR}$ |
| 2 | GND |
| 3 | $V_{CCA}$ |
| 4 | PRA, I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | $V_{CCI}$ |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | TCK, I/O |
| 12 | TDI, I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | TMS |
| 17 | I/O |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | I/O |
| 22 | I/O |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | I/O |
| 27 | GND |
| 28 | $V_{CCI}$ |
| 29 | I/O |
| 30 | I/O |
| 31 | I/O |
| 32 | I/O |
| 33 | I/O |
| 34 | I/O |
| 35 | I/O |
| 36 | I/O |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | PRB, I/O |
| 41 | $V_{CCA}$ |
| 42 | GND |
| 43 | $V_{CCR}$ |
| 44 | I/O |
| 45 | HCLK |
| 46 | I/O |
| 47 | I/O |
| 48 | I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | TDO, I/O |
| 53 | I/O |
| 54 | I/O |
| 55 | I/O |
| 56 | I/O |
| 57 | I/O |
| 58 | I/O |
| 59 | $V_{CCA}$ |
| 60 | $V_{CCI}$ |
| 61 | GND |
| 62 | I/O |
| 63 | I/O |
| 64 | I/O |
| 65 | I/O |
| 66 | I/O |
| 67 | I/O |
| 68 | $V_{CCA}$ |
| 69 | GND |
| 70 | I/O |
| 71 | I/O |
| 72 | I/O |
| 73 | I/O |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | I/O |
| 79 | I/O |
| 80 | I/O |
| 81 | I/O |
| 82 | I/O |
| 83 | CLKA |
| 84 | CLKB |

| 208-Pin PQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 145 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 146 | GND | GND | GND |
| 147 | I/O | I/O | I/O |
| 148 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | I/O |
| 151 | I/O | I/O | I/O |
| 152 | I/O | I/O | I/O |
| 153 | I/O | I/O | I/O |
| 154 | I/O | I/O | I/O |
| 155 | NC | I/O | I/O |
| 156 | NC | I/O | I/O |
| 157 | GND | GND | GND |
| 158 | I/O | I/O | I/O |
| 159 | I/O | I/O | I/O |
| 160 | I/O | I/O | I/O |
| 161 | I/O | I/O | I/O |
| 162 | I/O | I/O | I/O |
| 163 | I/O | I/O | I/O |
| 164 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 165 | I/O | I/O | I/O |
| 166 | I/O | I/O | I/O |
| 167 | NC | I/O | I/O |
| 168 | I/O | I/O | I/O |
| 169 | I/O | I/O | I/O |
| 170 | NC | I/O | I/O |
| 171 | I/O | I/O | I/O |
| 172 | I/O | I/O | I/O |
| 173 | NC | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O |
| 176 | NC | I/O | I/O |
| 177 | I/O | I/O | I/O |
| 178 | I/O | I/O | I/O |
| 179 | I/O | I/O | I/O |
| 180 | CLKA | CLKA | CLKA |

| 208-Pin PQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 181 | CLKB | CLKB | CLKB |
| 182 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 183 | GND | GND | GND |
| 184 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 185 | GND | GND | GND |
| 186 | PRA, I/O | PRA, I/O | PRA, I/O |
| 187 | I/O | I/O | I/O |
| 188 | I/O | I/O | I/O |
| 189 | NC | I/O | I/O |
| 190 | I/O | I/O | I/O |
| 191 | I/O | I/O | I/O |
| 192 | NC | I/O | I/O |
| 193 | I/O | I/O | I/O |
| 194 | I/O | I/O | I/O |
| 195 | NC | I/O | I/O |
| 196 | I/O | I/O | I/O |
| 197 | I/O | I/O | I/O |
| 198 | NC | I/O | I/O |
| 199 | I/O | I/O | I/O |
| 200 | I/O | I/O | I/O |
| 201 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 202 | NC | I/O | I/O |
| 203 | NC | I/O | I/O |
| 204 | I/O | I/O | I/O |
| 205 | NC | I/O | I/O |
| 206 | I/O | I/O | I/O |
| 207 | I/O | I/O | I/O |
| 208 | TCK, I/O | TCK, I/O | TCK, I/O |

***Note:*** ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | TMS | TMS | TMS |
| 10 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 11 | GND | GND | GND |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 20 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 21 | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | GND | GND | GND |
| 29 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 30 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | GND | GND | GND |

| 144-Pin TQFP | | | |
|---|---|---|---|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 37 | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | PRB, I/O | PRB, I/O | PRB, I/O |
| 55 | I/O | I/O | I/O |
| 56 | $V_{CCA}$ | $V_{CCA}$ | $V_{CCA}$ |
| 57 | GND | GND | GND |
| 58 | $V_{CCR}$ | $V_{CCR}$ | $V_{CCR}$ |
| 59 | I/O | I/O | I/O |
| 60 | HCLK | HCLK | HCLK |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | $V_{CCI}$ | $V_{CCI}$ | $V_{CCI}$ |
| 69 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O |
| 71 | TDO, I/O | TDO, I/O | TDO, I/O |
| 72 | I/O | I/O | I/O |

# 176-Pin TQFP

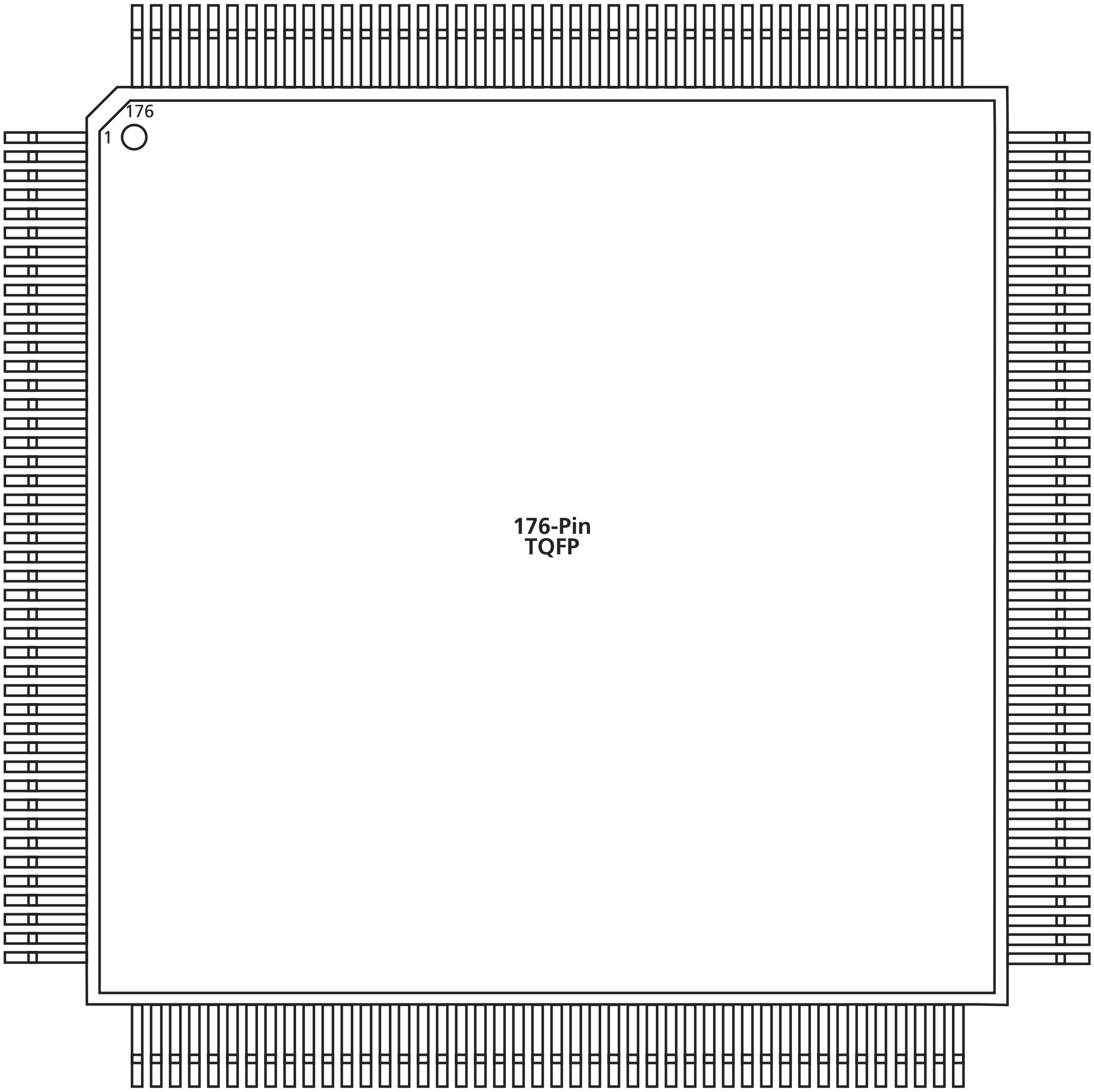



*Figure 2-4* • **176-Pin TQFP (Top View)**

## Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

| 100-Pin VQFP | | |
|---|---|---|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function |
| 1 | GND | GND |
| 2 | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | TMS | TMS |
| 8 | $V_{CCI}$ | $V_{CCI}$ |
| 9 | GND | GND |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | I/O | I/O |
| 15 | I/O | I/O |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | $V_{CCI}$ | $V_{CCI}$ |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | I/O | I/O |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | I/O | I/O |
| 33 | I/O | I/O |
| 34 | PRB, I/O | PRB, I/O |
| 35 | $V_{CCA}$ | $V_{CCA}$ |
| 36 | GND | GND |
| 37 | $V_{CCR}$ | $V_{CCR}$ |
| 38 | I/O | I/O |
| 39 | HCLK | HCLK |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | $V_{CCI}$ | $V_{CCI}$ |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | TDO, I/O | TDO, I/O |
| 50 | I/O | I/O |
| 51 | GND | GND |
| 52 | I/O | I/O |
| 53 | I/O | I/O |
| 54 | I/O | I/O |
| 55 | I/O | I/O |
| 56 | I/O | I/O |
| 57 | $V_{CCA}$ | $V_{CCA}$ |
| 58 | $V_{CCI}$ | $V_{CCI}$ |
| 59 | I/O | I/O |
| 60 | I/O | I/O |
| 61 | I/O | I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | I/O | I/O |
| 66 | I/O | I/O |
| 67 | $V_{CCA}$ | $V_{CCA}$ |
| 68 | GND | GND |
| 69 | GND | GND |
| 70 | I/O | I/O |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | I/O |
| 74 | I/O | I/O |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | I/O | I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |
| 81 | I/O | I/O |
| 82 | $V_{CCI}$ | $V_{CCI}$ |
| 83 | I/O | I/O |
| 84 | I/O | I/O |
| 85 | I/O | I/O |
| 86 | I/O | I/O |
| 87 | CLKA | CLKA |
| 88 | CLKB | CLKB |
| 89 | $V_{CCR}$ | $V_{CCR}$ |
| 90 | $V_{CCA}$ | $V_{CCA}$ |
| 91 | GND | GND |
| 92 | PRA, I/O | PRA, I/O |
| 93 | I/O | I/O |
| 94 | I/O | I/O |
| 95 | I/O | I/O |
| 96 | I/O | I/O |
| 97 | I/O | I/O |
| 98 | I/O | I/O |
| 99 | I/O | I/O |
| 100 | TCK, I/O | TCK, I/O |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| A1 | GND |
| A2 | GND |
| A3 | $V_{CCI}$ |
| A4 | NC |
| A5 | I/O |
| A6 | I/O |
| A7 | $V_{CCI}$ |
| A8 | NC |
| A9 | I/O |
| A10 | I/O |
| A11 | I/O |
| A12 | I/O |
| A13 | CLKB |
| A14 | I/O |
| A15 | I/O |
| A16 | I/O |
| A17 | I/O |
| A18 | I/O |
| A19 | I/O |
| A20 | I/O |
| A21 | NC |
| A22 | $V_{CCI}$ |
| A23 | GND |
| AA1 | $V_{CCI}$ |
| AA2 | I/O |
| AA3 | GND |
| AA4 | I/O |
| AA5 | I/O |
| AA6 | I/O |
| AA7 | I/O |
| AA8 | I/O |
| AA9 | I/O |
| AA10 | I/O |
| AA11 | I/O |
| AA12 | I/O |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| AA13 | I/O |
| AA14 | I/O |
| AA15 | I/O |
| AA16 | I/O |
| AA17 | I/O |
| AA18 | I/O |
| AA19 | I/O |
| AA20 | TDO, I/O |
| AA21 | $V_{CCI}$ |
| AA22 | I/O |
| AA23 | $V_{CCI}$ |
| AB1 | I/O |
| AB2 | GND |
| AB3 | I/O |
| AB4 | I/O |
| AB5 | I/O |
| AB6 | I/O |
| AB7 | I/O |
| AB8 | I/O |
| AB9 | I/O |
| AB10 | I/O |
| AB11 | PRB, I/O |
| AB12 | I/O |
| AB13 | HCLK |
| AB14 | I/O |
| AB15 | I/O |
| AB16 | I/O |
| AB17 | I/O |
| AB18 | I/O |
| AB19 | I/O |
| AB20 | I/O |
| AB21 | I/O |
| AB22 | GND |
| AB23 | I/O |
| AC1 | GND |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| AC2 | $V_{CCI}$ |
| AC3 | NC |
| AC4 | I/O |
| AC5 | I/O |
| AC6 | I/O |
| AC7 | I/O |
| AC8 | I/O |
| AC9 | $V_{CCI}$ |
| AC10 | I/O |
| AC11 | I/O |
| AC12 | I/O |
| AC13 | I/O |
| AC14 | I/O |
| AC15 | NC |
| AC16 | I/O |
| AC17 | I/O |
| AC18 | I/O |
| AC19 | I/O |
| AC20 | I/O |
| AC21 | NC |
| AC22 | $V_{CCI}$ |
| AC23 | GND |
| B1 | $V_{CCI}$ |
| B2 | GND |
| B3 | I/O |
| B4 | I/O |
| B5 | I/O |
| B6 | I/O |
| B7 | I/O |
| B8 | I/O |
| B9 | I/O |
| B10 | I/O |
| B11 | I/O |
| B12 | PRA, I/O |
| B13 | CLKA |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| B14 | I/O |
| B15 | I/O |
| B16 | I/O |
| B17 | I/O |
| B18 | I/O |
| B19 | I/O |
| B20 | I/O |
| B21 | I/O |
| B22 | GND |
| B23 | $V_{CCI}$ |
| C1 | NC |
| C2 | TDI, I/O |
| C3 | GND |
| C4 | I/O |
| C5 | I/O |
| C6 | I/O |
| C7 | I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | I/O |
| C11 | I/O |
| C12 | I/O |
| C13 | I/O |
| C14 | I/O |
| C15 | I/O |
| C16 | I/O |
| C17 | I/O |
| C18 | I/O |
| C19 | I/O |
| C20 | I/O |
| C21 | $V_{CCI}$ |
| C22 | GND |
| C23 | NC |
| D1 | I/O |
| D2 | I/O |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| D3 | I/O |
| D4 | TCK, I/O |
| D5 | I/O |
| D6 | I/O |
| D7 | I/O |
| D8 | I/O |
| D9 | I/O |
| D10 | I/O |
| D11 | $V_{CCA}$ |
| D12 | $V_{CCR}$ |
| D13 | I/O |
| D14 | I/O |
| D15 | I/O |
| D16 | I/O |
| D17 | I/O |
| D18 | I/O |
| D19 | I/O |
| D20 | I/O |
| D21 | I/O |
| D22 | I/O |
| D23 | I/O |
| E1 | $V_{CCI}$ |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E20 | I/O |
| E21 | I/O |
| E22 | I/O |
| E23 | I/O |
| F1 | I/O |
| F2 | TMS |
| F3 | I/O |
| F4 | I/O |
| F20 | I/O |
| F21 | I/O |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| F22 | I/O |
| F23 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | I/O |
| G4 | I/O |
| G20 | I/O |
| G21 | I/O |
| G22 | I/O |
| G23 | GND |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H20 | $V_{CCA}$ |
| H21 | I/O |
| H22 | I/O |
| H23 | I/O |
| J1 | NC |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J20 | I/O |
| J21 | I/O |
| J22 | I/O |
| J23 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | GND |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| K20 | I/O |
| K21 | I/O |
| K22 | I/O |
| K23 | I/O |
| L1 | I/O |
| L2 | I/O |
| L3 | I/O |
| L4 | $V_{CCR}$ |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | GND |
| L20 | $V_{CCR}$ |
| L21 | I/O |
| L22 | I/O |
| L23 | NC |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | $V_{CCA}$ |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M20 | $V_{CCA}$ |
| M21 | I/O |
| M22 | I/O |
| M23 | $V_{CCI}$ |
| N1 | I/O |
| N2 | I/O |
| N3 | I/O |
| N4 | I/O |
| N10 | GND |

| 329-Pin PBGA | |
|---|---|
| Pin Number | A54SX32 Function |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N20 | NC |
| N21 | I/O |
| N22 | I/O |
| N23 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | I/O |
| P10 | GND |
| P11 | GND |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P20 | I/O |
| P21 | I/O |
| P22 | I/O |
| P23 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | I/O |
| R20 | I/O |
| R21 | I/O |
| R22 | I/O |
| R23 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T20 | I/O |
| T21 | I/O |

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