



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

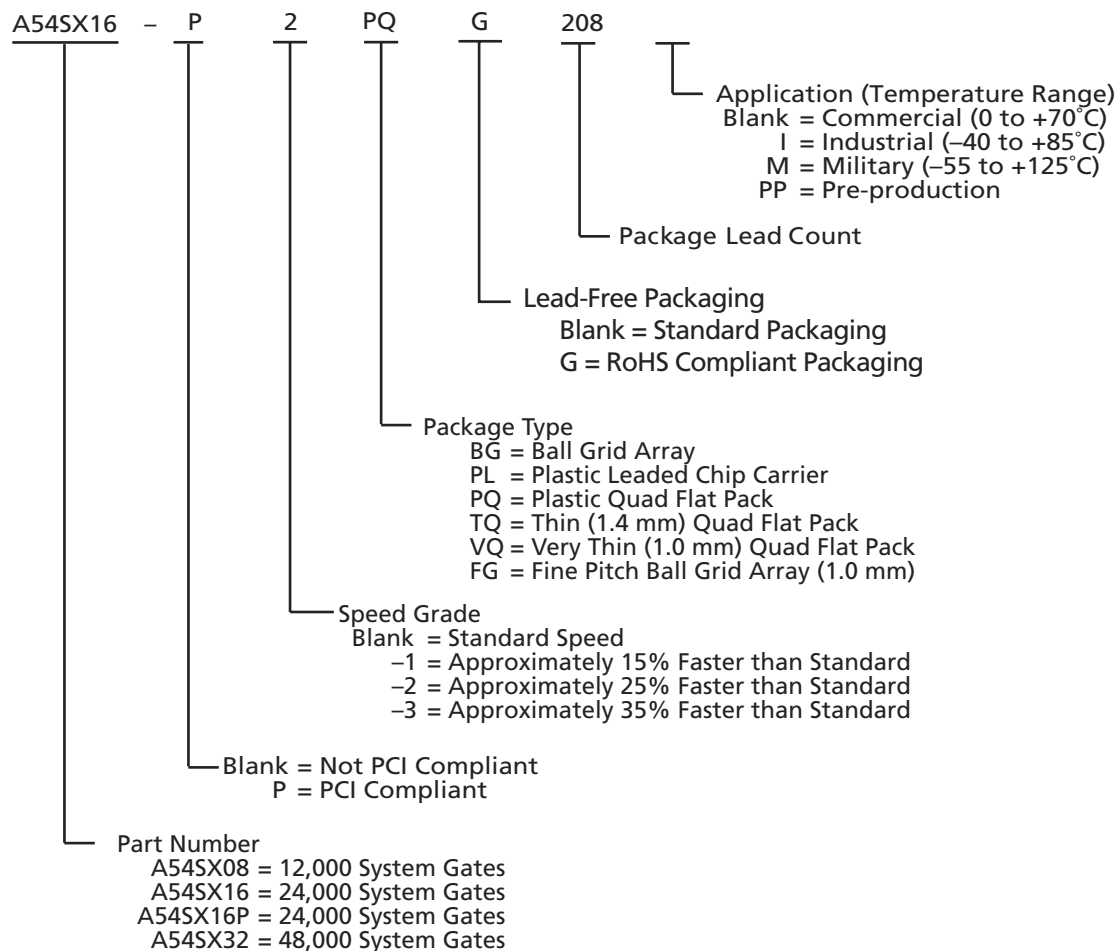
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	111
Number of Gates	12000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a54sx08-1fgg144

Ordering Information



Plastic Device Resources

Device	User I/Os (including clock buffers)							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin	FBGA 144-Pin
A54SX08	69	81	130	113	128	–	–	111
A54SX16	–	81	175	–	147	–	–	–
A54SX16P	–	81	175	113	147	–	–	–
A54SX32	–	–	174	113	147	249	249	–

Note: Package Definitions (Consult your local Actel sales representative for product availability):

PLCC = Plastic Leaded Chip Carrier

PQFP = Plastic Quad Flat Pack

TQFP = Thin Quad Flat Pack

VQFP = Very Thin Quad Flat Pack

PBGA = Plastic Ball Grid Array

FBGA = Fine Pitch (1.0 mm) Ball Grid Array

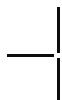


Table of Contents

SX Family FPGAs

General Description 1-1

SX Family Architecture 1-1

Programming 1-7

3.3 V / 5 V Operating Conditions 1-7

PCI Compliance for the SX Family 1-9

A54SX16P AC Specifications for (PCI Operation) 1-10

A54SX16P DC Specifications (3.3 V PCI Operation) 1-12

A54SX16P AC Specifications (3.3 V PCI Operation) 1-13

Power-Up Sequencing 1-15

Power-Down Sequencing 1-15

Evaluating Power in SX Devices 1-16

SX Timing Model 1-21

Timing Characteristics 1-23

Package Pin Assignments

84-Pin PLCC 2-1

208-Pin PQFP 2-3

144-Pin TQFP 2-7

176-Pin TQFP 2-10

100-Pin VQFP 2-14

313-Pin PBGA 2-16

329-Pin PBGA 2-19

144-Pin FBGA 2-23

Datasheet Information

List of Changes 3-1

Datasheet Categories 3-1

International Traffic in Arms Regulations (ITAR) and Export Administration
Regulations (EAR) 3-1

Chip Architecture

The SX family chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *clusters*. There are two types of *clusters*: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 1-4). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature more SuperCluster 1 modules because designers typically require significantly more combinatorial logic than flip-flops.

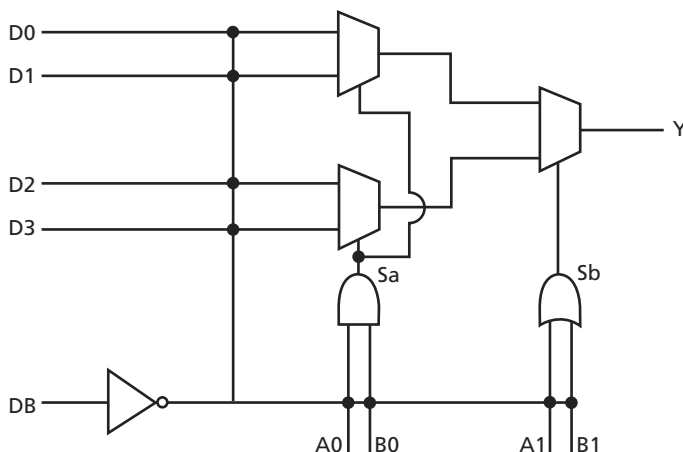


Figure 1-3 • C-Cell

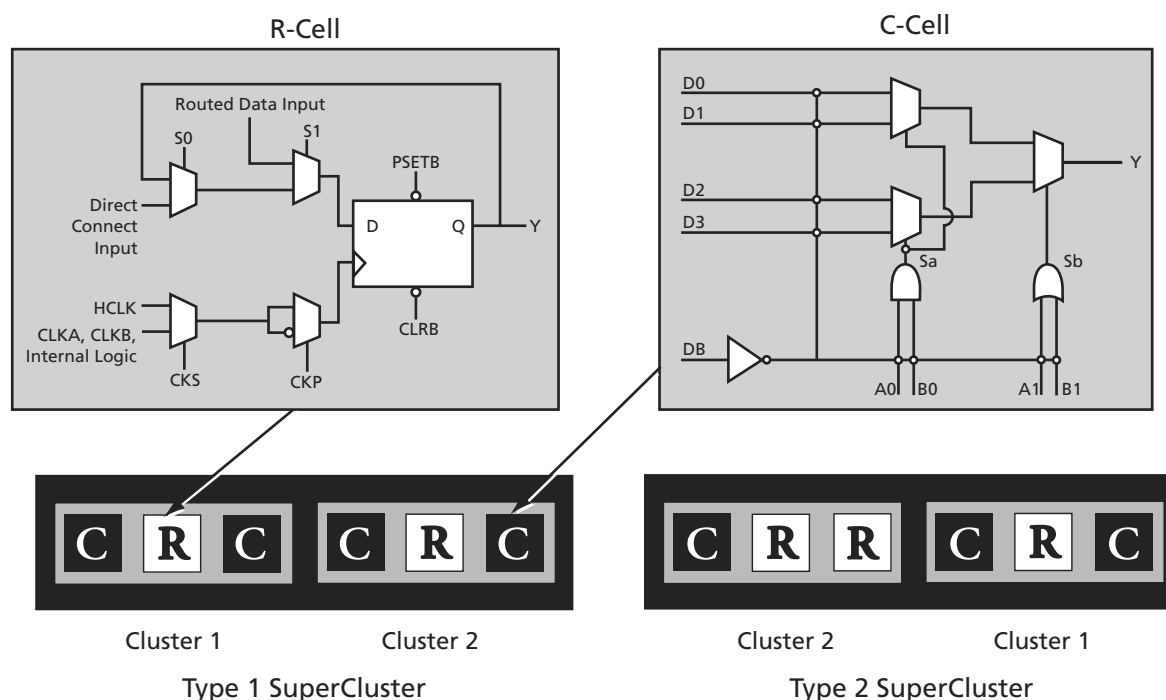


Figure 1-4 • Cluster Organization

Table 1-4 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	%V _{CC}
5.0 V Power Supply Tolerance	±5	±10	±10	%V _{CC}

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Table 1-5 • Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V _{OH}	(I _{OH} = –20 μ A) (CMOS) (I _{OH} = –8 mA) (TTL) (I _{OH} = –6 mA) (TTL)	(V _{CCI} – 0.1) 2.4	V _{CCI} V _{CCI}	(V _{CCI} – 0.1) 2.4	V _{CCI} V _{CCI}	V
V _{OL}	(I _{OL} = 20 μ A) (CMOS) (I _{OL} = 12 mA) (TTL) (I _{OL} = 8 mA) (TTL)		0.10 0.50		0.50	V
V _{IL}			0.8		0.8	V
V _{IH}		2.0		2.0		V
t _R , t _F	Input Transition Time t _R , t _F		50		50	ns
C _{IO}	C _{IO} I/O Capacitance		10		10	pF
I _{CC}	Standby Current, I _{CC}		4.0		4.0	mA
I _{CC(D)}	I _{CC(D)} I _{Dynamic} V _{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

A54SX16P AC Specifications for (PCI Operation)

Table 1-7 • A54SX16P AC Specifications for (PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4^1$	-44		mA
		$1.4 \leq V_{OUT} < 2.4^1, ^2$	$-44 + (V_{OUT} - 1.4)/0.024$		mA
		$3.1 < V_{OUT} < V_{CC}^{1, ^3}$		EQ 1-1 on page 1-11	
	(Test Point)	$V_{OUT} = 3.1^3$		-142	mA
$I_{OL(AC)}$	Switching Current High	$V_{OUT} \geq 2.2^1$	95		mA
		$2.2 > V_{OUT} > 0.55^1$	$V_{OUT}/0.023$		
		$0.71 > V_{OUT} > 0^{1, ^3}$		EQ 1-2 on page 1-11	mA
	(Test Point)	$V_{OUT} = 0.71^3$		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4 V to 2.4 V load ⁴	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4 V to 0.4 V load ⁴	1	5	V/ns

Notes:

1. Refer to the *V_I* curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maxima (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

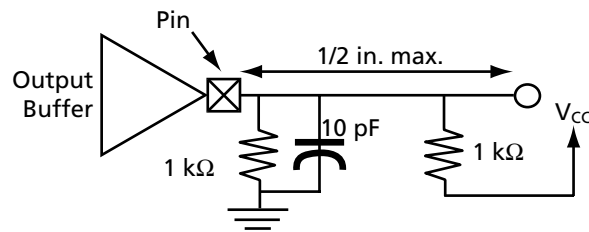


Figure 1-9 shows the 5.0 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

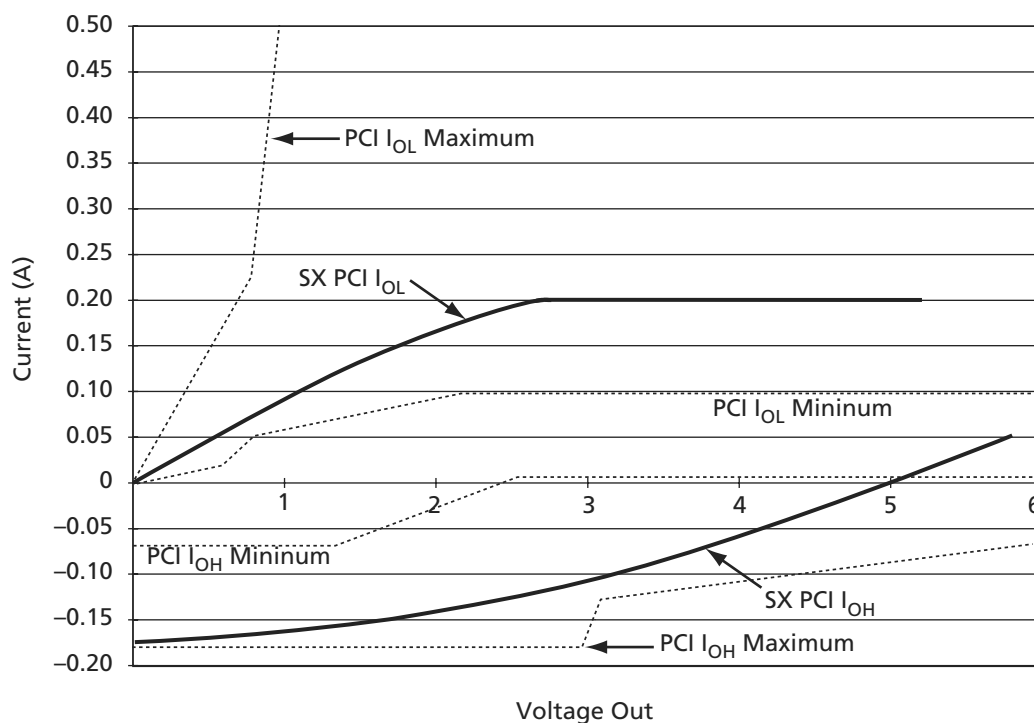


Figure 1-9 • **5.0 V PCI Curve for A54SX16P Device**

$$I_{OH} = 11.9 \times (V_{OUT} - 5.25) \times (V_{OUT} + 2.45)$$

for $V_{CC} > V_{OUT} > 3.1$ V

EQ 1-1

$$I_{OL} = 78.5 \times V_{OUT} \times (4.4 - V_{OUT})$$

for 0 V $< V_{OUT} < 0.71$ V

EQ 1-2

Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}}$$

EQ 1-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • Standby Power

I _{CC}	V _{CC}	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{\text{DC}} = (I_{\text{standby}}) \times V_{\text{CCA}} + (I_{\text{standby}}) \times V_{\text{CCR}} + (I_{\text{standby}}) \times V_{\text{CCI}} + xV_{\text{OL}} \times I_{\text{OL}} + y(V_{\text{CCI}} - V_{\text{OH}}) \times V_{\text{OH}}$$

EQ 1-6

AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-7

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 \times (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 \times (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 \times (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-8

Definition of Terms Used in Formula

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q₁ = Number of clock loads on the first routed array clock
- q₂ = Number of clock loads on the second routed array clock
- x = Number of I/Os at logic low
- y = Number of I/Os at logic high
- r₁ = Fixed capacitance due to first routed array clock
- r₂ = Fixed capacitance due to second routed array clock
- s₁ = Number of clock loads on the dedicated array clock
- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_{EQHV} = Variable capacitance of dedicated array clock
- C_{EQHF} = Fixed capacitance of dedicated array clock
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz
- f_{q2} = Average second routed array clock rate in MHz
- f_{s1} = Average dedicated array clock rate in MHz

Table 1-13 shows capacitance values for various devices.

Table 1-13 • Capacitance Values for Devices

	A545X08	A545X16	A545X16P	A545X32
C_{EQM} (pF)	4.0	4.0	4.0	4.0
C_{EQI} (pF)	3.4	3.4	3.4	3.4
C_{EQO} (pF)	4.7	4.7	4.7	4.7
C_{EQCR} (pF)	1.6	1.6	1.6	1.6
C_{EQHV}	0.615	0.615	0.615	0.615
C_{EQHF}	60	96	96	140
r_1 (pF)	87	138	138	171
r_2 (pF)	87	138	138	171

Table 1-14 • Power Consumption Guidelines

Description	Power Consumption Guideline
Logic Modules (m)	20% of modules
Inputs Switching (n)	# inputs/4
Outputs Switching (p)	# outputs/4
First Routed Array Clock Loads (q_1)	20% of register cells
Second Routed Array Clock Loads (q_2)	20% of register cells
Load Capacitance (C_L)	35 pF
Average Logic Module Switching Rate (f_m)	$f/10$
Average Input Switching Rate (f_n)	$f/5$
Average Output Switching Rate (f_p)	$f/10$
Average First Routed Array Clock Rate (f_{q1})	$f/2$
Average Second Routed Array Clock Rate (f_{q2})	$f/2$
Average Dedicated Array Clock Rate (f_{s1})	f
Dedicated Clock Array Clock Loads (s_1)	20% of regular modules

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{\text{Total}} = P_{\text{AC}} \text{ (dynamic power)} + P_{\text{DC}} \text{ (static power)}$$

EQ 1-9

Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A545X16P device. A pattern of 0101... was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101... caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

AC Power Dissipation

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-10

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-11

A54SX08 Timing Characteristics

Table 1-17 • A54SX08 Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays ¹										
t _{PD}	Internal Array Module	0.6		0.7		0.8		0.9		ns
Predicted Routing Delays ²										
t _{DC}	FO = 1 Routing Delay, Direct Connect	0.1		0.1		0.1		0.1		ns
t _{FC}	FO = 1 Routing Delay, Fast Connect	0.3		0.4		0.4		0.5		ns
t _{RD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{RD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{RD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{RD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{RD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{RD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns
R-Cell Timing										
t _{RCO}	Sequential Clock-to-Q	0.8		1.1		1.2		1.4		ns
t _{CLR}	Asynchronous Clear-to-Q	0.5		0.6		0.7		0.8		ns
t _{PRESET}	Asynchronous Preset-to-Q	0.7		0.8		0.9		1.0		ns
t _{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t _{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t _{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t _{INYH}	Input Data Pad-to-Y HIGH	1.5		1.7		1.9		2.2		ns
t _{INYL}	Input Data Pad-to-Y LOW	1.5		1.7		1.9		2.2		ns
Input Module Predicted Routing Delays ²										
t _{IRD1}	FO = 1 Routing Delay	0.3		0.4		0.4		0.5		ns
t _{IRD2}	FO = 2 Routing Delay	0.6		0.7		0.8		0.9		ns
t _{IRD3}	FO = 3 Routing Delay	0.8		0.9		1.0		1.2		ns
t _{IRD4}	FO = 4 Routing Delay	1.0		1.2		1.4		1.6		ns
t _{IRD8}	FO = 8 Routing Delay	1.9		2.2		2.5		2.9		ns
t _{IRD12}	FO = 12 Routing Delay	2.8		3.2		3.7		4.3		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

Table 1-19 • A54SX16P Timing Characteristics (Continued)

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TTL/PCI Output Module Timing										
t _{DLH}	Data-to-Pad LOW to HIGH	1.5		1.7		2.0		2.3		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.9		2.2		2.4		2.9		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.3		2.6		3.0		3.5		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.5		1.7		1.9		2.3		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.7		3.1		3.5		4.1		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.9		3.3		3.7		4.4		ns
PCI Output Module Timing ³										
t _{DLH}	Data-to-Pad LOW to HIGH	1.8		2.0		2.3		2.7		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.7		2.0		2.2		2.6		ns
t _{ENZL}	Enable-to-Pad, Z to L	0.8		1.0		1.1		1.3		ns
t _{ENZH}	Enable-to-Pad, Z to H	1.2		1.2		1.5		1.8		ns
t _{ENLZ}	Enable-to-Pad, L to Z	1.0		1.1		1.3		1.5		ns
t _{ENHZ}	Enable-to-Pad, H to Z	1.1		1.3		1.5		1.7		ns
TTL Output Module Timing										
t _{DLH}	Data-to-Pad LOW to HIGH	2.1		2.5		2.8		3.3		ns
t _{DHL}	Data-to-Pad HIGH to LOW	2.0		2.3		2.6		3.1		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.5		2.9		3.2		3.8		ns
t _{ENZH}	Enable-to-Pad, Z to H	3.0		3.5		3.9		4.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	2.3		2.7		3.1		3.6		ns
t _{ENHZ}	Enable-to-Pad, H to Z	2.9		3.3		3.7		4.4		ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

Table 1-20 • A54SX32 Timing Characteristics (Continued)
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Network										
t _{HCKH}	Input LOW to HIGH (pad to R-Cell input)	1.9		2.1		2.4		2.8		ns
t _{HCKL}	Input HIGH to LOW (pad to R-Cell input)	1.9		2.1		2.4		2.8		ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew	0.3		0.4		0.4		0.5		ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency	350		320		280		240		MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (light load) (pad to R-Cell input)	2.4		2.7		3.0		3.5		ns
t _{RCKL}	Input HIGH to LOW (light load) (pad to R-Cell input)	2.4		2.7		3.1		3.6		ns
t _{RCKH}	Input LOW to HIGH (50% load) (pad to R-Cell input)	2.7		3.0		3.5		4.1		ns
t _{RCKL}	Input HIGH to LOW (50% load) (pad to R-Cell input)	2.7		3.1		3.6		4.2		ns
t _{RCKH}	Input LOW to HIGH (100% load) (pad to R-Cell input)	2.7		3.1		3.5		4.1		ns
t _{RCKL}	Input HIGH to LOW (100% load) (pad to R-Cell input)	2.8		3.2		3.6		4.3		ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (light load)	0.85		0.98		1.1		1.3		ns
t _{RCKSW}	Maximum Skew (50% load)	1.23		1.4		1.6		1.9		ns
t _{RCKSW}	Maximum Skew (100% load)	1.30		1.5		1.7		2.0		ns
TTL Output Module Timing ³										
t _{DLH}	Data-to-Pad LOW to HIGH	1.6		1.9		2.1		2.5		ns
t _{DHL}	Data-to-Pad HIGH to LOW	1.6		1.9		2.1		2.5		ns
t _{ENZL}	Enable-to-Pad, Z to L	2.1		2.4		2.8		3.2		ns
t _{ENZH}	Enable-to-Pad, Z to H	2.3		2.7		3.1		3.6		ns
t _{ENLZ}	Enable-to-Pad, L to Z	1.4		1.7		1.9		2.2		ns
t _{ENHZ}	Enable-to-Pad, H to Z	1.3		1.5		1.7		2.0		ns

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

84-Pin PLCC	
Pin Number	A54SX08 Function
1	V _{CCR}
2	GND
3	V _{CCA}
4	PRA, I/O
5	I/O
6	I/O
7	V _{CCI}
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V _{CCI}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V _{CCA}
42	GND
43	V _{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V _{CCA}
60	V _{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V _{CCA}
69	GND
70	I/O

84-Pin PLCC	
Pin Number	A54SX08 Function
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

208-Pin PQFP

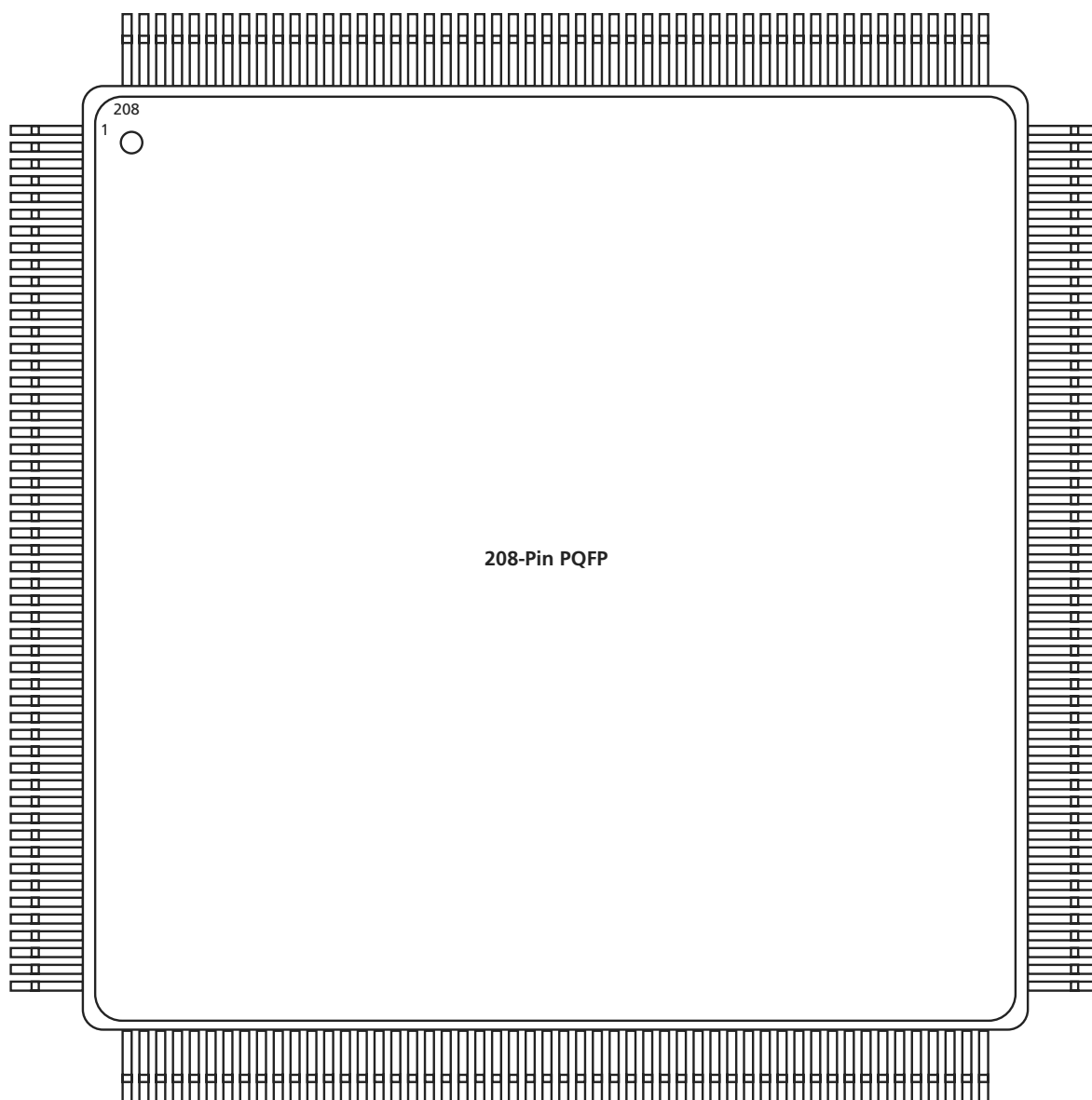


Figure 2-2 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V _{CCI}	V _{CCI}	V _{CCI}
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	V _{CCR}	V _{CCR}	V _{CCR}
26	GND	GND	GND
27	V _{CCA}	V _{CCA}	V _{CCA}
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V _{CCI}	V _{CCI}	V _{CCI}
41	V _{CCA}	V _{CCA}	V _{CCA}
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V _{CCI}	V _{CCI}	V _{CCI}
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
145	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND
147	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA

208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
181	CLKB	CLKB	CLKB
182	V _{CCR}	V _{CCR}	V _{CCR}
183	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
69	HCLK	HCLK	HCLK
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	I/O	I/O	I/O
81	NC	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	TDO, I/O	TDO, I/O	TDO, I/O
88	I/O	I/O	I/O
89	GND	GND	GND
90	NC	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	V _{CCI}	V _{CCI}	V _{CCI}
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O

176-Pin TQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	GND	GND	GND
109	V _{CCA}	V _{CCA}	V _{CCA}
110	GND	GND	GND
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	NC	I/O	I/O
119	I/O	I/O	I/O
120	NC	I/O	I/O
121	NC	I/O	I/O
122	V _{CCA}	V _{CCA}	V _{CCA}
123	GND	GND	GND
124	V _{CCI}	V _{CCI}	V _{CCI}
125	I/O	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	NC	I/O	I/O
132	NC	I/O	I/O
133	GND	GND	GND
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O

329-Pin PBGA

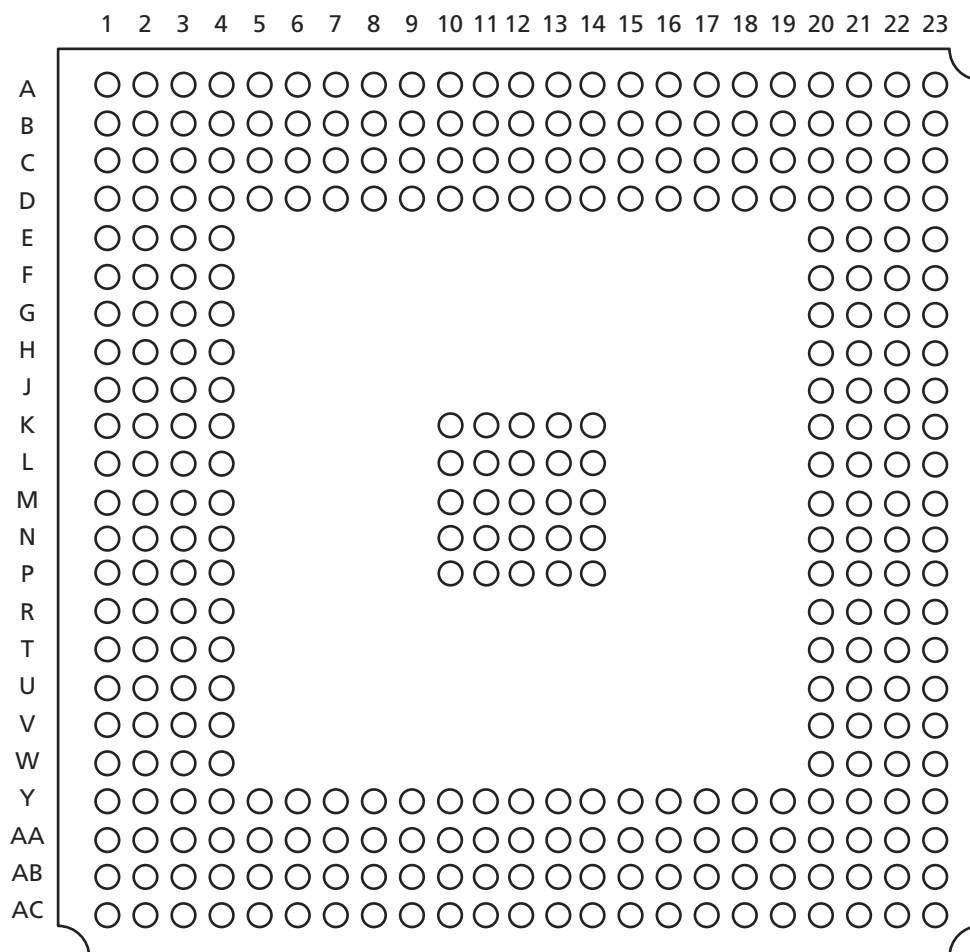


Figure 2-7 • 329-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A1	GND	AA13	I/O	AC2	V _{CCI}	B14	I/O
A2	GND	AA14	I/O	AC3	NC	B15	I/O
A3	V _{CCI}	AA15	I/O	AC4	I/O	B16	I/O
A4	NC	AA16	I/O	AC5	I/O	B17	I/O
A5	I/O	AA17	I/O	AC6	I/O	B18	I/O
A6	I/O	AA18	I/O	AC7	I/O	B19	I/O
A7	V _{CCI}	AA19	I/O	AC8	I/O	B20	I/O
A8	NC	AA20	TDO, I/O	AC9	V _{CCI}	B21	I/O
A9	I/O	AA21	V _{CCI}	AC10	I/O	B22	GND
A10	I/O	AA22	I/O	AC11	I/O	B23	V _{CCI}
A11	I/O	AA23	V _{CCI}	AC12	I/O	C1	NC
A12	I/O	AB1	I/O	AC13	I/O	C2	TDI, I/O
A13	CLKB	AB2	GND	AC14	I/O	C3	GND
A14	I/O	AB3	I/O	AC15	NC	C4	I/O
A15	I/O	AB4	I/O	AC16	I/O	C5	I/O
A16	I/O	AB5	I/O	AC17	I/O	C6	I/O
A17	I/O	AB6	I/O	AC18	I/O	C7	I/O
A18	I/O	AB7	I/O	AC19	I/O	C8	I/O
A19	I/O	AB8	I/O	AC20	I/O	C9	I/O
A20	I/O	AB9	I/O	AC21	NC	C10	I/O
A21	NC	AB10	I/O	AC22	V _{CCI}	C11	I/O
A22	V _{CCI}	AB11	PRB, I/O	AC23	GND	C12	I/O
A23	GND	AB12	I/O	B1	V _{CCI}	C13	I/O
AA1	V _{CCI}	AB13	HCLK	B2	GND	C14	I/O
AA2	I/O	AB14	I/O	B3	I/O	C15	I/O
AA3	GND	AB15	I/O	B4	I/O	C16	I/O
AA4	I/O	AB16	I/O	B5	I/O	C17	I/O
AA5	I/O	AB17	I/O	B6	I/O	C18	I/O
AA6	I/O	AB18	I/O	B7	I/O	C19	I/O
AA7	I/O	AB19	I/O	B8	I/O	C20	I/O
AA8	I/O	AB20	I/O	B9	I/O	C21	V _{CCI}
AA9	I/O	AB21	I/O	B10	I/O	C22	GND
AA10	I/O	AB22	GND	B11	I/O	C23	NC
AA11	I/O	AB23	I/O	B12	PRA, I/O	D1	I/O
AA12	I/O	AC1	GND	B13	CLKA	D2	I/O

329-Pin PBGA		329-Pin PBGA		329-Pin PBGA		329-Pin PBGA	
Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function	Pin Number	A545X32 Function
D3	I/O	F22	I/O	K20	I/O	N11	GND
D4	TCK, I/O	F23	I/O	K21	I/O	N12	GND
D5	I/O	G1	I/O	K22	I/O	N13	GND
D6	I/O	G2	I/O	K23	I/O	N14	GND
D7	I/O	G3	I/O	L1	I/O	N20	NC
D8	I/O	G4	I/O	L2	I/O	N21	I/O
D9	I/O	G20	I/O	L3	I/O	N22	I/O
D10	I/O	G21	I/O	L4	V _{CCR}	N23	I/O
D11	V _{CCA}	G22	I/O	L10	GND	P1	I/O
D12	V _{CCR}	G23	GND	L11	GND	P2	I/O
D13	I/O	H1	I/O	L12	GND	P3	I/O
D14	I/O	H2	I/O	L13	GND	P4	I/O
D15	I/O	H3	I/O	L14	GND	P10	GND
D16	I/O	H4	I/O	L20	V _{CCR}	P11	GND
D17	I/O	H20	V _{CCA}	L21	I/O	P12	GND
D18	I/O	H21	I/O	L22	I/O	P13	GND
D19	I/O	H22	I/O	L23	NC	P14	GND
D20	I/O	H23	I/O	M1	I/O	P20	I/O
D21	I/O	J1	NC	M2	I/O	P21	I/O
D22	I/O	J2	I/O	M3	I/O	P22	I/O
D23	I/O	J3	I/O	M4	V _{CCA}	P23	I/O
E1	V _{CCI}	J4	I/O	M10	GND	R1	I/O
E2	I/O	J20	I/O	M11	GND	R2	I/O
E3	I/O	J21	I/O	M12	GND	R3	I/O
E4	I/O	J22	I/O	M13	GND	R4	I/O
E20	I/O	J23	I/O	M14	GND	R20	I/O
E21	I/O	K1	I/O	M20	V _{CCA}	R21	I/O
E22	I/O	K2	I/O	M21	I/O	R22	I/O
E23	I/O	K3	I/O	M22	I/O	R23	I/O
F1	I/O	K4	I/O	M23	V _{CCI}	T1	I/O
F2	TMS	K10	GND	N1	I/O	T2	I/O
F3	I/O	K11	GND	N2	I/O	T3	I/O
F4	I/O	K12	GND	N3	I/O	T4	I/O
F20	I/O	K13	GND	N4	I/O	T20	I/O
F21	I/O	K14	GND	N10	GND	T21	I/O

Actel and the Actel logo are registered trademarks of Actel Corporation.
All other trademarks are the property of their owners.



www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA

Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom

Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan

www.jp.actel.com

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan

Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong

www.actel.com.cn

Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong

Phone +852 2185 6460
Fax +852 2185 6488