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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	130
Number of Gates	12000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx08-2pqg208i

SX Family FPGAs

General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design

The SX family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

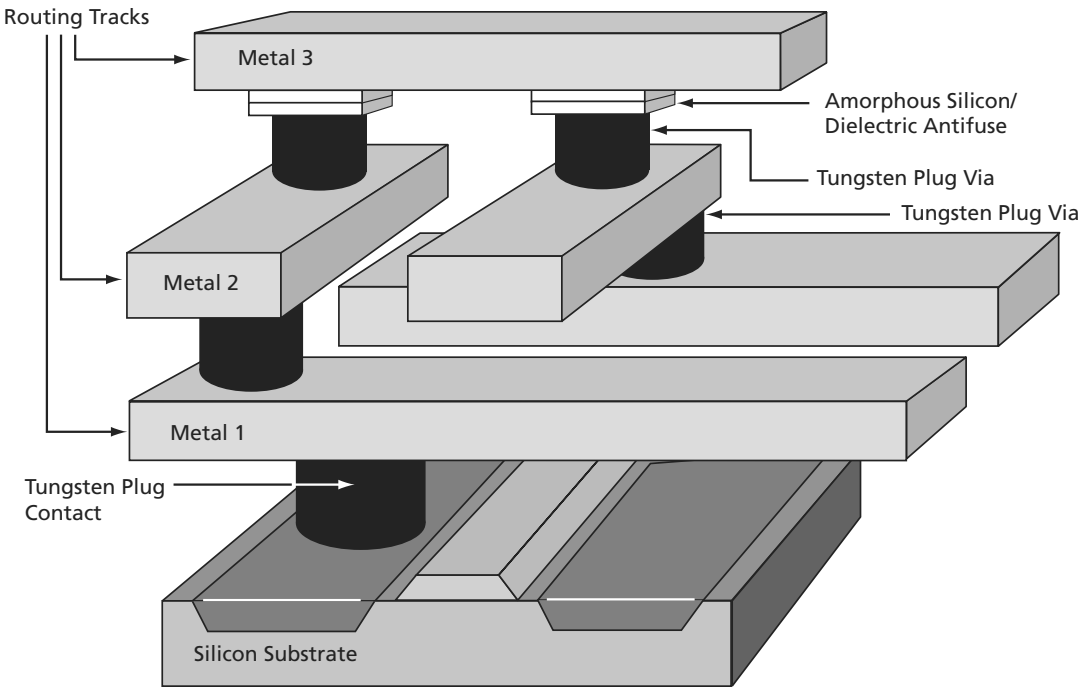

Figure 1-1 • **SX Family Interconnect Elements**

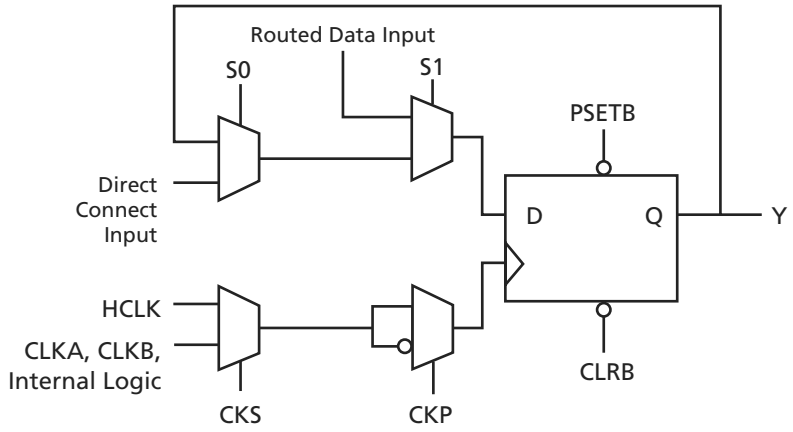

Figure 1-2 • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

Other Architectural Features

Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35 µ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with a capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

Table 1-1 • **Supply Voltages**

Device	V_{CCA}	V_{CCI}	V_{CCR}	Maximum Input Tolerance	Maximum Output Drive
A54SX08 A54SX16 A54SX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
A54SX16-P*	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V

Note: **A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.*

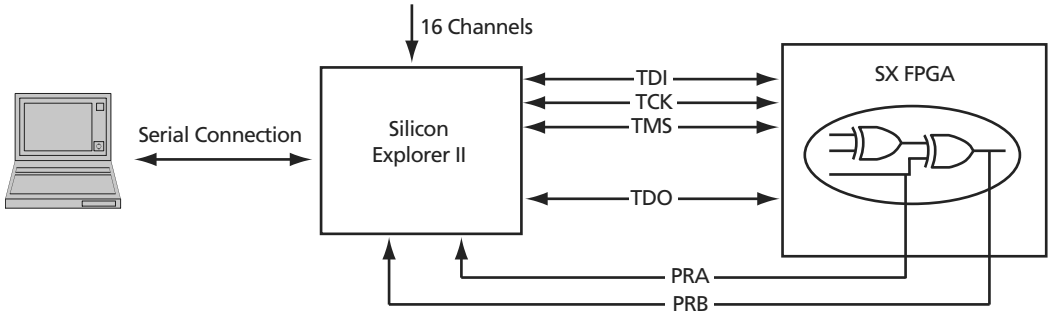

Figure 1-8 • **Probe Setup**

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the *Programming Antifuse Devices* application note and the *Silicon Sculptor II User's Guide*.

3.3 V / 5 V Operating Conditions

Table 1-3 • **Absolute Maximum Ratings[1]**

Symbol	Parameter	Limits	Units
V_{CCR}[2]	DC Supply Voltage[3]	–0.3 to + 6.0	V
V_{CCA}[2]	DC Supply Voltage	–0.3 to + 4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	–0.3 to + 4.0	V
V_{CCI}[2]	DC Supply Voltage (A54SX16P)	–0.3 to + 6.0	V
V_I	Input Voltage	–0.5 to + 5.5	V
V_O	Output Voltage	–0.5 to + 3.6	V
I_{IO}	I/O Source Sink Current[3]	–30 to + 5.0	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.*
3. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward-bias and can draw excessive current.*

Table 1-4 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	–40 to + 85	–55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	%V_{CC}
5.0 V Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note: **Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 1-5 • **Electrical Specifications**

		Commercial		Industrial		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{OH}	(I_{OH} = –20 µA) (CMOS) (I_{OH} = –8 mA) (TTL) (I_{OH} = –6 mA) (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	(I_{OL}= 20 µA) (CMOS) (I_{OL} = 12 mA) (TTL) (I_{OL} = 8 mA) (TTL)		0.10 0.50		 0.50	V
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

PCI Compliance for the SX Family

The SX family supports 3.3 V and 5.0 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 1-6 • **A54SX16P DC Specifications (5.0 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		3.0	3.6	V
V_{CCR}	Supply Voltage required for Internal Biasing		4.75	5.25	V
V_{CCI}	Supply Voltage for I/Os		4.75	5.25	V
V_{IH}	Input High Voltage[1]		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage[1]		–0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance[4]			8	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used, AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*
4. *Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].*

A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • **A54SX16P AC Specifications (3.3 V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CC}$ [1]			mA
		$0.3V_{CC} \le V_{OUT} < 0.9V_{CC}$ [1]	$-12V_{CC}$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}$ [1, 2]	$-17.1 + (V_{CC} - V_{OUT})$	EQ 1-3 on page 1-14	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CC}$	mA
$I_{OL(AC)}$	Switching Current High	$V_{CC} > V_{OUT} \ge 0.6V_{CC}$ [1]			mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}$ [1]	$16V_{CC}$		mA
		$0.18V_{CC} > V_{OUT} > 0$ [1, 2]	$26.7V_{OUT}$	EQ 1-4 on page 1-14	mA
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CC}$	
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$-3 < V_{IN} \le -1$	$25 + (V_{IN} - V_{OUT} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate[3]	$0.2V_{CC}$ to $0.6V_{CC}$ load	1	4	V/ns
$slew_F$	Output Fall Slew Rate[3]	$0.6V_{CC}$ to $0.2V_{CC}$ load	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

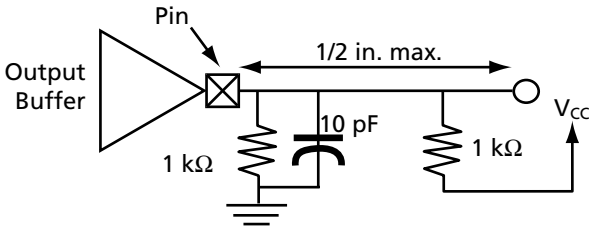

Figure 1-10 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

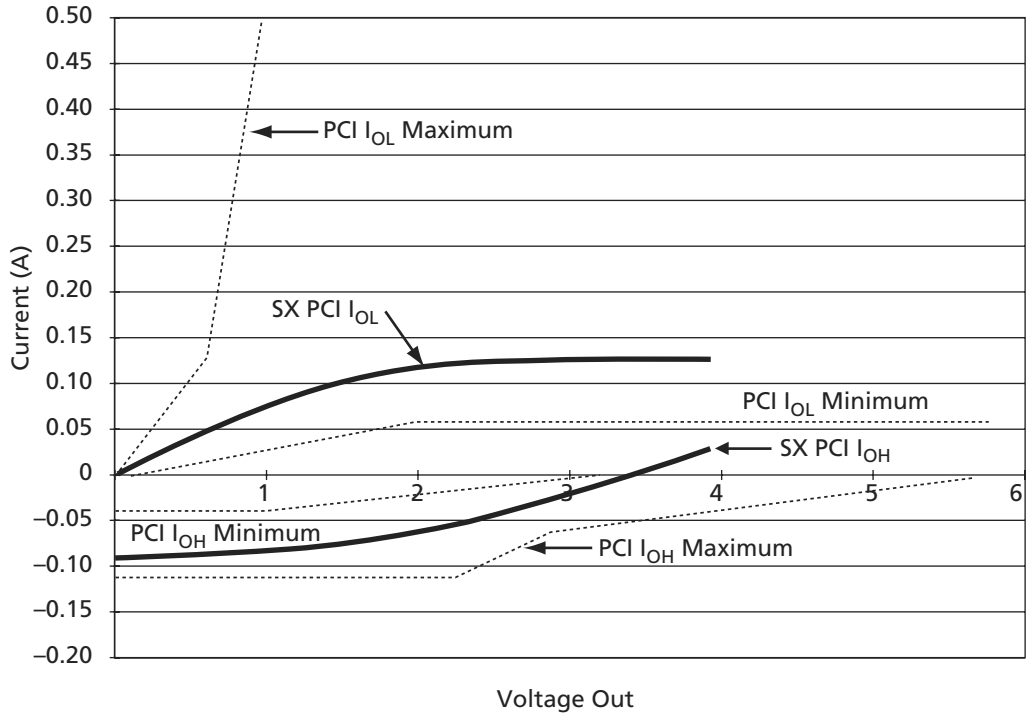

Figure 1-10 • **3.3 V PCI Curve for A54SX16P Device**

$$I_{OH} = (98.0/V_{CC}) \times (V_{OUT} - V_{CC}) \times (V_{OUT} + 0.4V_{CC})$$
$$\text{for } V_{CC} > V_{OUT} > 0.7\ V_{CC} \qquad \textit{EQ 1-3}$$

$$I_{OL} = (256/V_{CC}) \times V_{OUT} \times (V_{CC} - V_{OUT})$$
$$\text{for } 0\ V < V_{OUT} < 0.18\ V_{CC} \qquad \textit{EQ 1-4}$$

Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{Total} = P_{DC} + P_{AC}$$

EQ 1-5

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • **Standby Power**

I_{CC}	V_{CC}	Power
4 mA	3.6 V	14.4 mW

The DC power dissipation is defined in EQ 1-6.

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + xV_{OL} \times I_{OL} + y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-6

AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

EQ 1-7

$$P_{AC} = V_{CCA}^2 \times [(m \times C_{EQM} \times f_m)_{Module} + (n \times C_{EQI} \times f_n)_{Input\ Buffer} + (p \times (C_{EQO} + C_L) \times f_p)_{Output\ Buffer} + (0.5 \times (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1}))_{RCLKA} + (0.5 \times (q2 \times CEQCR \times f_{q2}) + (r2 \times f_{q2}))RCLKB + (0.5 \times (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1}))_{HCLK}]$$

EQ 1-8

Definition of Terms Used in Formula

m = Number of logic modules switching at f_m
n = Number of input buffers switching at f_n
p = Number of output buffers switching at f_p
q_1 = Number of clock loads on the first routed array clock
q_2 = Number of clock loads on the second routed array clock
x = Number of I/Os at logic low
y = Number of I/Os at logic high
r_1 = Fixed capacitance due to first routed array clock
r_2 = Fixed capacitance due to second routed array clock
s_1 = Number of clock loads on the dedicated array clock
C_{EQM} = Equivalent capacitance of logic modules in pF
C_{EQI} = Equivalent capacitance of input buffers in pF
C_{EQO} = Equivalent capacitance of output buffers in pF
C_{EQCR} = Equivalent capacitance of routed array clock in pF
C_{EQHV} = Variable capacitance of dedicated array clock
C_{EQHF} = Fixed capacitance of dedicated array clock
C_L = Output lead capacitance in pF
f_m = Average logic module switching rate in MHz
f_n = Average input buffer switching rate in MHz
f_p = Average output buffer switching rate in MHz
f_{q1} = Average first routed array clock rate in MHz
f_{q2} = Average second routed array clock rate in MHz
f_{s1} = Average dedicated array clock rate in MHz

Step 1: Define Terms Used in Formula

	V_{CCA}	3.3
Module		
Number of logic modules switching at f_m (Used 50%)	m	264
Average logic modules switching rate f_m (MHz) (Guidelines: f/10)	f_m	20
Module capacitance C_{EQM} (pF)	C_{EQM}	4.0
Input Buffer		
Number of input buffers switching at f_n	n	1
Average input switching rate f_n (MHz) (Guidelines: f/5)	f_n	40
Input buffer capacitance C_{EQI} (pF)	C_{EQI}	3.4
Output Buffer		
Number of output buffers switching at f_p	p	1
Average output buffers switching rate f_p(MHz) (Guidelines: f/10)	f_p	20
Output buffers buffer capacitance C_{EQO} (pF)	C_{EQO}	4.7
Output Load capacitance C_L (pF)	C_L	35
RCLKA		
Number of Clock loads q_1	q_1	528
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q1}	200
Fixed capacitance (pF)	r_1	138
RCLKB		
Number of Clock loads q_2	q_2	0
Capacitance of routed array clock (pF)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q2}	0
Fixed capacitance (pF)	r_2	138
HCLK		
Number of Clock loads	s_1	0
Variable capacitance of dedicated array clock (pF)	C_{EQHV}	0.615
Fixed capacitance of dedicated array clock (pF)	C_{EQHF}	96
Average clock rate (MHz)	f_{s1}	0

Step 2: Calculate Dynamic Power Consumption

$V_{CCA} \times V_{CCA}$	10.89
$m \times f_m \times C_{EQM}$	0.02112
$n \times f_n \times C_{EQI}$	0.000136
$p \times f_p \times (C_{EQO}+C_L)$	0.000794
$0.5\ (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$	0.11208
$0.5(q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$	0
$0.5\ (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$	0

P_{AC} = 1.461 W

Step 3: Calculate DC Power Dissipation

DC Power Dissipation

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{standby}) \times V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$P_{DC} = (I_{standby}) \times V_{CCA}$

P_{DC} = .55 mA × 3.3 V

P_{DC} = 0.001815 W

Step 4: Calculate Total Power Consumption

$P_{Total} = P_{AC} + P_{DC}$

P_{Total} = 1.461 + 0.001815

P_{Total} = 1.4628 W

Step 5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

Table 1-15 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min.	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Thin Quad Flat Pack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	38	32	°C/W
Plastic Quad Flat Pack (PQFP) without Heat Spreader	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W
Plastic Ball Grid Array (PBGA)	313	3	23	17	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W

Note: *SX08 does not have a heat spreader.*

Table 1-16 • **Temperature and Voltage Derating Factors***

	Junction Temperature						
V_{CCA}	–55	–40	0	25	70	85	125
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

Note: **Normalized to worst-case commercial, T_J = 70°C, V_{CCA} = 3.0 V*

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

A54SX32 Timing Characteristics

Table 1-20 • **A54SX32 Timing Characteristics (Worst-Case Commercial Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)**

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{RD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{RD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{RD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{IRD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{IRD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{IRD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
145	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND
147	I/O	I/O	I/O
148	V_{CCI}	V_{CCI}	V_{CCI}
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA

208-Pin PQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
181	CLKB	CLKB	CLKB
182	V_{CCR}	V_{CCR}	V_{CCR}
183	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V_{CCI}	V_{CCI}	V_{CCI}
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

Note: ** Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).*

176-Pin TQFP

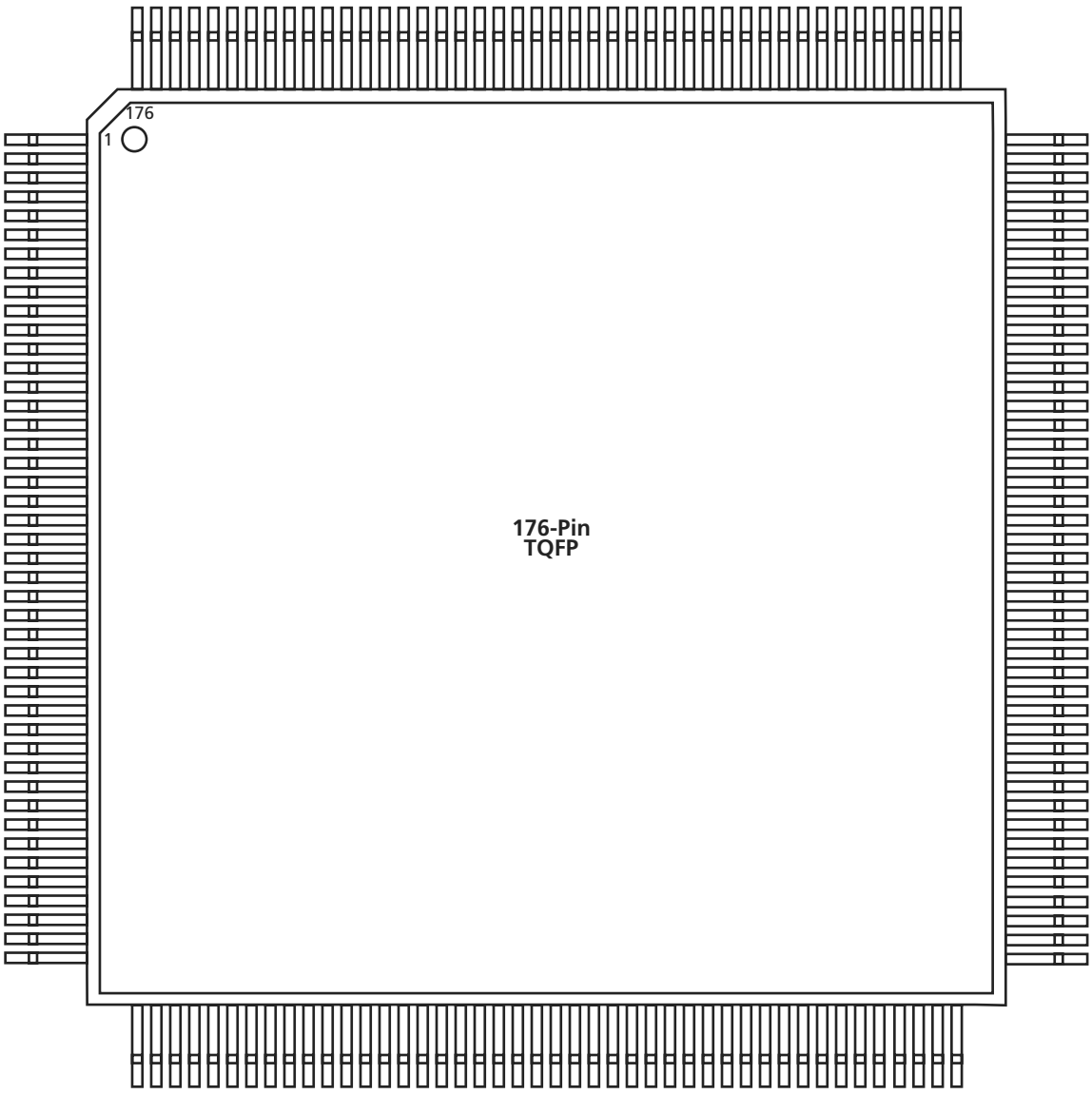

Figure 2-4 • **176-Pin TQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

100-Pin VQFP

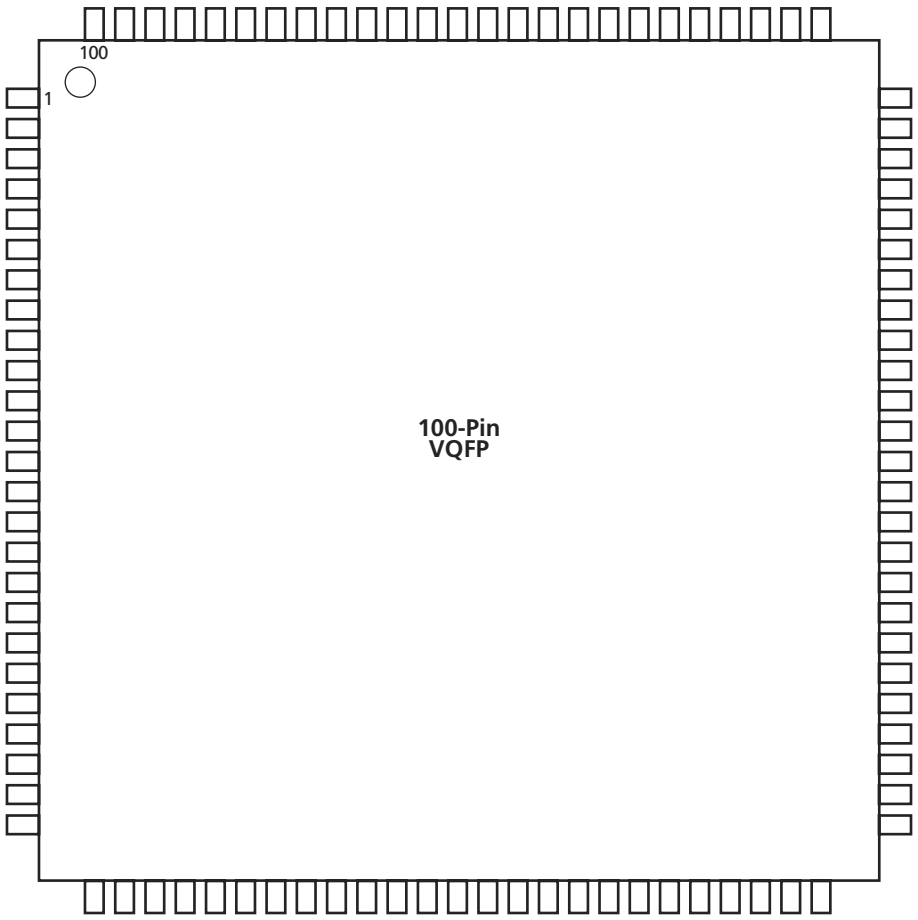

Figure 2-5 • **100-Pin VQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

313-Pin PBGA	
Pin Number	**A54SX32 Function**
A1	GND
A3	NC
A5	I/O
A7	I/O
A9	I/O
A11	I/O
A13	V_{CCR}
A15	I/O
A17	I/O
A19	I/O
A21	I/O
A23	NC
A25	GND
AA1	I/O
AA3	I/O
AA5	NC
AA7	I/O
AA9	NC
AA11	I/O
AA13	I/O
AA15	I/O
AA17	I/O
AA19	I/O
AA21	I/O
AA23	NC
AA25	I/O
AB2	NC
AB4	NC
AB6	I/O
AB8	I/O
AB10	I/O
AB12	I/O
AB14	I/O
AB16	I/O
AB18	V_{CCI}
AB20	NC
AB22	I/O
AB24	I/O
AC1	I/O
AC3	I/O

313-Pin PBGA	
Pin Number	**A54SX32 Function**
AC5	I/O
AC7	I/O
AC9	I/O
AC11	I/O
AC13	V_{CCR}
AC15	I/O
AC17	I/O
AC19	I/O
AC21	I/O
AC23	I/O
AC25	NC
AD2	GND
AD4	I/O
AD6	V_{CCI}
AD8	I/O
AD10	I/O
AD12	PRB, I/O
AD14	I/O
AD16	I/O
AD18	I/O
AD20	I/O
AD22	NC
AD24	I/O
AE1	NC
AE3	I/O
AE5	I/O
AE7	I/O
AE9	I/O
AE11	I/O
AE13	V_{CCA}
AE15	I/O
AE17	I/O
AE19	I/O
AE21	I/O
AE23	TDO, I/O
AE25	GND
B2	TCK, I/O
B4	I/O
B6	I/O
B8	I/O

313-Pin PBGA	
Pin Number	**A54SX32 Function**
B10	I/O
B12	I/O
B14	I/O
B16	I/O
B18	I/O
B20	I/O
B22	I/O
B24	I/O
C1	TDI, I/O
C3	I/O
C5	NC
C7	I/O
C9	I/O
C11	I/O
C13	V_{CCI}
C15	I/O
C17	I/O
C19	V_{CCI}
C21	I/O
C23	I/O
C25	NC
D2	I/O
D4	NC
D6	I/O
D8	I/O
D10	I/O
D12	I/O
D14	I/O
D16	I/O
D18	I/O
D20	I/O
D22	I/O
D24	NC
E1	I/O
E3	NC
E5	I/O
E7	I/O
E9	I/O
E11	I/O
E13	V_{CCA}

313-Pin PBGA	
Pin Number	**A54SX32 Function**
E15	I/O
E17	I/O
E19	I/O
E21	I/O
E23	I/O
E25	I/O
F2	I/O
F4	I/O
F6	NC
F8	I/O
F10	NC
F12	I/O
F14	I/O
F16	NC
F18	I/O
F20	I/O
F22	I/O
F24	I/O
G1	I/O
G3	TMS
G5	I/O
G7	I/O
G9	V_{CCI}
G11	I/O
G13	CLKB
G15	I/O
G17	I/O
G19	I/O
G21	I/O
G23	I/O
G25	I/O
H2	I/O
H4	I/O
H6	I/O
H8	I/O
H10	I/O
H12	PRA, I/O
H14	I/O
H16	I/O
H18	NC

329-Pin PBGA

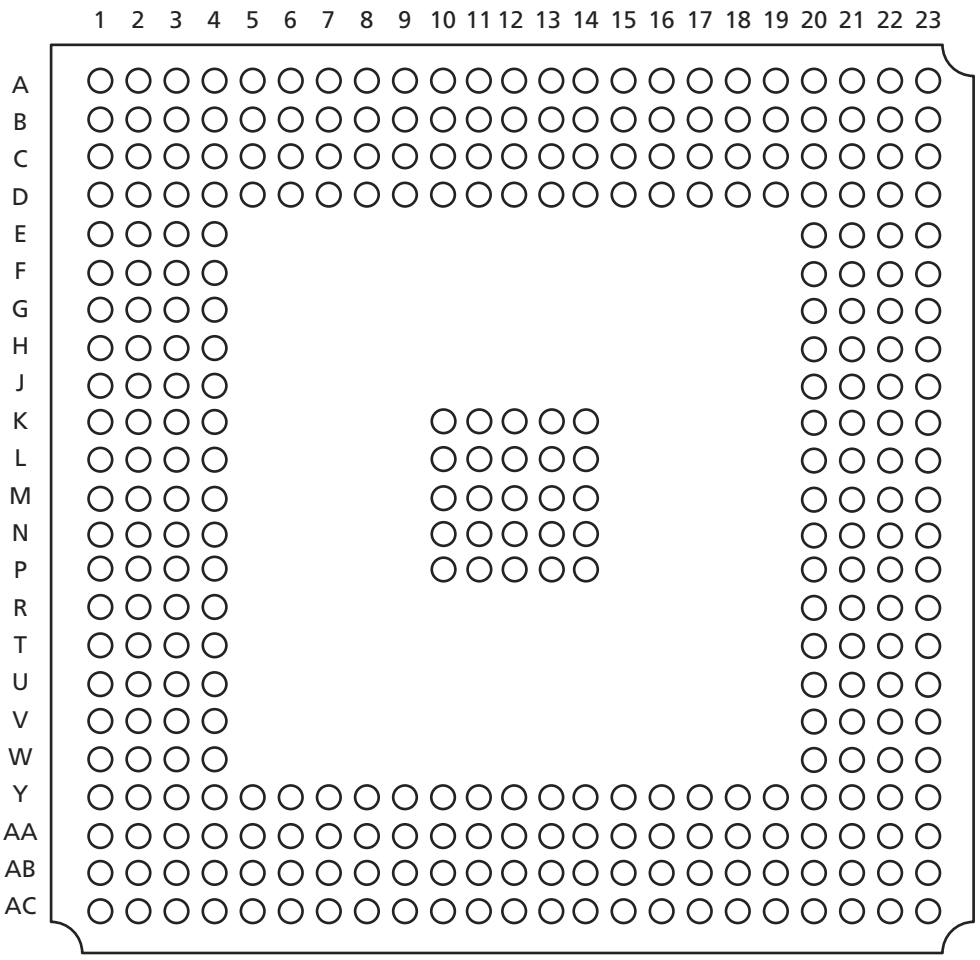

Figure 2-7 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

144-Pin FBGA	
Pin Number	**A54SX08 Function**
A1	I/O
A2	I/O
A3	I/O
A4	I/O
A5	V_{CCA}
A6	GND
A7	CLKA
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
B1	I/O
B2	GND
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	CLKB
B8	I/O
B9	I/O
B10	I/O
B11	GND
B12	I/O
C1	I/O
C2	I/O
C3	TCK, I/O
C4	I/O
C5	I/O
C6	PRA, I/O
C7	I/O
C8	I/O
C9	I/O
C10	I/O
C11	I/O
C12	I/O

144-Pin FBGA	
Pin Number	**A54SX08 Function**
D1	I/O
D2	V_{CCI}
D3	TDI, I/O
D4	I/O
D5	I/O
D6	I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O
E1	I/O
E2	I/O
E3	I/O
E4	I/O
E5	TMS
E6	V_{CCI}
E7	V_{CCI}
E8	V_{CCI}
E9	V_{CCA}
E10	I/O
E11	GND
E12	I/O
F1	I/O
F2	I/O
F3	V_{CCR}
F4	I/O
F5	GND
F6	GND
F7	GND
F8	V_{CCI}
F9	I/O
F10	GND
F11	I/O
F12	I/O

144-Pin FBGA	
Pin Number	**A54SX08 Function**
G1	I/O
G2	GND
G3	I/O
G4	I/O
G5	GND
G6	GND
G7	GND
G8	V_{CCI}
G9	I/O
G10	I/O
G11	I/O
G12	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H5	V_{CCA}
H6	V_{CCA}
H7	V_{CCI}
H8	V_{CCI}
H9	V_{CCA}
H10	I/O
H11	I/O
H12	V_{CCR}
J1	I/O
J2	I/O
J3	I/O
J4	I/O
J5	I/O
J6	PRB, I/O
J7	I/O
J8	I/O
J9	I/O
J10	I/O
J11	I/O
J12	V_{CCA}

144-Pin FBGA	
Pin Number	**A54SX08 Function**
K1	I/O
K2	I/O
K3	I/O
K4	I/O
K5	I/O
K6	I/O
K7	GND
K8	I/O
K9	I/O
K10	GND
K11	I/O
K12	I/O
L1	GND
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L6	I/O
L7	HCLK
L8	I/O
L9	I/O
L10	I/O
L11	I/O
L12	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M5	I/O
M6	I/O
M7	V_{CCA}
M8	I/O
M9	I/O
M10	I/O
M11	TDO, I/O
M12	I/O

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