Welcome to E-XFL.COM

Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	768
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	113
Number of Gates	12000
Voltage - Supply	3V ~ 3.6V, 4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a54sx08-2tqg144i

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.
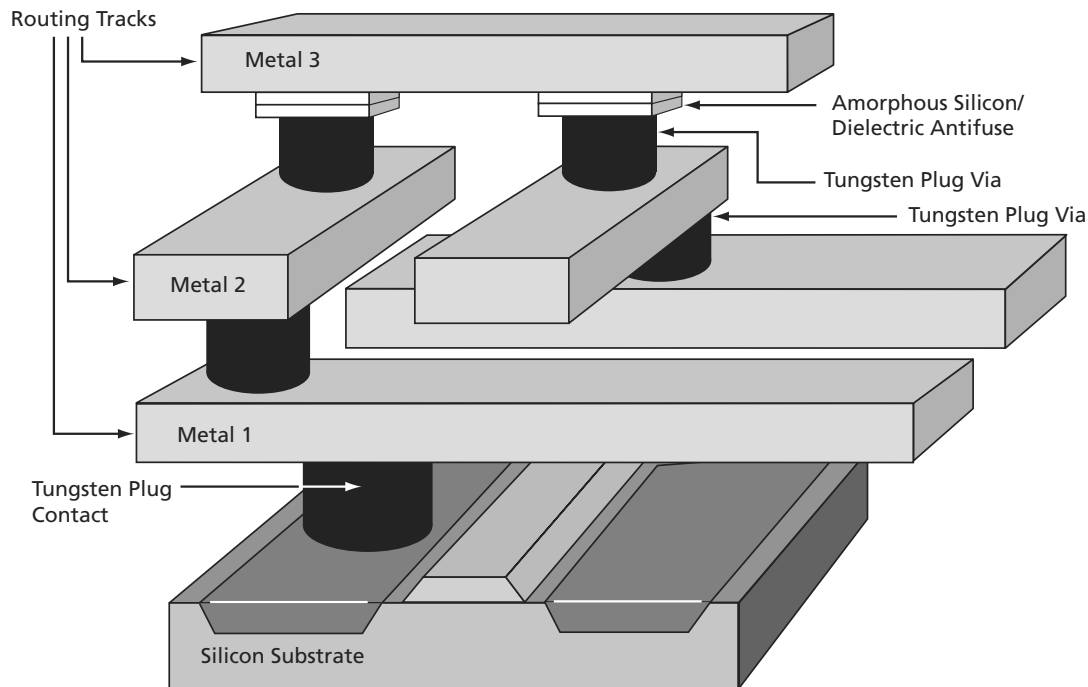

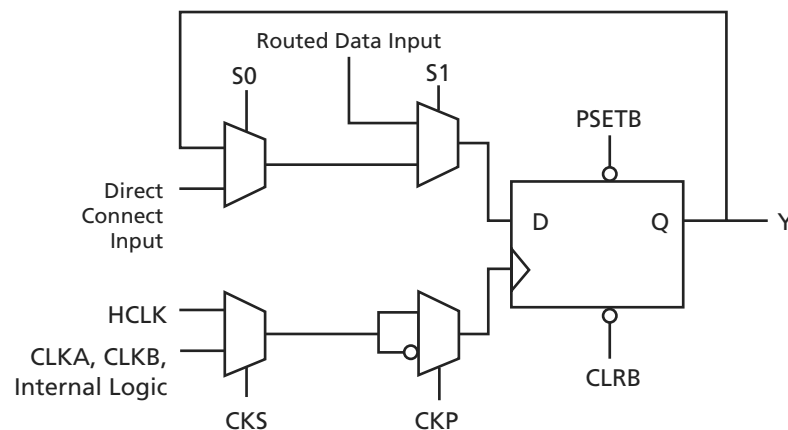*Figure 1-1* • **SX Family Interconnect Elements**

Figure 1-2 • **R-Cell**

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect,* which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.
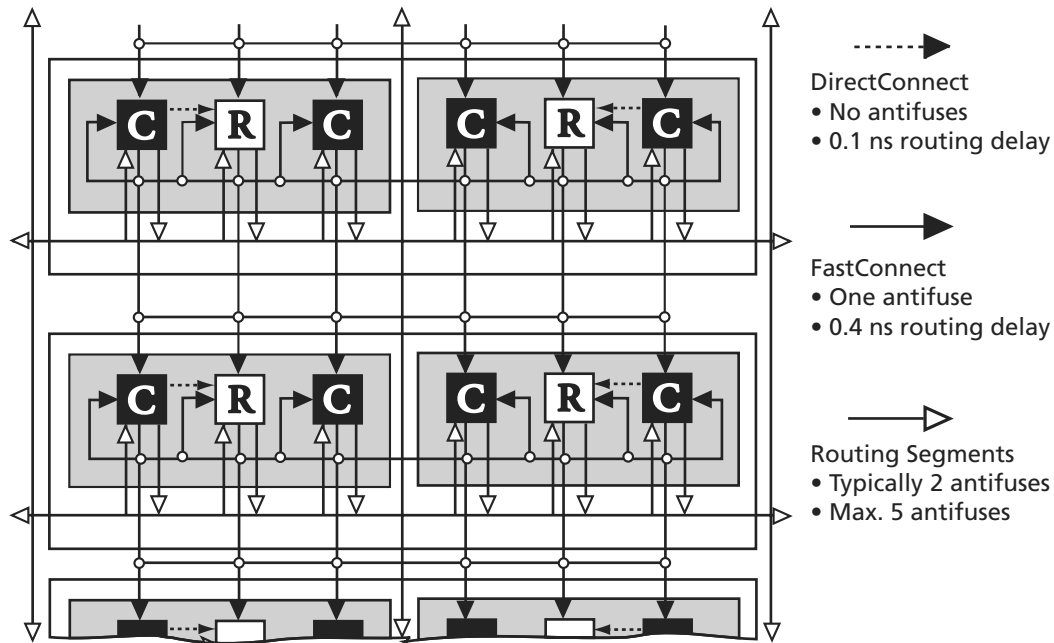

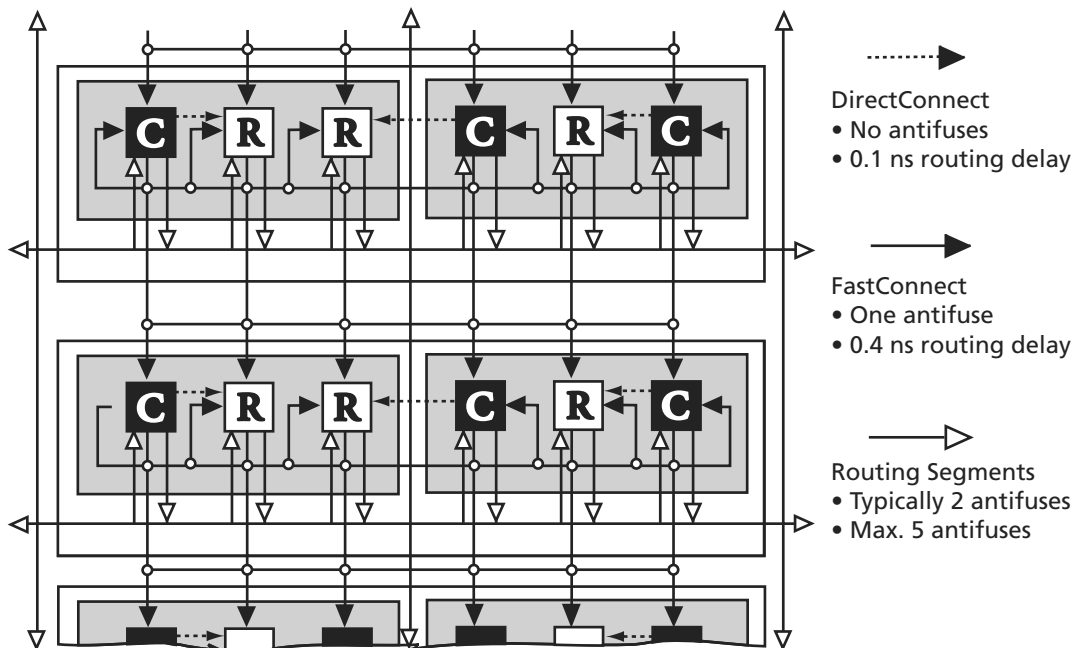*Figure 1-5* • **DirectConnect and FastConnect for Type 1 SuperClusters**

Figure 1-6 • **DirectConnect and FastConnect for Type 2 SuperClusters**

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

Other Architectural Features

Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35 µ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with a capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

Table 1-1 • **Supply Voltages**

Device	V_{CCA}	V_{CCI}	V_{CCR}	Maximum Input Tolerance	Maximum Output Drive
A54SX08 A54SX16 A54SX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
A54SX16-P*	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
	3.3 V	5.0 V	5.0 V	5.0 V	5.0 V

Note: **A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.*

Table 1-4 • **Recommended Operating Conditions**

Parameter	Commercial	Industrial	Military	Units
Temperature Range*	0 to + 70	−40 to + 85	−55 to +125	°C
3.3 V Power Supply Tolerance	±10	±10	±10	%V_{CC}
5.0 V Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Table 1-5 • **Electrical Specifications**

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{OH}	(I_{OH} = −20 µA) (CMOS)	(V_{CCI} − 0.1)	V_{CCI}	(V_{CCI} − 0.1)	V_{CCI}	V
	(I_{OH} = −8 mA) (TTL)	2.4	V_{CCI}			
	(I_{OH} = −6 mA) (TTL)			2.4	V_{CCI}	
V_{OL}	(I_{OL}= 20 µA) (CMOS)		0.10			V
	(I_{OL} = 12 mA) (TTL)		0.50			
	(I_{OL} = 8 mA) (TTL)				0.50	
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Evaluating Power in SX Devices" on page 1-16.				

Figure 1-10 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.
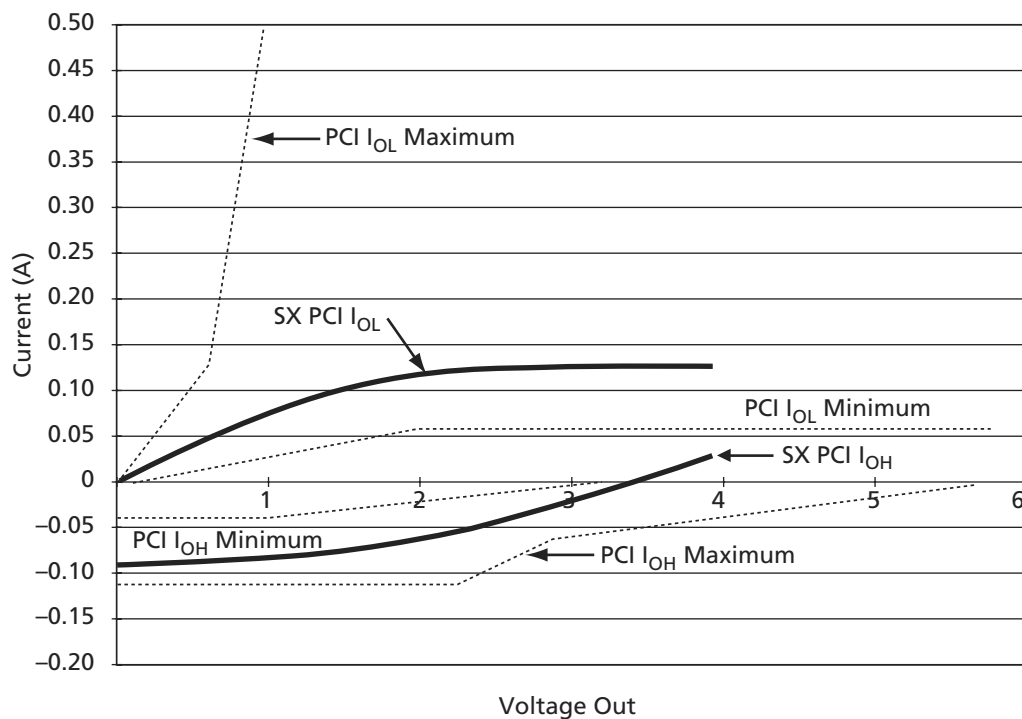

Figure 1-10 • **3.3 V PCI Curve for A54SX16P Device**

$I_{OH} = (98.0/V_{CC}) \times (V_{OUT} - V_{CC}) \times (V_{OUT} + 0.4V_{CC})$

for $V_{CC} > V_{OUT} > 0.7\ V_{CC}$

EQ 1-3

$I_{OL} = (256/V_{CC}) \times V_{OUT} \times (V_{CC} - V_{OUT})$

for $0\ V < V_{OUT} < 0.18\ V_{CC}$

EQ 1-4

Power-Up Sequencing

Table 1-10 • **Power-Up Sequencing**

V_{CCA}	V_{CCR}	V_{CCI}	Power-Up Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: No inputs should be driven (high or low) before completion of power-up.

Power-Down Sequencing

Table 1-11 • **Power-Down Sequencing**

V_{CCA}	V_{CCR}	V_{CCI}	Power-Down Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
A54SX16P				
3.3 V	3.3 V	3.3 V	3.3 V Only	No possible damage to device
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device
3.3 V	5.0 V	5.0 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Note: No inputs should be driven (high or low) after the beginning of the power-down sequence.
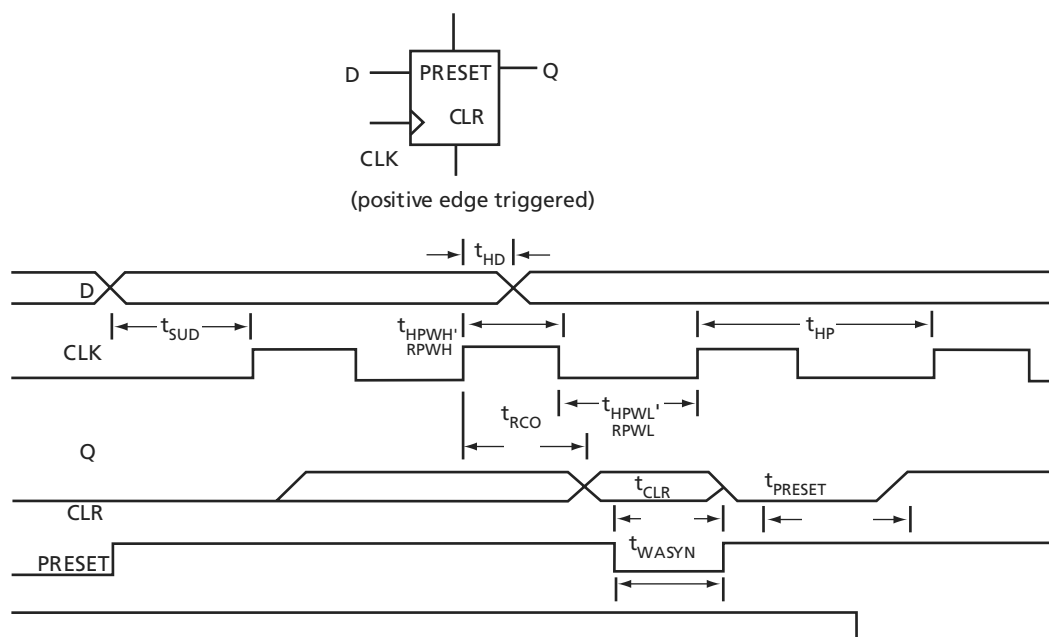
Register Cell Timing Characteristics

Figure 1-17 • **Flip-Flops**

Timing Characteristics

Timing characteristics for SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO = 24) routing delays in the datasheet specifications section.

Timing Derating

SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX08 Timing Characteristics

Table 1-17 • **A54SX08 Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed Min.	'–3' Speed Max.	'–2' Speed Min.	'–2' Speed Max.	'–1' Speed Min.	'–1' Speed Max.	'Std' Speed Min.	'Std' Speed Max.	Units
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Input Module Predicted Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Characteristics

Table 1-18 • **A54SX16 Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed Min.	'–3' Speed Max.	'–2' Speed Min.	'–2' Speed Max.	'–1' Speed Min.	'–1' Speed Max.	'Std' Speed Min.	'Std' Speed Max.	Units
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

A54SX16P Timing Characteristics

Table 1-19 • **A54SX16P Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.9		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{IRD3}	FO = 3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{IRD4}	FO = 4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD8}	FO = 8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{IRD12}	FO = 12 Routing Delay		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Delays based on 10 pF loading.*

Table 1-19 • **A54SX16P Timing Characteristics (Continued)**
(Worst-Case Commercial Conditions, V$_{CCR}$ = 4.75 V, V$_{CCA}$,V$_{CCI}$ = 3.0 V, T$_J$ = 70°C)

Parameter	Description	'–3' Speed Min.	'–3' Speed Max.	'–2' Speed Min.	'–2' Speed Max.	'–1' Speed Min.	'–1' Speed Max.	'Std' Speed Min.	'Std' Speed Max.	Units
Dedicated (Hardwired) Array Clock Network										
t$_{HCKH}$	Input LOW to HIGH (pad to R-Cell input)		1.2		1.4		1.5		1.8	ns
t$_{HCKL}$	Input HIGH to LOW (pad to R-Cell input)		1.2		1.4		1.6		1.9	ns
t$_{HPWH}$	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t$_{HPWL}$	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t$_{HCKSW}$	Maximum Skew		0.2		0.2		0.3		0.3	ns
t$_{HP}$	Minimum Period	2.7		3.1		3.6		4.2		ns
f$_{HMAX}$	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t$_{RCKH}$	Input LOW to HIGH (light load) (pad to R-Cell input)		1.6		1.8		2.1		2.5	ns
t$_{RCKL}$	Input HIGH to LOW (Light Load) (pad to R-Cell input)		1.8		2.0		2.3		2.7	ns
t$_{RCKH}$	Input LOW to HIGH (50% load) (pad to R-Cell input)		1.8		2.1		2.5		2.8	ns
t$_{RCKL}$	Input HIGH to LOW (50% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t$_{RCKH}$	Input LOW to HIGH (100% load) (pad to R-Cell input)		1.8		2.1		2.4		2.8	ns
t$_{RCKL}$	Input HIGH to LOW (100% load) (pad to R-Cell input)		2.0		2.2		2.5		3.0	ns
t$_{RPWH}$	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t$_{RPWL}$	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t$_{RCKSW}$	Maximum Skew (light load)		0.5		0.5		0.5		0.7	ns
t$_{RCKSW}$	Maximum Skew (50% load)		0.5		0.6		0.7		0.8	ns
t$_{RCKSW}$	Maximum Skew (100% load)		0.5		0.6		0.7		0.8	ns
TTL Output Module Timing										
t$_{DLH}$	Data-to-Pad LOW to HIGH		2.4		2.8		3.1		3.7	ns
t$_{DHL}$	Data-to-Pad HIGH to LOW		2.3		2.9		3.2		3.8	ns
t$_{ENZL}$	Enable-to-Pad, Z to L		3.0		3.4		3.9		4.6	ns
t$_{ENZH}$	Enable-to-Pad, Z to H		3.3		3.8		4.3		5.0	ns
t$_{ENLZ}$	Enable-to-Pad, L to Z		2.3		2.7		3.0		3.5	ns
t$_{ENHZ}$	Enable-to-Pad, H to Z		2.8		3.2		3.7		4.3	ns

Note:

1. *For dual-module macros, use t$_{PD}$ + t$_{RD1}$ + t$_{PDn}$, t$_{RCO}$ + t$_{RD1}$ + t$_{PDn}$, or t$_{PD1}$ + t$_{RD1}$ + t$_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Delays based on 10 pF loading.*

A54SX32 Timing Characteristics

Table 1-20 • **A54SX32 Timing Characteristics**
(Worst-Case Commercial Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 70°C)

Parameter	Description	'–3' Speed Min.	'–3' Speed Max.	'–2' Speed Min.	'–2' Speed Max.	'–1' Speed Min.	'–1' Speed Max.	'Std' Speed Min.	'Std' Speed Max.	Units
C-Cell Propagation Delays[1]										
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays[2]										
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{RD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{RD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{RD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns
Input Module Propagation Delays										
t_{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays[2]										
t_{IRD1}	FO = 1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{IRD2}	FO = 2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{IRD3}	FO = 3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{IRD4}	FO = 4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{IRD8}	FO = 8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{IRD12}	FO = 12 Routing Delay		4.0		4.7		5.3		6.2	ns

Note:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

3. *Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

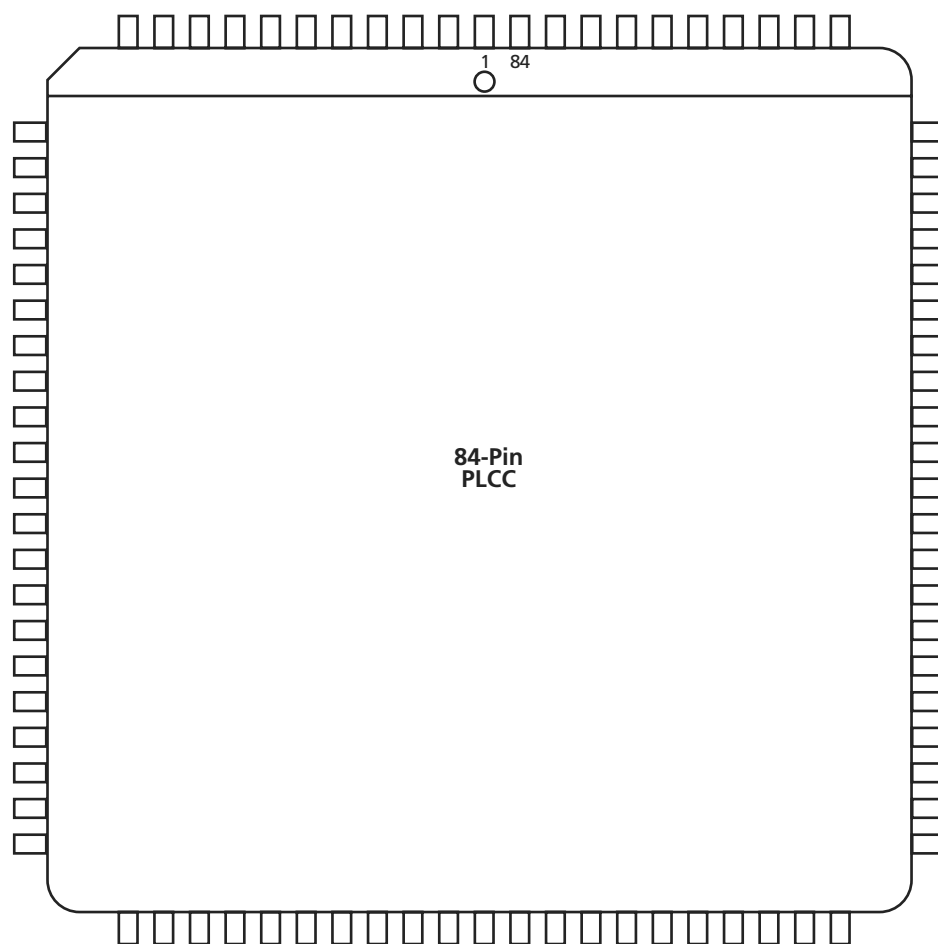# Package Pin Assignments

84-Pin PLCC

Figure 2-1 • **84-Pin PLCC (Top View)**

Note
For Package Manufacturing and Environmental information, visit the Package Resource center at
http://www.actel.com/products/rescenter/package/index.html.

84-Pin PLCC	
Pin Number	**A54SX08 Function**
1	V_{CCR}
2	GND
3	V_{CCA}
4	PRA, I/O
5	I/O
6	I/O
7	V_{CCI}
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V_{CCI}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O

84-Pin PLCC	
Pin Number	**A54SX08 Function**
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V_{CCA}
42	GND
43	V_{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V_{CCA}
60	V_{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V_{CCA}
69	GND
70	I/O

84-Pin PLCC	
Pin Number	**A54SX08 Function**
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

208-Pin PQFP				208-Pin PQFP			
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function	Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
73	NC	I/O	I/O	109	I/O	I/O	I/O
74	I/O	I/O	I/O	110	I/O	I/O	I/O
75	NC	I/O	I/O	111	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	112	I/O	I/O	I/O
77	GND	GND	GND	113	I/O	I/O	I/O
78	V_{CCA}	V_{CCA}	V_{CCA}	114	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND	115	V_{CCI}	V_{CCI}	V_{CCI}
80	V_{CCR}	V_{CCR}	V_{CCR}	116	NC	I/O	I/O
81	I/O	I/O	I/O	117	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	118	I/O	I/O	I/O
83	I/O	I/O	I/O	119	NC	I/O	I/O
84	I/O	I/O	I/O	120	I/O	I/O	I/O
85	NC	I/O	I/O	121	I/O	I/O	I/O
86	I/O	I/O	I/O	122	NC	I/O	I/O
87	I/O	I/O	I/O	123	I/O	I/O	I/O
88	NC	I/O	I/O	124	I/O	I/O	I/O
89	I/O	I/O	I/O	125	NC	I/O	I/O
90	I/O	I/O	I/O	126	I/O	I/O	I/O
91	NC	I/O	I/O	127	I/O	I/O	I/O
92	I/O	I/O	I/O	128	I/O	I/O	I/O
93	I/O	I/O	I/O	129	GND	GND	GND
94	NC	I/O	I/O	130	V_{CCA}	V_{CCA}	V_{CCA}
95	I/O	I/O	I/O	131	GND	GND	GND
96	I/O	I/O	I/O	132	V_{CCR}	V_{CCR}	V_{CCR}
97	NC	I/O	I/O	133	I/O	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}	134	I/O	I/O	I/O
99	I/O	I/O	I/O	135	NC	I/O	I/O
100	I/O	I/O	I/O	136	I/O	I/O	I/O
101	I/O	I/O	I/O	137	I/O	I/O	I/O
102	I/O	I/O	I/O	138	NC	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	139	I/O	I/O	I/O
104	I/O	I/O	I/O	140	I/O	I/O	I/O
105	GND	GND	GND	141	NC	I/O	I/O
106	NC	I/O	I/O	142	I/O	I/O	I/O
107	I/O	I/O	I/O	143	NC	I/O	I/O
108	NC	I/O	I/O	144	I/O	I/O	I/O

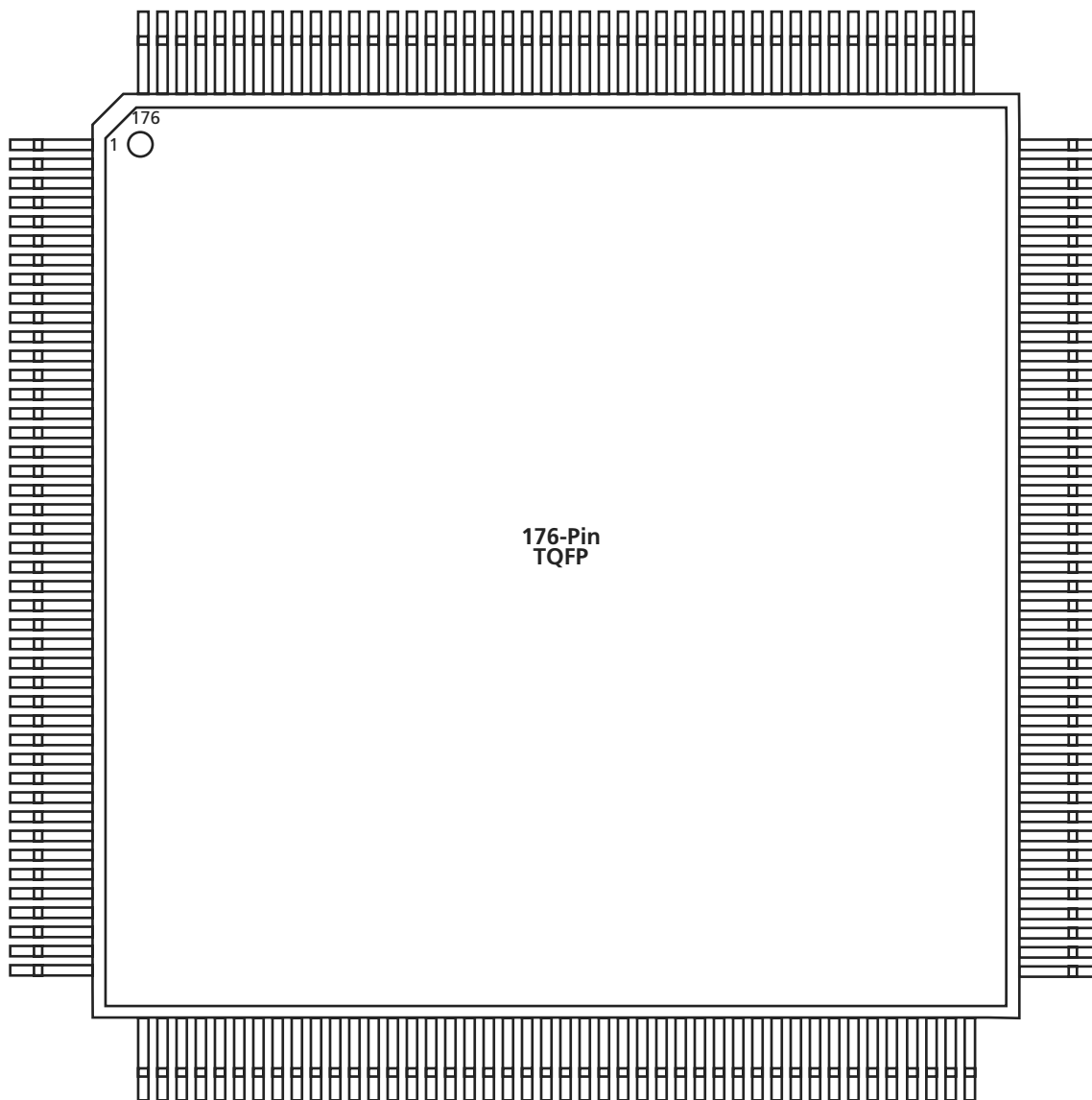**Note:**   * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

176-Pin TQFP

Figure 2-4 • **176-Pin TQFP (Top View)**

Note
For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

176-Pin TQFP				176-Pin TQFP			
Pin Number	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**	**Pin Number**	**A54SX08 Function**	**A54SX16, A54SX16P Function**	**A54SX32 Function**
137	I/O	I/O	I/O	157	PRA, I/O	PRA, I/O	PRA, I/O
138	I/O	I/O	I/O	158	I/O	I/O	I/O
139	I/O	I/O	I/O	159	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}	160	I/O	I/O	I/O
141	I/O	I/O	I/O	161	I/O	I/O	I/O
142	I/O	I/O	I/O	162	I/O	I/O	I/O
143	I/O	I/O	I/O	163	I/O	I/O	I/O
144	I/O	I/O	I/O	164	I/O	I/O	I/O
145	I/O	I/O	I/O	165	I/O	I/O	I/O
146	I/O	I/O	I/O	166	I/O	I/O	I/O
147	I/O	I/O	I/O	167	I/O	I/O	I/O
148	I/O	I/O	I/O	168	NC	I/O	I/O
149	I/O	I/O	I/O	169	V_{CCI}	V_{CCI}	V_{CCI}
150	I/O	I/O	I/O	170	I/O	I/O	I/O
151	I/O	I/O	I/O	171	NC	I/O	I/O
152	CLKA	CLKA	CLKA	172	NC	I/O	I/O
153	CLKB	CLKB	CLKB	173	NC	I/O	I/O
154	V_{CCR}	V_{CCR}	V_{CCR}	174	I/O	I/O	I/O
155	GND	GND	GND	175	I/O	I/O	I/O
156	V_{CCA}	V_{CCA}	V_{CCA}	176	TCK, I/O	TCK, I/O	TCK, I/O

| 313-Pin PBGA		313-Pin PBGA		313-Pin PBGA		313-Pin PBGA	
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
H20	I/O	L25	I/O	R5	I/O	V10	I/O
H22	V_{CCI}	M2	I/O	R7	I/O	V12	I/O
H24	I/O	M4	I/O	R9	I/O	V14	I/O
J1	I/O	M6	I/O	R11	I/O	V16	NC
J3	I/O	M8	I/O	R13	GND	V18	I/O
J5	I/O	M10	I/O	R15	I/O	V20	I/O
J7	NC	M12	GND	R17	I/O	V22	V_{CCA}
J9	I/O	M14	GND	R19	I/O	V24	V_{CCI}
J11	I/O	M16	V_{CCI}	R21	I/O	W1	I/O
J13	CLKA	M18	I/O	R23	I/O	W3	I/O
J15	I/O	M20	I/O	R25	I/O	W5	I/O
J17	I/O	M22	I/O	T2	I/O	W7	NC
J19	I/O	M24	I/O	T4	I/O	W9	I/O
J21	GND	N1	I/O	T6	I/O	W11	I/O
J23	I/O	N3	V_{CCA}	T8	I/O	W13	V_{CCI}
J25	I/O	N5	V_{CCR}	T10	I/O	W15	I/O
K2	I/O	N7	I/O	T12	I/O	W17	I/O
K4	I/O	N9	V_{CCI}	T14	HCLK	W19	I/O
K6	I/O	N11	GND	T16	I/O	W21	I/O
K8	V_{CCI}	N13	GND	T18	I/O	W23	I/O
K10	I/O	N15	GND	T20	I/O	W25	I/O
K12	I/O	N17	I/O	T22	I/O	Y2	I/O
K14	I/O	N19	I/O	T24	I/O	Y4	I/O
K16	I/O	N21	I/O	U1	I/O	Y6	I/O
K18	I/O	N23	V_{CCR}	U3	I/O	Y8	I/O
K20	V_{CCA}	N25	V_{CCA}	U5	V_{CCI}	Y10	I/O
K22	I/O	P2	I/O	U7	I/O	Y12	I/O
K24	I/O	P4	I/O	U9	I/O	Y14	I/O
L1	I/O	P6	I/O	U11	I/O	Y16	I/O
L3	I/O	P8	I/O	U13	I/O	Y18	I/O
L5	I/O	P10	I/O	U15	I/O	Y20	NC
L7	I/O	P12	GND	U17	I/O	Y22	I/O
L9	I/O	P14	GND	U19	I/O	Y24	NC
L11	I/O	P16	I/O	U21	I/O		
L13	GND	P18	I/O	U23	I/O		
L15	I/O	P20	NC	U25	I/O		
L17	I/O	P22	I/O	V2	V_{CCA}		
L19	I/O	P24	I/O	V4	I/O		
L21	I/O	R1	I/O	V6	I/O		
L23	I/O	R3	I/O	V8	I/O		

329-Pin PBGA
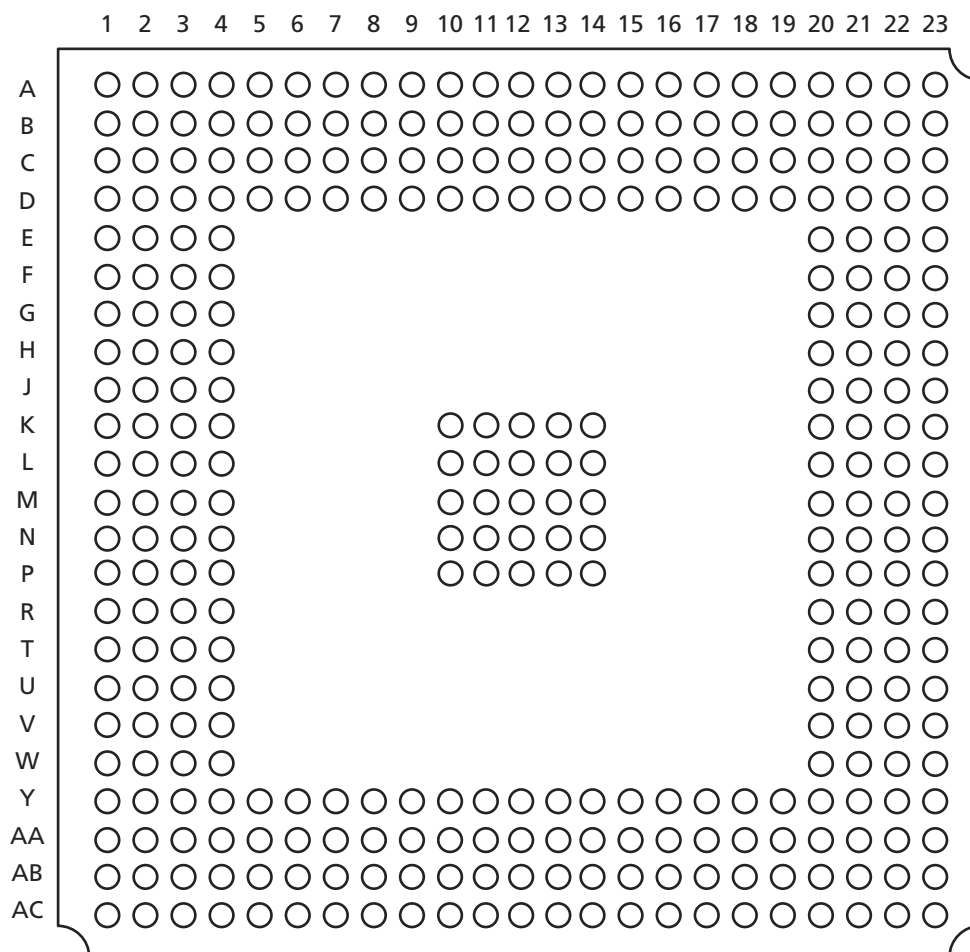
Figure 2-7 • **329-Pin PBGA (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at
http://www.actel.com/products/rescenter/package/index.html.

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.2)	Page
v3.1 (June 2003)	The "Ordering Information" was updated to include RoHS information.	1-ii
	The Product Plan was removed since all products have been released.	N/A
	Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed.	1-6
	The "Dedicated Test Mode" section is new.	1-6
	The "Programming" section is new.	1-7
	A note was added to the "Power-Up Sequencing" table.	1-15
	A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A54SX08, A54SX16, A54SX32.	1-15
	U11 and U13 were added to the "313-Pin PBGA" table.	2-17
v3.0.1	Storage temperature in Table 1-3 was updated.	1-7
	Table 1-1 was updated.	1-5

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

International Traffic in Arms Regulations (ITAR) and Export Administration Regulations (EAR)

The products described in this datasheet are subject to the International Traffic in Arms Regulations (ITAR) or the Export Administration Regulations (EAR). They may require an approved export license prior to their export. An export can include a release or disclosure to a foreign national inside or outside the United States.